PCI CLOCK GENERATOR

MK1493-03B

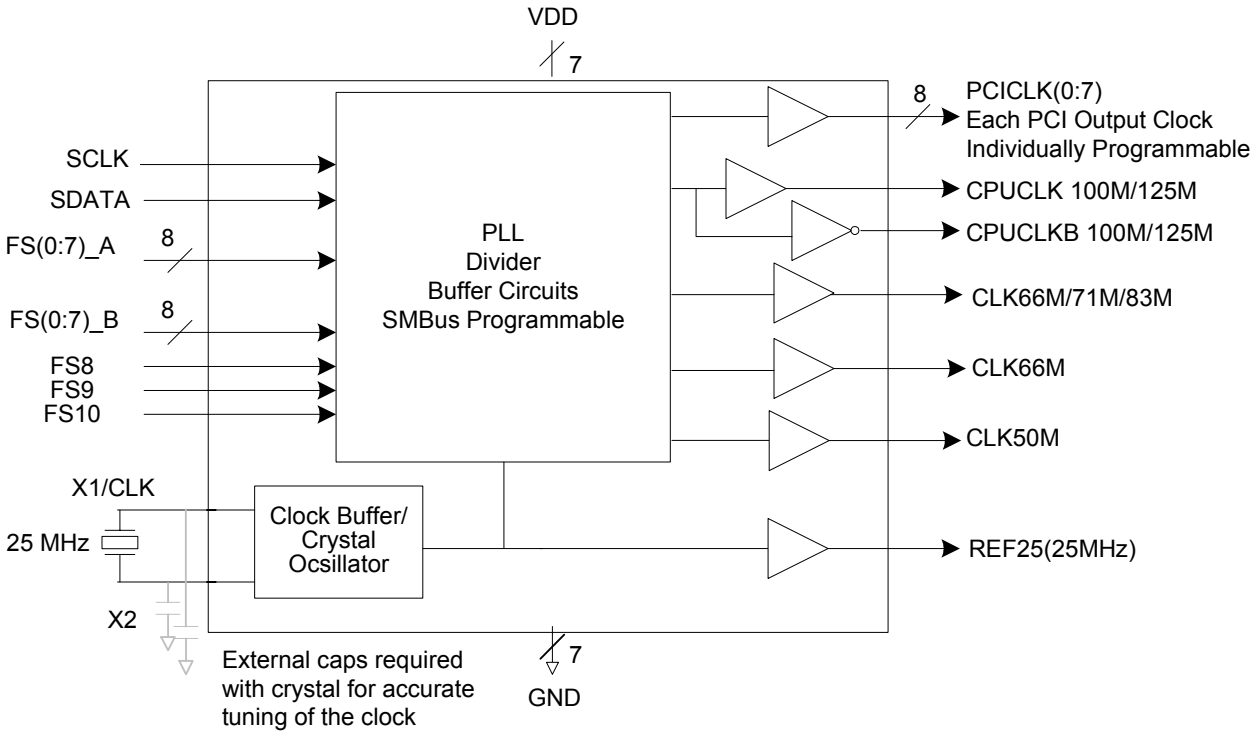
Description

The MK1493-03B is a general purpose clock generator device that provides an integrated clocking solution for PCI /networking applications. It provides eight individually programmable PCI clocks, one CPU clock, three additional fixed PCI clocks, and a 25 MHz reference clock for LAN support. This part incorporates IDT's newest clock technology, offering more robust features and functionality. The device provides a gradual transition from its initial clock frequency to the new one. Using a serially programmable SMBus interface, the MK1493-03B can select the output clock frequency and the transition from the original value to the new value. The SMBus also allows each of the 8 programmable PCI clocks to be individually enabled and disabled.

Features

- Individually programmable (25, 33.33, 50, 66.66 MHz) PCI clocks (Serial or external pin control)
- 1 CPU clock at 100/125 MHz Selectable; single ended/differential selectable
- 1 Clock at 66.66 MHz
- 1 Clock at 66/71/83 MHz selectable
- 1 Clock at 50 MHz
- 25 MHz reference clock
- SMBus Programming
- Power-up default frequency can be selected through FS inputs
- 25 MHz crystal or clock input required
- PCICLK cycle to cycle jitter <250 ps
- CPUCLK cycle to cycle jitter <150 ps
- 48-pin, 240 mil TSSOP Package
- Operating Voltage 3.3 V ±5%
- Commercial (0 to +70°C) and Industrial temperature ranges (-40 to +85°C)

Block Diagram



Pin Assignment 48-pin TSSOP

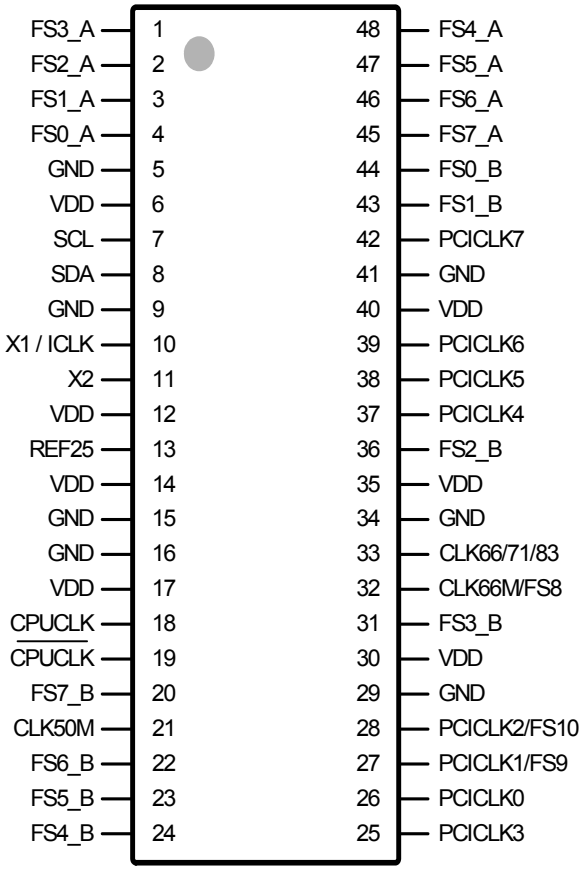


Table 1. Frequency Select

FS(0:7)_B	FS(0:7)_A	PCICLK(0:7)* [1] [2]
0	0	25 MHz
0	1	33.3333 MHz
1	0	50 MHz
1	1	66.6666 MHz

1) Each PCI clock is individually selectable.

Table 2. Input Select (FS8, FS9,FS10&FS11)

FS8 (pin 32)	CPUCLK/$\overline{\text{CPUCLK}}$ [2]
0	125MHz
1	100MHz[3]

FS9 (pin 27)	FS10 (pin 28)	CLK66M/71M/83M [2] (pin 33)
0	0	83.33 MHz[3]
0	1	71.42 MHz
1	0	66.66 MHz
1	1	OFF

2) The changes in frequency are step changes.

3) Default Value upon Power up.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	FS3_A	Input	Freq select input pin for PCI CLK3 per table 1. Internal pull-up resistor 120K.
2	FS2_A	Input	Freq select input pin for PCI CLK2 per table 1. Internal pull-up resistor 120K.
3	FS1_A	Input	Freq select input pin for PCI CLK1 per table 1. Internal pull-up resistor 120K.
4	FS0_A	Input	Freq select input pin for PCI CLK0 per table 1. Internal pull-up resistor 120K.
5	GND	Power	Connect to ground.
6	VDD	Power	Connect to +3.3 V.
7	SCL	Input	Clock pin for SMBus circuitry, 5 V tolerant.
8	SDA	Input	Data pin for SMBus circuitry, 5 V tolerant.
9	GND	Power	Connect to ground.
10	X1/ICLK	Input	Crystal connection/input clock. Connect to a 25 MHz fundamental mode crystal or clock input.
11	X2	XO	Connect to a 25 MHz fundamental mode crystal or leave open for clock input.
12	VDD	Power	Connect to +3.3 V.

Pin Number	Pin Name	Pin Type	Pin Description
13	REF25	Output	Buffered reference output of 25 MHz, (See table2, FS11=0 turns this clock off).
14	VDD	Power	Connect to +3.3 V.
15	GND	Power	Connect to ground.
16	GND	Power	Connect to ground.
17	VDD	Power	Connect to +3.3 V.
18	CPUCLK	Output	100/125 MHz CPU clock.
19	$\overline{\text{CPUCLK}}$	Output	100/125 MHz CPU clock.
20	FS7_B	Input	1 of 4 freq select input pin for PCI CLK7 per table 1. Internal pull-up resistor 120 KΩ
21	CLK50M	Output	50 MHz clock output.
22	FS6_B	Input	Freq select input pin for PCI CLK6 per table 1. Internal pull-up resistor 120 KΩ
23	FS5_B	Input	Freq select input pin for PCI CLK5 per table 1. Internal pull-up resistor 120 KΩ
24	FS4_B	Input	Freq select input pin for PCI CLK4 per table 1. Internal pull-up resistor 120 KΩ
25	PCICLK3	Output	PCI CLK3 (Programmable PCI Clock 3).
26	PCICLK0	Output	PCI CLK0 (Programmable PCI Clock 0).
27	PCICLK1/FS9	I/O	PCI CLK1 (For CLK66/71/83 selection on pin 33, using FS9) (See table 2).
28	PCICLK2/FS10	I/O	PCI CLK2 (For CLK66/71/83 selection on pin 33, using FS10) (See table 2).
29	GND	Power	Connect to ground.
30	VDD	Power	Connect to +3.3 V.
31	FS3_B	Input	Freq select input pin for PCI CLK3 per table 1. Internal pull-up resistor 120 KΩ
32	CLK66M/FS8	I/O	66.66 MHz clock, FS8=1 CPUCLK=100 MHz, FS8=0 CPUCLK=125 MHz) (table 2).
33	CLK66/71/83	Output	Clock66/71/83. Default Value is 83.33 MHz.
34	GND	Power	Connect to ground.
35	VDD	Power	Connect to +3.3 V.
36	FS2_B	Input	Freq select input pin for PCI CLK2 per table 1. Internal pull-up resistor 120 KΩ
37	PCICLK4	Output	PCI CLK4 (Programmable PCI Clock 4).
38	PCICLK5	Output	PCI CLK5 (Programmable PCI Clock 5).
39	PCICLK6	Output	PCI CLK6 (Programmable PCI Clock 6).
40	VDD	Power	Connect to +3.3 V.
41	GND	Power	Connect to ground.
42	PCICLK7	Output	PCI CLK7.
43	FS1_B	Input	Freq select input pin for PCI CLK1 per table 1. Internal Pull up resistor 120 KΩ
44	FS0_B	Input	Freq select input pin for PCI CLK0 per table 1. Internal Pull up resistor 120 KΩ
45	FS7_A	Input	Freq select input pin for PCI CLK7 per table 1. Internal Pull up resistor 120 KΩ
46	FS6_A	Input	Freq select input pin for PCI CLK6 per table 1. Internal Pull up resistor 120 KΩ
47	FS5_A	Input	Freq select input pin for PCI CLK5 per table 1. Internal Pull up resistor 120 KΩ
48	FS4_A	Input	Freq select input pin for PCI CLK4 per table 1. Internal Pull up resistor 120 KΩ

Power Groups

Pin Number		Description
VDD	GND	
12	9	Ref, Crystal Osc Power supply
30, 40	29, 41	PCICLK
35	34	PCI 66 clocks
6	5	SMBus
17	16	CPU Clocks(100MHz)
14	15	PLL

Index Block Write Operation			
Beginning Byte N			
O O O		X Byte	ACK O O O
Byte N + X - 1			
			ACK
P	stoP		

General SM-Bus Serial Interface Information

How to Write:

- Controller (host) sends a start bit
- Controller (host) sends the write address D2 (H)
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = **N**
- IDT clock will **acknowledge**
- Controller sends Byte Count **X**
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT		
Slave Address D2 (H)	WR		
			ACK
Beg Location = N			
			ACK
Data Byte Count = X			
			ACK

How to Read:

- Controller (host) will send a start bit
- Controller (host) sends the write address D2 (H)
- IDT clock will **acknowledge**
- Controller (host) sends the beginning Byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a repeat start bit
- Controller (host) sends the read address Byte D3 (H)
- IDT clock will **acknowledge**
- IDT clock will send the data Byte count = X
- IDT clock sends Byte **N**
- IDT clock sends Byte **N+X-1**
- Controller (host) will need to acknowledge each Byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address D2 (H)	WR =0		
			ACK
Beginning Loc = N			
			ACK
RT	repeat starT		
Slave Address D2 (H)	RD =1		
			ACK
			Data Byte Count=X
ACK			
		X B Y T E S	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	NAK		
P	stoP bit		

SMBus Table 3: Read-Back Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Power UP State
Bit 7	-		RESERVED				0
Bit 6	-	FS vs. SMBus prog	HW/SW select	RW	HW	SW	0
Bit 5	-		RESERVED				0
Bit 4	-		Frequency Selection		See Frequency table 4		0
Bit 3	-						0
Bit 2	-						0
Bit 1	-						0
Bit 0	-						0

SMBus Table 3 (cont.): Output Enable Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Power UP State
Bit 7	40	PCICLK7	Output Control	RW	Disable	Enable	1
Bit 6	39	PCICLK6	Output Control	RW	Disable	Enable	1
Bit 5	38	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4	37	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3	31	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2	28	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	27	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	26	PCICLK0	Output Control	RW	Disable	Enable	1

SMBus Table 3 (cont.): Output Enable Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Power UP State
Bit 7	-		RESERVED				0
Bit 6	-		RESERVED				0
Bit 5	32	CLK66	Output Control	RW	Disable	Enable	1
Bit 4	33	CLK66/71/83	Output Control	RW	Disable	Enable	1
Bit 3	13	REF25	Output Control	RW	Disable	Enable	1
Bit 2	19	$\overline{\text{CPUCLK}}$	Output Control	RW	Disable	Enable	1
Bit 1	18	CPUCLK	Output Control	RW	Disable	Enable	1
Bit 0	21	CLK50	Output Control	RW	Disable	Enable	1

SMBus Table 3 (cont.): Frequency Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Power UP State
Bit 7	4	-	FS0_A	RW	See Frequency Table 1		X
Bit 6	44	-	FS0_B	RW			X
Bit 5	3	-	FS1_A	RW			X
Bit 4	43	-	FS1_B	RW			X
Bit 3	2	-	FS2_A	RW			X
Bit 2	36	-	FS2_B	RW			X
Bit 1	1	-	FS3_A	RW			X
Bit 0	31	-	FS3_B	RW			X

SMBus Table 3 (cont.): Frequency Control Register

Byte 4	Pin #	Control Function	Type	0	1	Power UP State
Bit 7	48	FS4_A	RW	See Frequency Table 1		X
Bit 6	24	FS4_B	RW			X
Bit 5	47	FS5_A	RW			X
Bit 4	23	FS5_B	RW			X
Bit 3	46	FS6_A	RW			X
Bit 2	22	FS6_B	RW			X
Bit 1	45	FS7_A	RW			X
Bit 0	20	FS7_B	RW			X

SMBus Table 3 (cont.): Frequency Control Register

Byte 5	Pin #	Control Function	Type	0	1	Power UP State
Bit 7		FS8	RW	CPU=125M	CPU=100M	1
Bit 6		FS9	RW	00=83.33M, 01=71.42M 10=66.66M, 11=OFF		0
Bit 5		FS10	RW			0
Bit 4		RESERVED	-			0
Bit 3		RESERVED	-			1
Bit 2		RESERVED	-			1
Bit 1		RESERVED	-			1
Bit 0		RESERVED	-			1

SMBus Table 3 (cont.): Reserved

Byte 6	Pin #	Control Function	Type	0	1	Power UP State
Bit 7		RESERVED	-			1
Bit 6		RESERVED	-			1
Bit 5		RESERVED	-			1
Bit 4		RESERVED	-			1
Bit 3		RESERVED	-			1
Bit 2		RESERVED	-			1
Bit 1		RESERVED	-			1
Bit 0		RESERVED	-			1

SMBus Table 3 (cont.): Vendor and Revision ID Register

Byte 7	Pin #	Control Function	Type	0	1	Power UP State
Bit 7		RID3	R	REVISION		0
Bit 6		RID2	R			0
Bit 5		RID1	R			1
Bit 4		RID0	R			0
Bit 3		VID3	R	VENDOR ID		0
Bit 2		VID2	R			0
Bit 1		VID1	R			0
Bit 0		VID0	R			1

SMBus Table 3 (cont.): Byte Count Register

Byte 8	Pin #	Control Function	Type	0	1	Power UP State
Bit 7		BC7	RW	Writing to this Register will confirm how many bytes will be read back, default 08=8 bytes		0
Bit 6		BC6	RW			0
Bit 5		BC5	RW			0
Bit 4		BC4	RW			0
Bit 3		BC3	RW			1
Bit 2		BC2	RW			0
Bit 1		BC1	RW			0
Bit 0		BC0	RW			0

SMBus Table 3 (cont.): Reserved

Byte 9	Pin #	Control Function	Type	0	1	Power UP State
Bit 7		RESERVED	-			1
Bit 6		RESERVED	-			1
Bit 5		RESERVED	-			1
Bit 4		RESERVED	-			1
Bit 3		RESERVED	-			1
Bit 2		RESERVED	-			1
Bit 1		RESERVED	-			1
Bit 0		RESERVED	-			1

SMBus Table 3 (cont.): Programming Enable

Byte 10	Pin #	Name	Control Function	Type	0	1	Power UP State
Bit 7		Programming M/N Enable	Enables prog bytes 11-12	RW	Disabled	Enabled	0
Bit 6		RESERVED	RESERVED	RW			0
Bit 5		RESERVED	RESERVED	RW			0
Bit 4		RESERVED	RESERVED	RW			0
Bit 3		RESERVED	RESERVED	RW			0
Bit 2		RESERVED	RESERVED	RW			0
Bit 1		RESERVED	RESERVED	RW			0
Bit 0		RESERVED	RESERVED	RW			0

SMBus Table 3 (cont.): MN

Byte 11	Pin #	Name	Control Function	Type	0	1	Power UP State
Bit 7		N Div8	N Divider Bit 8	RW			X
Bit 6		M Div6	The decimal representation of M Div(6:0) is equal to reference divider value. default Powerup=latch-in or Byte o ROM table.	RW			X
Bit 5		M Div5		RW			X
Bit 4		M Div4		RW			X
Bit 3		M Div3		RW			X
Bit 2		M Div2		RW			X
Bit 1		M Div1		RW			X
Bit 0		M Div0		RW			X

SMBus Table 3 (cont.): MN

Byte 12	Pin #	Name	Control Function	Type	0	1	Power UP State
Bit 7		N Div7	The decimal representation of N Div(8:0) is equal to feedback divider value. default Powerup=latch-in or Byte o ROM table. N Div8 is in byte11	RW			X
Bit 6		N Div6		RW			X
Bit 5		N Div5		RW			X
Bit 4		N Div4		RW			X
Bit 3		N Div3		RW			X
Bit 2		N Div2		RW			X
Bit 1		N Div1		RW			X
Bit 0		N Div0		RW			X

Table 4. Frequency Margin Selection through SMBus (Byte 0)

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CPUCLK [4] / CPUCLK (MHz)	CLK50 (MHz) [4]	CLK66, 66/71/83 (MHz) [4]	PCICLK (MHz) [4]
0	0	0	0	0	100.00/125.00	50.00	66, 66/71/83	nominal
0	0	0	0	1	nominal + 1%	nominal + 1%	nominal + 1%	nominal + 1%
0	0	0	1	0	nominal + 2%	nominal + 2%	nominal + 2%	nominal + 2%
0	0	0	1	1	nominal + 3%	nominal + 3%	nominal + 3%	nominal + 3%
0	0	1	0	0	nominal + 4%	nominal + 4%	nominal + 4%	nominal + 4%
0	0	1	0	1	nominal + 5%	nominal + 5%	nominal + 5%	nominal + 5%
0	0	1	1	0	nominal + 6%	nominal + 6%	nominal + 6%	nominal + 6%
0	0	1	1	1	nominal + 7%	nominal + 7%	nominal + 7%	nominal + 7%
0	1	0	0	0	nominal + 8%	nominal+ 8%	nominal + 8%	nominal + 8%
0	1	0	0	1	nominal + 9%	nominal + 9%	nominal + 9%	nominal + 9%
0	1	0	1	0	nominal + 10%	nominal + 10%	nominal + 10%	nominal + 10%
0	1	0	1	1	nominal + 11%	nominal + 11%	nominal + 11%	nominal + 11%
0	1	1	0	0	nominal + 12%	nominal + 12%	nominal + 12%	nominal + 12%
0	1	1	0	1	nominal + 13%	nominal + 13%	nominal + 13%	nominal + 13%
0	1	1	1	0	nominal + 14%	nominal + 14%	nominal + 14%	nominal + 14%
0	1	1	1	1	nominal + 15%	nominal + 15%	nominal + 15%	nominal + 15%
1	0	0	0	0	nominal + 16%	nominal + 16%	nominal + 16%	nominal + 16%
1	0	0	0	1	nominal + 17%	nominal + 17%	nominal + 17%	nominal + 17%
1	0	0	1	0	nominal + 18%	nominal + 18%	nominal + 18%	nominal + 18%
1	0	0	1	1	nominal + 19%	nominal + 19%	nominal + 19%	nominal + 19%
1	0	1	0	0	nominal +20%	nominal +20%	nominal +20%	nominal +20%
1	0	1	0	1	nominal +21%	nominal +21%	nominal +21%	nominal +21%
1	0	1	1	0	nominal +22%	nominal +22%	nominal +22%	nominal +22%
1	0	1	1	1	nominal +23%	nominal +23%	nominal +23%	nominal +23%
1	1	0	0	0	nominal +24%	nominal +24%	nominal +24%	nominal +24%
1	1	0	0	1	nominal +25%	nominal +25%	nominal +25%	nominal +25%
1	1	0	1	0	nominal - 3%	nominal - 3%	nominal - 3%	nominal - 3%
1	1	0	1	1	nominal - 5%	nominal - 5%	nominal - 5%	nominal - 5%
1	1	1	0	0	nominal - 10%	nominal - 10%	nominal - 10%	nominal - 10%
1	1	1	0	1	nominal - 15%	nominal - 15%	nominal - 15%	nominal - 15%
1	1	1	1	0	nominal - 20%	nominal - 20%	nominal - 20%	nominal - 20%
1	1	1	1	1	nominal - 25%	nominal - 25%	nominal - 25%	nominal - 25%

[4] The transition of each of these clock frequencies is gradual.

External Components

The MK1493-03B requires a minimum number of external components for proper operation.

Decoupling Capacitor

Decoupling capacitors of 0.1µF and 0.001µF must be connected between each VDD and GND (pins 12&9, 30&29, 40&41, 35&34, 6&5, 17&16, 14&15) as close to the device as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

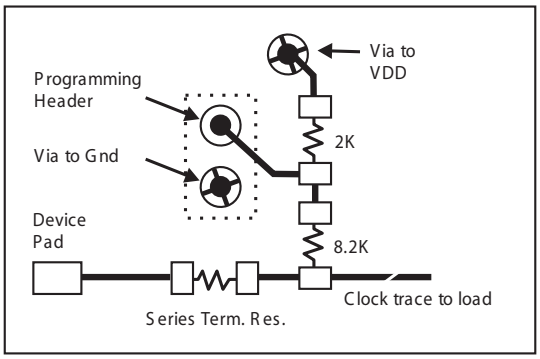
$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. So, for a crystal with a 16 pF load capacitance, two 20 pF [(16-6) x 2] capacitors should be used.

Shared Pin Operation- Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level(voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

Figure 1



To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10Kilo ohm (10 K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 above shows a means of implementing this function when a switch or 2-pin header is used. With no jumpers installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1493-03B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Recommended Operation Conditions

Item	Rating
Max Supply Voltage, VDD	5.5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70° C
Ambient Operating Temperature (industrial)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	° C
Ambient Operating Temperature (industrial)	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.15	3.3	+3.45	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	IIH	VIN=VDD	-5		5	µA
Input Low Current	I_{IL1}	VIN=0V, SDA, SCL no pull-up resistors.	-5			µA
	I_{IL2}	VIN=0V, All other inputs with pull-up resistors	-200			µA
Supply Current	I_{DD}	CL = full load		155		mA
Input Frequency	F_{IN}			25		MHz
Pin Inductance	L_{PIN}				7	nH
Input Capacitance	C_{IN}	Logic inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 and X2 pins			5	pF
CLK Stabilization	T_{STAB}	From VDD Power-up			3	ms

Electrical Characteristics - Input

Unless stated otherwise, **VDD = 3.3 V±5%**, C_L=20 pF Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Crystal or clock input		25		MHz
SM Bus clock	SCL	SM Bus clock		100	110	KHz

Electrical Characteristics - CPUCLK (Single-ended)

Unless stated otherwise, **VDD = 3.3 V±5%**, C_L=20 pF Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency	F_{O1}			100		MHz
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}	I_{OH} = -12 mA,	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA,		0.3	0.4	V
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.0		ns
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V		3.0		ns
Duty Cycle	dt	Measured @ VDD/2	45	50	55	%
C-C Jitter Single ended		Measured @ VDD/2		150		ps

Electrical Characteristics - CPUCLK, $\overline{\text{CPUCLK}}$ (CMOS complimentary)

Unless stated otherwise, **VDD = 3.3 V±5%**, C_L= 20 pF, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Impedance	Z_O	Vo=Vx	15		55	Ohms
Output High Voltage	V_{OH2B}		2.4			V
Output Low Voltage	V_{OL2B}				0.4V	V
Rise Time		V_{OL} = 0.4 V, V_{OH} = 2.4 V	2	2		ns
Fall Time		V_{OH} = 2.4 V, V_{OL} = 0.4 V	2	3		ns
V_{CM}		Common Mode Voltage		1.5		V
Duty Cycle		Measured @ VDD/2	45		55	%
Jitter, Cycle-to-Cycle		Measured @ VDD/2		110		ps
Output to Output Skew between CPU to $\overline{\text{CPU}}$ clocks		Measured @ VDD/2		50		

Electrical Characteristics - CPUCLK, $\overline{\text{CPUCLK}}$ (CMOS complimentary)

Unless stated otherwise, **VDD = 3.3 V±5%**, C_L= 20 pF, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Impedance	Z_O	Vo=Vx	15		55	Ohms
Output High Voltage	V_{OH2B}		2.4			V
Output Low Voltage	V_{OL2B}				0.4V	V
Rise Time		V_{OL} = 0.4 V, V_{OH} = 2.4 V		2		ns
Fall Time		V_{OH} = 2.4 V, V_{OL} = 0.4 V		3		ns
V_{CM}		Common Mode Voltage		1.5		V
Duty Cycle		Measured @ VDD/2	45		55	%
Jitter, Cycle-to-Cycle		Measured @ VDD/2		110		ps
Output to Output Skew between CPU to $\overline{\text{CPU}}$ clocks		Measured @ VDD/2		50		

Electrical Characteristics - CLK50M, CLK66M & CLK66M/71M/83M

Unless stated otherwise, **VDD = 3.3 V±5%**, C_L= 20 pF, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA		0.3	0.4	V
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.0		ns
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.4		ns
Duty Cycle		Measured @ VDD/2	45	50	55	%
Cycle to Cycle Jitter		Measured @ VDD/2		250		ps

Electrical Characteristics - PCICLK

Unless stated otherwise, **VDD = 3.3 V±5%**, C_L=30 pF, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.0	2.4	ns
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V,		2.0	3.0	ns
Duty Cycle		Measured @ VDD/2	45	50	55	%
Output to Output Skew		Measured @ VDD/2		250		ps
Cycle to Cycle Jitter		Measured @ VDD/2		250		ps

Electrical Characteristics - PCICLK

Unless stated otherwise, **VDD = 3.3 V±5%**, C_L=30 pF, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V		3.0		ns
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V,		3.0		ns
Duty Cycle		Measured @ VDD/2	45	50	55	%
Output to Output Skew		Measured @ VDD/2		250		ps
Cycle to Cycle Jitter		Measured @ VDD/2		250		ps

Electrical Characteristics - 25 MHz Reference

Unless stated otherwise, **VDD = 3.3 V±5%**, C_L=20 pF VDD = 3.3 V, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency	F_O			25		MHz
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}	I_{OH} = -1 mA,	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 1 mA,			0.4	V
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.0		ns
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.0		ns
Duty Cycle		Measured @ VDD/2	45	50	55	%
Jitter Cycle to Cycle		Measured @ VDD/2		150		ps

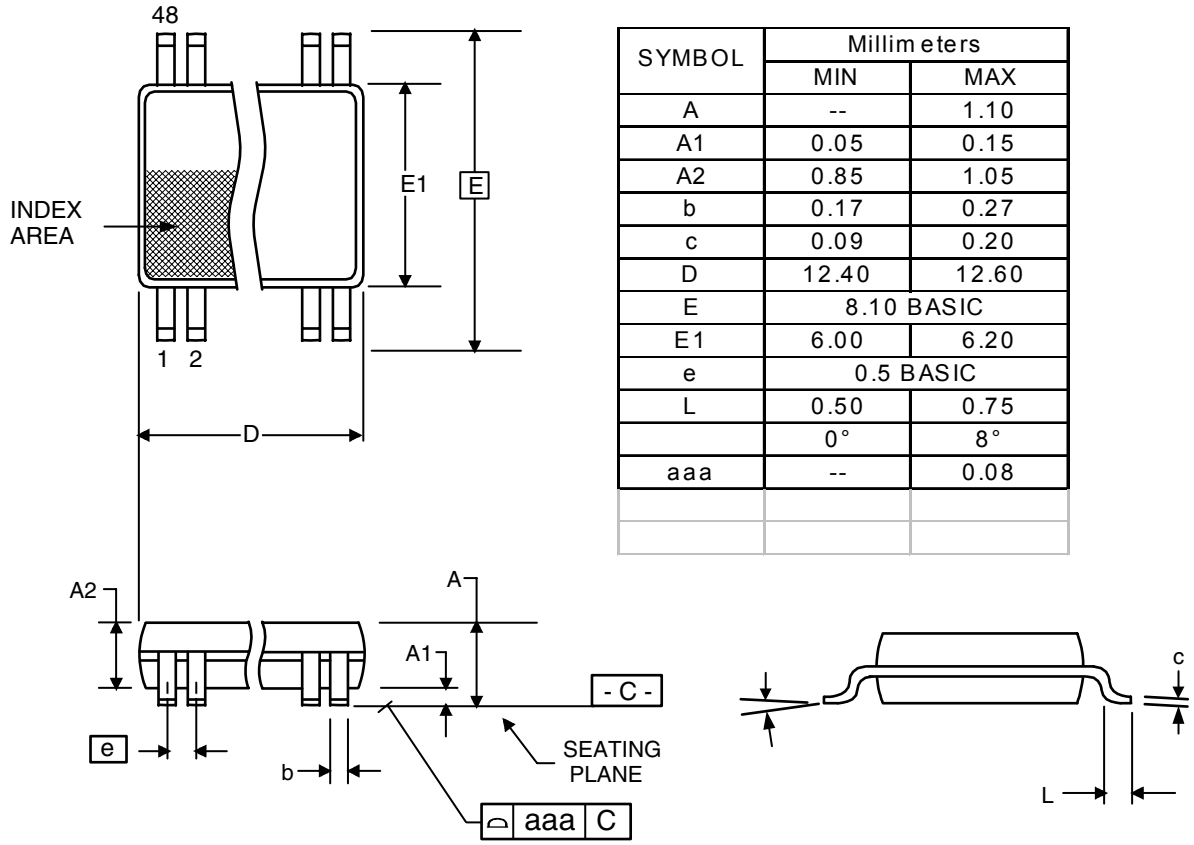
Electrical Characteristics - 25 MHz Reference

Unless stated otherwise, **VDD = 3.3 V±5%**, C_L=20 pF VDD = 3.3 V, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency	F_O			25		MHz
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}	I_{OH} = -1 mA,	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 1 mA,			0.4	V
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.0		ns
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.0		ns
Duty Cycle		Measured @ VDD/2	40	50	60	%
Jitter Cycle to Cycle		Measured @ VDD/2		150		ps

Package Outline and Package Dimensions (48-pin TSSOP, 6.10 mm Body, .50mm pitch)

Package dimensions are kept current with JEDEC Publication No. 95



SYMBOL	Millimeters	
	MIN	MAX
A	--	1.10
A1	0.05	0.15
A2	0.85	1.05
b	0.17	0.27
c	0.09	0.20
D	12.40	12.60
E	8.10 BASIC	
E1	6.00	6.20
e	0.5 BASIC	
L	0.50	0.75
	0°	8°
aaa	--	0.08

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1493-03BGLF	MK1493-03BGLF	Tubes	48-pin TSSOP	0 to +70° C
MK1493-03BGLFTR	MK1493-03BGLF	Tape and Reel	48-pin TSSOP	0 to +70° C
MK1493-03BGILF	1493-03BGIL	Tubes	48-pin TSSOP	-40 to +85° C
MK1493-03BGILFTR	1493-03BGIL	Tape and Reel	48-pin TSSOP	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

ERRATA

Changes from MK1493-03 to MK1493-03A Data Sheet

Page 1 The part number changed from MK1493-03 to MK1493-03A
FS11 on the block diagram is removed
Page 2, Table 2, FS11 column removed
Default Output clock value for CLK66M/71M/83M is 83M.
Page3 Pin 33 description/function changed from I/O pin to Output pin only. The FS11 input option is deleted
Page6 Table 3 Byte2, bit3 (pin13) and bit5 (pin32) changed from Disable upon power upon to Enable upon powerup.
Page 7 Table 3 Byte 5, Bit 4 changed from FS11 to reserved
Byte 5 bit 5 and 6 changed to 0 upon power up.
Page 8 Byte 7 bit 4 changed from 0 to 1
Page 13 SMBUs max clock speed increased from 64KHz to 110KHz
Page 17 Ordering Information changed from MK1493-03G to MK1493-03AG

Changes from MK1493-03A to MK1493-03B Data Sheet

Page 1 The part number changed from MK1493-03A to MK1493-03B
Page 8 SMBUS vendor Revision ID
Byte 7 Power up state changed from o to 1, Bit 4 Power up state changed from 1 to 0
Page 13 The fall time for CPUCLK (single ended) and complimentary the V_{OL}=0.8V changed to V_{OL}=0.4V
Page 16 The part ordering number changed from MK1493-03AG to MK1493-03BG; added LF.

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