

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4060B

MSI

14-stage ripple-carry binary counter/divider and oscillator

Product specification
File under Integrated Circuits, IC04

January 1995

14-stage ripple-carry binary counter/divider and oscillator

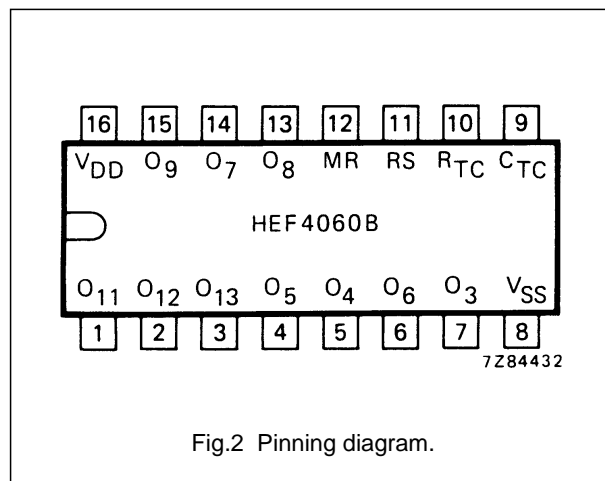
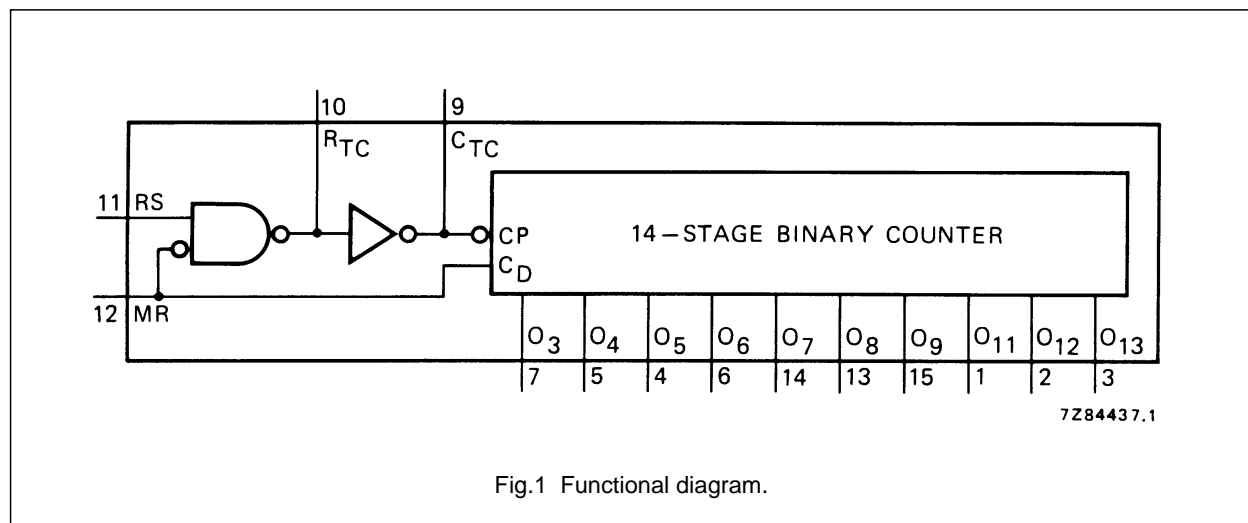
HEF4060B MSI

DESCRIPTION

The HEF4060B is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (O_3 to O_9 and O_{11} to O_{13}) and an overriding asynchronous master reset input (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may

be replaced by an external clock signal at input RS. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (O_3 to O_9 and O_{11} to O_{13} = LOW), independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.



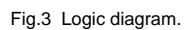
PINNING

MR	master reset
RS	clock input/oscillator pin
R_{TC}	oscillator pin
C_{TC}	external capacitor connection
O_3 to O_9	counter outputs
O_{11} to O_{13}	

HEF4060BP(N): 16-lead DIL; plastic (SOT38-1)
 HEF4060BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
 HEF4060BT(D): 16-lead SO; plastic (SOT109-1)
 (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

HEF4060B
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AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays	5 10 15	t_{PHL}	210 80 50	420 160 100	ns ns ns	183 ns + (0,55 ns/pF) C_L 69 ns + (0,23 ns/pF) C_L 42 ns + (0,16 ns/pF) C_L
	5 10 15	t_{PLH}	210 80 50	420 160 100	ns ns ns	183 ns + (0,55 ns/pF) C_L 69 ns + (0,23 ns/pF) C_L 42 ns + (0,16 ns/pF) C_L
	5 10 15	t_{PHL}	25 10 6	50 20 12	ns ns ns	
	5 10 15	t_{PLH}	25 10 6	50 20 12	ns ns ns	
	5 10 15	t_{PHL}	100 40 30	200 80 60	ns ns ns	73 ns + (0,55 ns/pF) C_L 29 ns + (0,23 ns/pF) C_L 22 ns + (0,16 ns/pF) C_L
Output transition times	5 10 15	t_{THL}	60 30 20	120 60 40	ns ns ns	10 ns + (1,0 ns/pF) C_L 9 ns + (0,42 ns/pF) C_L 6 ns + (0,28 ns/pF) C_L
	5 10 15	t_{TLH}	60 30 20	120 60 40	ns ns ns	10 ns + (1,0 ns/pF) C_L 9 ns + (0,42 ns/pF) C_L 6 ns + (0,28 ns/pF) C_L
Minimum clock pulse width input RS	5	t_{WRSH}	120	60	ns	
	10		50	25	ns	
	15		30	15	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	50	25	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t_{RMR}	160	80	ns	
	10		80	40	ns	
	15		60	30	ns	
Maximum clock pulse frequency input RS	5	f_{max}	4	8	MHz	
	10		10	20	MHz	
	15		15	30	MHz	

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AC CHARACTERISTICS

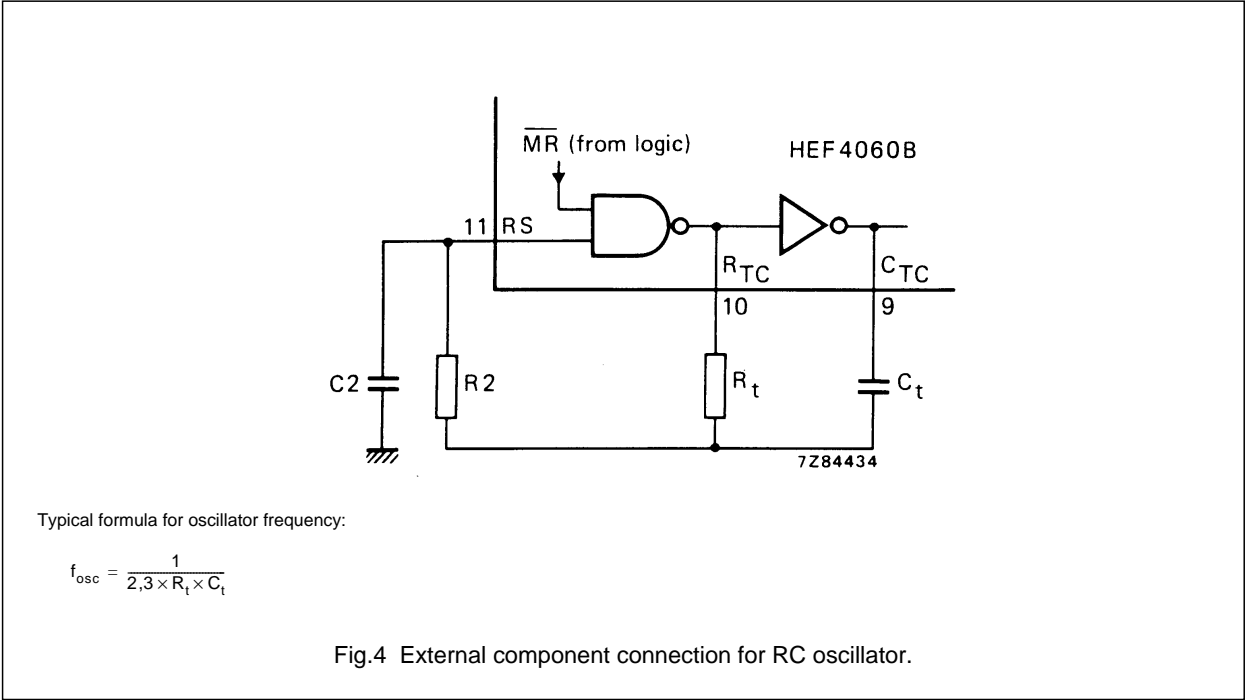
V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW) ⁽¹⁾
Dynamic power dissipation per package (P)	5	700 f _i + f _o C _L V _{DD} ²
	10	3 300 f _i + f _o C _L V _{DD} ²
	15	8 900 f _i + f _o C _L V _{DD} ²
Total power dissipation when using the on-chip oscillator (P)	5	700 f _{osc} + f _o C _L V _{DD} ² + 2C _t V _{DD} ² f _{osc} + 690 V _{DD}
	10	3 300 f _{osc} + f _o C _L V _{DD} ² + 2C _t V _{DD} ² f _{osc} + 6 900 V _{DD}
	15	8 900 f _{osc} + f _o C _L V _{DD} ² + 2C _t V _{DD} ² f _{osc} + 22 000 V _{DD}

Notes

1. where:
- f_i = input frequency (MHz)
 - f_o = output frequency (MHz)
 - C_L = load capacitance (pF)
 - V_{DD} = supply voltage (V)
 - C_t = timing capacitance (pF)
 - f_{osc} = oscillator frequency (MHz)

RC oscillator



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Timing component limitations

The oscillator frequency is mainly determined by $R_t C_t$, provided $R_t \ll R_2$ and $R_2 C_2 \ll R_t C_t$. The function of R_2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOC MOS 'ON' resistance in series with it, which typically is $500\ \Omega$ at $V_{DD} = 5\text{ V}$, $300\ \Omega$ at $V_{DD} = 10\text{ V}$ and $200\ \Omega$ at $V_{DD} = 15\text{ V}$.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t \geq 100\text{ pF}$, up to any practical value,
 $10\text{ k}\Omega \leq R_t \leq 1\text{ M}\Omega$.

Typical crystal oscillator circuit

In Fig.5, R_2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary.

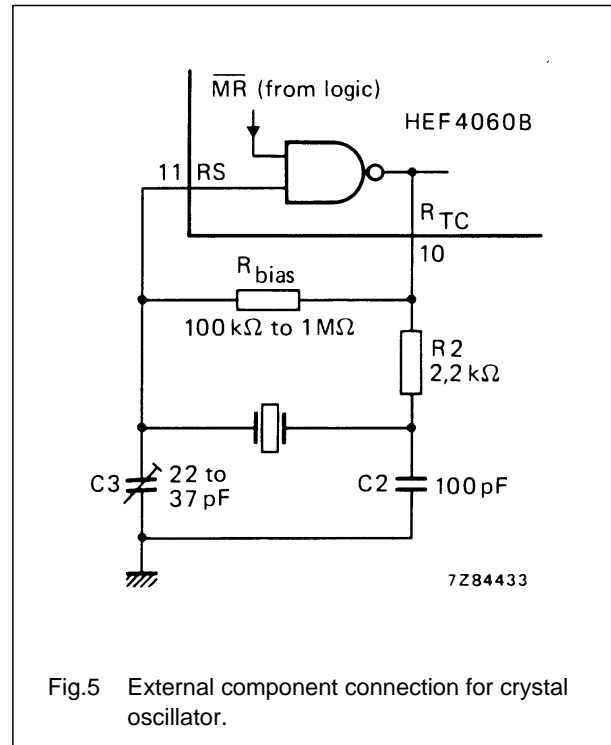


Fig.5 External component connection for crystal oscillator.

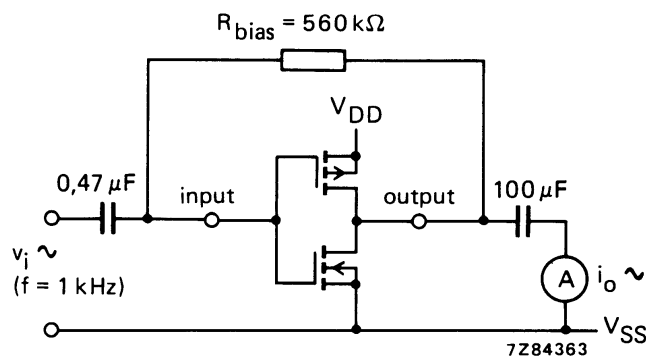


Fig.6 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.7); $MR = LOW$.

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