

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4042B** **MSI** Quadruple D-latch

Product specification  
File under Integrated Circuits, IC04

January 1995

# Quadruple D-latch

# HEF4042B MSI

### DESCRIPTION

The HEF4042B is a 4-bit latch with four data inputs ( $D_0$  to  $D_3$ ), four buffered latch outputs ( $O_0$  to  $O_3$ ), four buffered complementary latch outputs ( $\bar{O}_0$  to  $\bar{O}_3$ ) and two common enable inputs ( $E_0$  and  $E_1$ ). Information on  $D_0$  to  $D_3$  is transferred to  $O_0$  to  $O_3$  while both  $E_0$  and  $E_1$  are in the same state, either HIGH or LOW.  $O_0$  to  $O_3$  follow  $D_0$  to  $D_3$  as long as both  $E_0$  and  $E_1$  remain in the same state. When  $E_0$  and  $E_1$  are different,  $D_0$  to  $D_3$  do not affect  $O_0$  to  $O_3$  and the information in the latch is stored.  $\bar{O}_0$  to  $\bar{O}_3$  are always the complement of  $O_0$  to  $O_3$ . The exclusive-OR input structure allows the choice of either polarity for  $E_0$  and  $E_1$ . With one enable input HIGH, the other enable input is active HIGH; with one enable input LOW, the other enable input is active LOW.

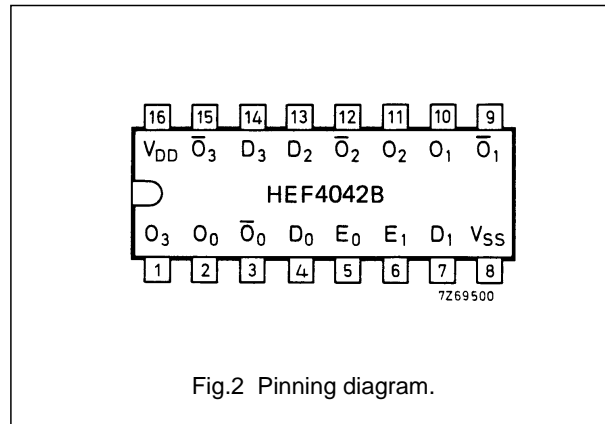


Fig.2 Pinning diagram.

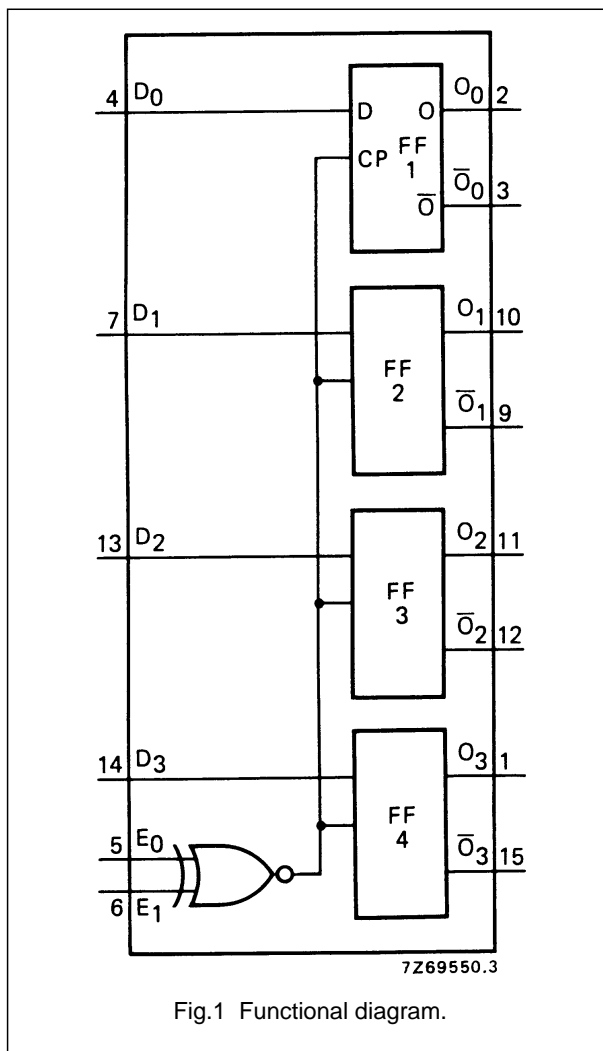


Fig.1 Functional diagram.

- HEF4042BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4042BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4042BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

### PINNING

- $D_0$  to  $D_3$  data inputs
- $E_0$  and  $E_1$  enable inputs
- $O_0$  to  $O_3$  parallel latch outputs
- $\bar{O}_0$  to  $\bar{O}_3$  complementary parallel latch outputs

### APPLICATION INFORMATION

Some examples of applications for the HEF4042B are:

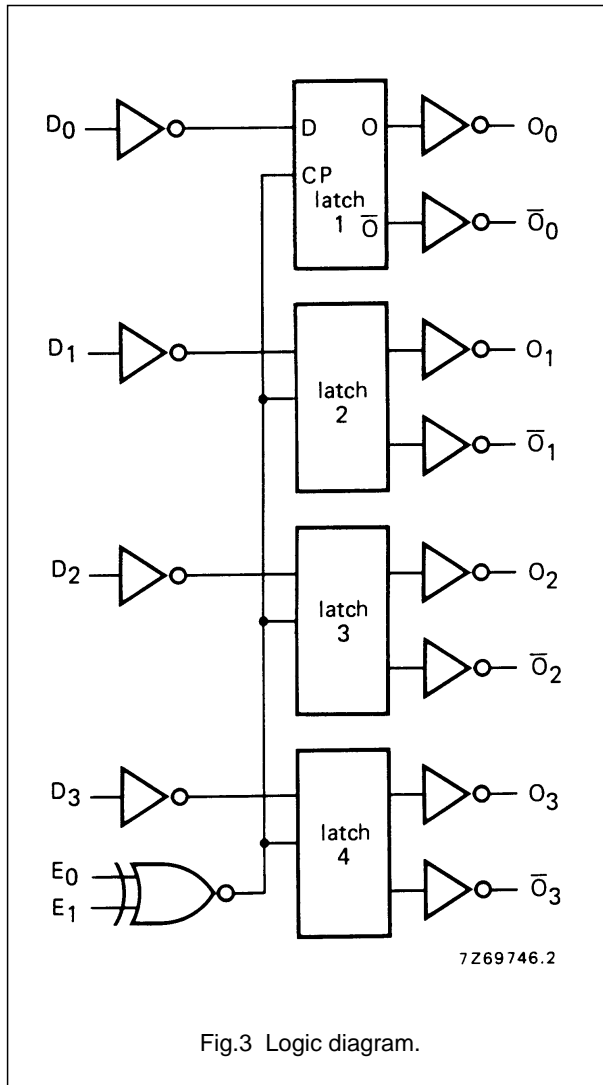
- Buffer storage
- Holding register

### FAMILY DATA, $I_{DD}$ LIMITS category MSI

See Family Specifications

Quadruple D-latch

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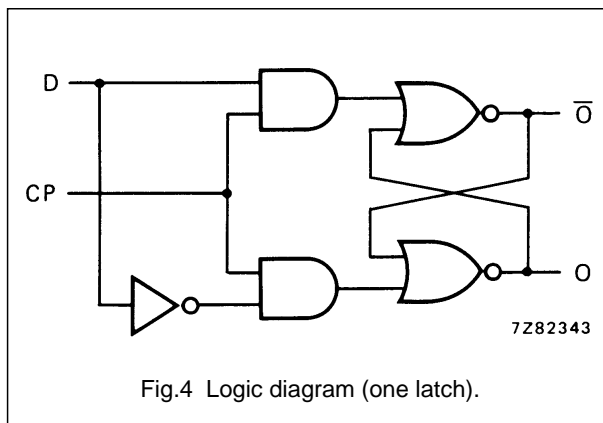


FUNCTION TABLE

$E_0$	$E_1$	OUTPUT $O_n$
L	L	$D_n$
L	H	latched
H	L	latched
H	H	$D_n$

Note

- H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage).



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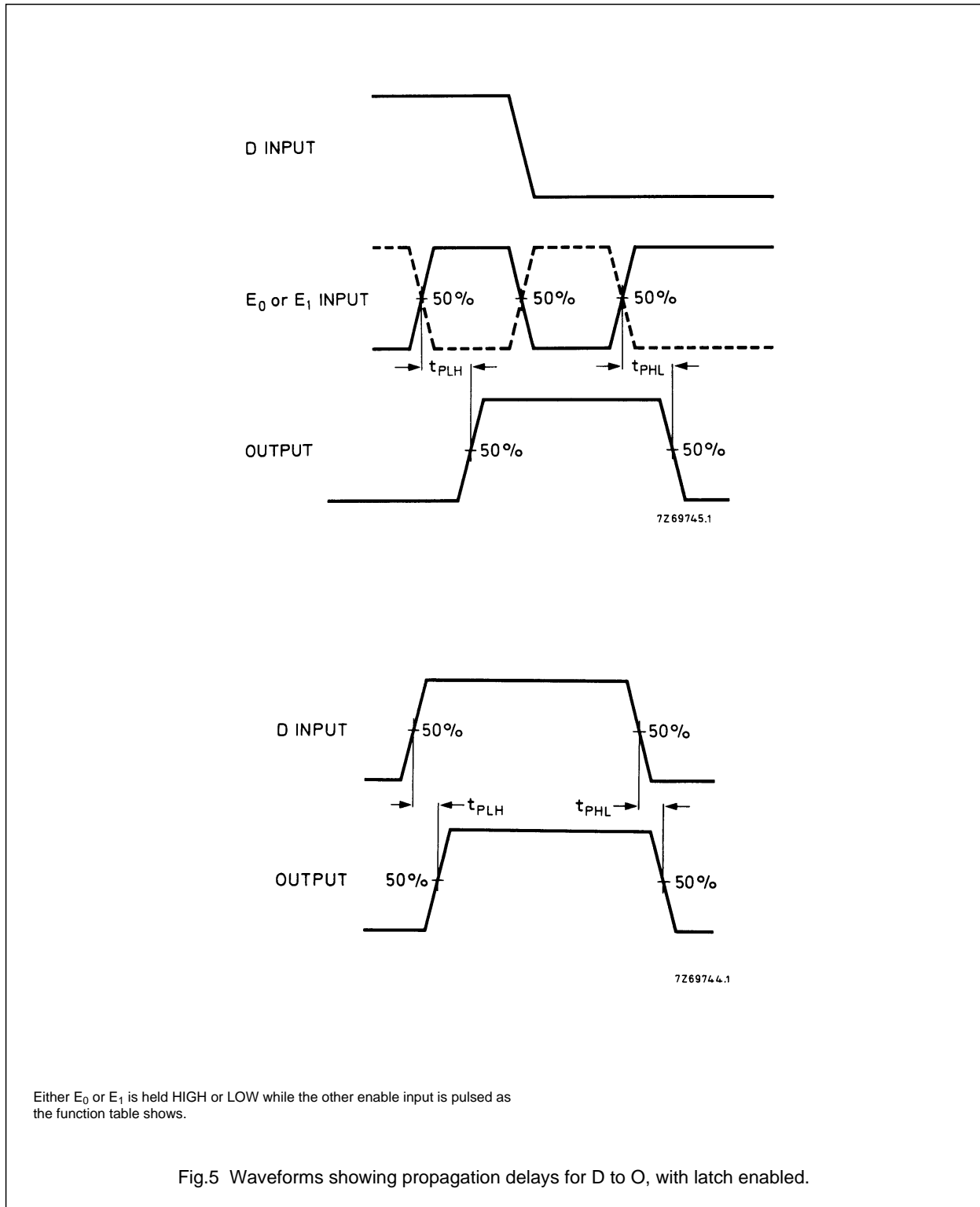
## AC CHARACTERISTICS

$V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA				
Propagation delays	5	$t_{PHL}$		95	190	ns	$67 \text{ ns} + (0,55 \text{ ns/pF}) C_L$			
				D $\rightarrow$ O, $\bar{O}$						
				HIGH to LOW						
	LOW to HIGH	10	$t_{PLH}$		40	80	ns	$28 \text{ ns} + (0,23 \text{ ns/pF}) C_L$		
					15	55	ns		$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
					5	85	175			ns
	E $\rightarrow$ O, $\bar{O}$	10	$t_{PHL}$		130	260	ns	$102 \text{ ns} + (0,55 \text{ ns/pF}) C_L$		
					15	30	60		ns	$38 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
					5	120	245		ns	
	LOW to HIGH	10	$t_{PLH}$		50	105	ns	$38 \text{ ns} + (0,23 \text{ ns/pF}) C_L$		
					15	35	75		ns	$27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
					5	60	120		ns	
Output transition times	5	$t_{THL}$		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$			
				HIGH to LOW						
				10	30	60		ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15	20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$					
	LOW to HIGH	10	$t_{TLH}$			60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
						15	20	40		ns
5					30	60	ns			
Set-up time D $\rightarrow$ E	5	$t_{su}$		30	10	ns	see also waveforms Figs 5 and 6			
				10	20	5		ns		
				15	20	5		ns		
Hold time D $\rightarrow$ E	5	$t_{hold}$		15	-5	ns				
				10	15	0		ns		
				15	15	0		ns		
Minimum enable pulse width	5	$t_{WE}$		90	45	ns				
				10	40	20		ns		
				15	30	15		ns		

	$V_{DD}$ V	TYPICAL FORMULA FOR P (W)	
Dynamic power dissipation per package (P)	5	$3800 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$15\,700 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$41\,100 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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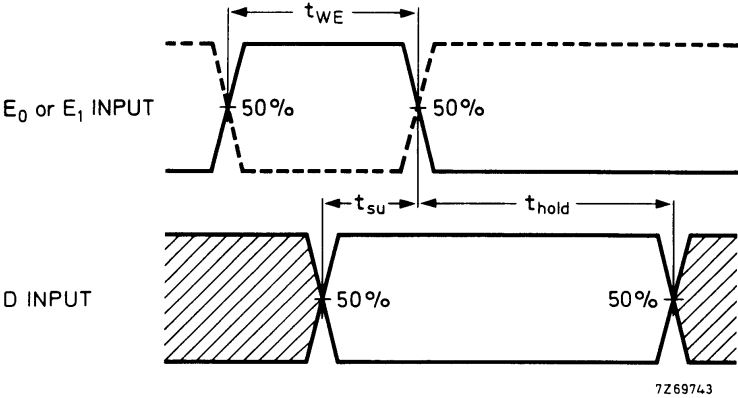


Fig.6 Waveforms showing minimum enable pulse width, set-up time and hold time for E and D. Set-up and hold-times are shown as positive values but may be specified as negative values.