Ordering number : ENA2013

SANYO Semiconductors
DATA SHEET

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LV8138V — Bi-CMOS IC For Brushless Motor Drive Sine wave PWM Drive, Pre driver IC

Overview

The LV8138V is a PWM system pre driver IC designed for three-phase brushless motors.
This IC reduces motor driving noise by using a high-efficiency, sine wave PWM drive type.
It incorporates a full complement of protection circuits and, by combining it with a hybrid IC in the STK611 or STK5C4 series, the number of components used can be reduced and a high level of reliability can be achieved. Furthermore, its power-saving mode enables the power consumption in the standby mode to be reduced to zero. This IC is optimally suited for driving various large-size motors such as those used in air conditioners and hot-water heaters.

Features

- Three-phase bipolar drive
- Sine wave PWM drive
- Drive phase setting function (Set 0-58 degrees 32 steps: There is an adjustment function corresponding to the CTL pin input)
- Supports power saving mode(power saving mode at CTL pin voltage of 1.0V (typ) or less; I_{CC} = 0mA, HB pin turned off)
- Supports bootstrap
- Automatic recovery type constraint protection circuit
- Forward/reverse switching circuit, Hall bias pin
- Current limiter circuit, low-voltage protection circuit, and thermal shutdown protection circuit
- FG1 and FG3 output (360-degree electrical angle/1 pulse and 3 pulses)

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Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max	V_{CC} pin	18	V
Output current	I_O max		15	mA
Allowable power dissipation	Pd max1	Independent IC	0.45	W
	Pd max2	Mounted on a specified circuit board.*	1.05	W
CTL pin applied voltage	V_{CTL} max		18	V
FG1,FG3 pin applied voltage	$V_{FG}1$ max $V_{FG}3$ max		18	V
Junction temperature	Tj max		150	°C
Operating temperature	Topr		-40 to +105	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified circuit board : 114.3mm × 76.1mm × 1.6mm, glass epoxy
Note 1) Absolute maximum ratings represent the values that cannot be exceeded for any length of time.
Note 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for further details.

Allowable Operating range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		9.5 to 16.5	V
5V constant voltage output current	I_{REG}		10	mA
HB pin output current	I_{HB}		30	mA
FG1,FG3 pin output current	$I_{FG}1$, $I_{FG}3$		10	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 15V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$			5.0	8.0	mA
Supply current 2	$I_{CC}2$	At stop CTL ≤ 1.0V typ		0	20	μA
Output Block						
High level output voltage	V_{HO}	I_O = -10mA	VREG-0.35	VREG-0.15		V
Low level output voltage	V_{LO}	I_O = 10mA		0.15	0.3	V
Lower output ON resistance	$R_{ON}L$	I_O = 10mA		15	30	Ω
Upper output ON resistance	$R_{ON}H$	I_O = -10mA		15	35	Ω
Output leakage current	$I_O$leak				10	μA
Minimum output pulse width	Tmin			2.0	4.0	μs
Output minimum dead time	Tdt			2.0	4.0	μs
5V Constant Voltage Output						
Output voltage	VREG	I_O = -5mA	4.7	5.0	5.3	V
Voltage fluctuation	ΔV (REG1)	V_{CC} = 9.5 to 16.5V, I_O = -5mA			100	mV
Load fluctuation	ΔV (REG2)	I_O = -5 to -10mA			100	mV
Hall Amplifier						
Input bias current	IB (HA)		-2		0	μA
Common-mode input voltage range 1	VICM1	When a Hall element is used	0.3		VREG-1.7	V
Common-mode input voltage range 2	VICM2	Single-sided input bias mode (when a Hall IC is used)	0		VREG	V
Hall input sensitivity	VHIN	Sine wave, Hall element offset = 0V	80			mVp-p
Hysteresis width	ΔV_{IN} (HA)		9	20	40	mV
Input voltage Low → High	VSLH		5	11	19	mV
Input voltage High → Low	VSHL		-19	-11	-5	mV

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CSD Oscillator Circuit						
High level output voltage	V_{OH} (CSD)		2.7	3.0	3.3	V
Low level output voltage	V_{OL} (CSD)		0.8	1.0	1.2	V
Amplitude	V (CSD)		1.75	2.0	2.25	Vp-p
External capacitor charging current	ICHG1 (CSD)	VCHG1 = 2.0V	-17	-10	-3	μA
External capacitor discharging current	ICHG2 (CSD)	VCHG2 = 2.0V	3	10	17	μA
Oscillation frequency	f (CSD)	C = 0.22μF (design target value)		113.6		Hz
PWM Oscillator (PWM pin)						
High level output voltage	V_{OH} (PWM)		3.3	3.5	3.7	V
Low level output voltage	V_{OL} (PWM)		1.3	1.5	1.7	V
Amplitude	V (PWM)		1.78	2.0	2.22	Vp-p
Oscillation frequency	f (PWM)	C = 2200pF, R = 15kΩ (design target value)		17		kHz
Current Limiter Operation						
Limiter voltage	VRF		0.225	0.25	0.275	V
Thermal Shutdown Protection Operation						
Thermal shutdown protection operating temperature	TSD	* Design target value (junction temperature)	150	175		°C
Hysteresis width	ΔTSD	* Design target value (junction temperature)		35		°C
TH pin						
Protection start voltage	VTH		0.25	0.6	1.05	V
Hysteresis width	ΔVTH		0.2	0.4	0.6	V
HB pin						
Output ON resistance	R_{ON} (HB)	IHB = 10mA		15	30	Ω
Output leakage current	I_L (HB)	Power saving mode V_{CC} = 15V			10	μA
Low Voltage Protection Circuit (detecting V_{CC} voltage)						
Operation voltage	VSD		7.0	8.0	9.0	V
Hysteresis width	ΔVSD		0.25	0.5	0.75	V
FG1 FG3 Pin						
Output ON resistance	R_{ON} (FG)	IFG = 5mA		40	60	Ω
Output leakage current	I_L (FG)	VFG = 18V			10	μA
CTL Amplifier (drive mode)						
Input voltage range	V_{IN} (CTL)		0		VCC	V
High level input voltage	V_{IH} (CTL)	PWM ON duty 100%	5.1	5.4	5.7	V
Middle level input voltage	V_{IM} (CTLI)	PWM ON duty 0%	1.8	2.1	2.4	V
CTL Amplifier (power saving mode)						
Low level input voltage	$V_{IL}1$ (CTL)	Power saving mode		1.0	1.5	V
Hysteresis width	ΔCTL		0.15	0.5	0.85	V
Input current	I_{IH} (CTLI)	CTL = 3.5V	10	18	26	μA
F/R Pin						
High level input voltage	V_{IH} (FR)		3.0		VREG	V
Low level input voltage	V_{IL} (FR)		0		0.7	V
Input open voltage	V_{IO} (FR)			0	0.3	V
Hysteresis width	V_{IS} (FR)		0.21	0.31	0.41	V
High level input current	I_{IH} (FR)	VF/R = VREG	10	50	100	μA
Low level input current	I_{IL} (FR)	VF/R = 0V	-10	0	+10	μA

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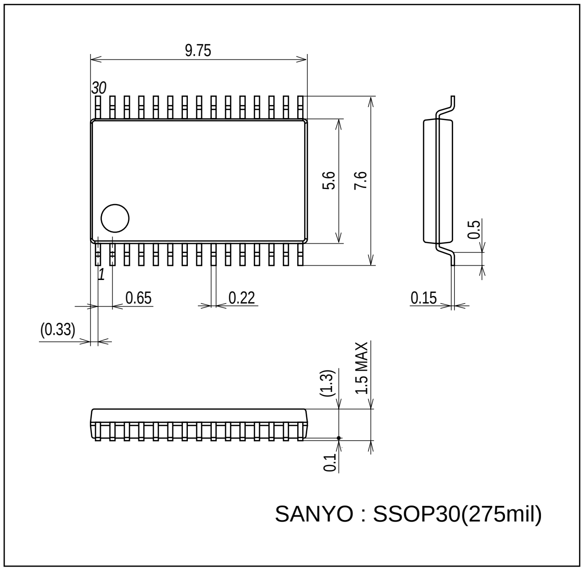
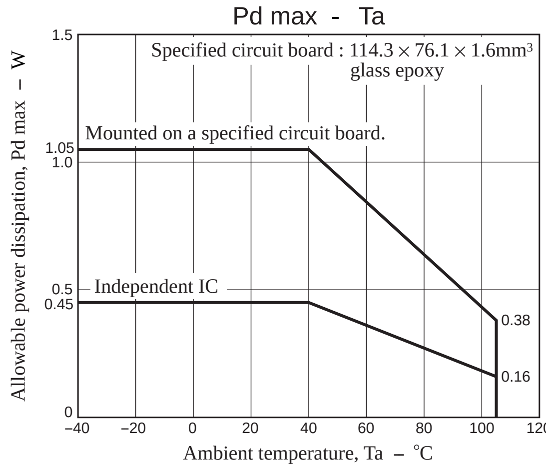
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FAULT Pin						
Drive stop voltage	VFOF		0		0.35	V
Drive start voltage	VFON		3.0		VREG	V
Input open voltage	V_{IO} (FLT)		4.6	VREG		V
High level input current	I_{IH} (FLT)	VFLT=VREG		0	10	μA
Low level input current	I_{IL} (FLT)	VFLT=0V	-250	-160	-70	μA
ADP1 Pin (drive phase adjustment)						
Minimum lead angle	Vadp01	ADP1 pin = 0V		0	2	Deg
Maximum lead angle	Vadp16	ADP1 pin = VREG	56	58		Deg
Current ratio with the ADP2 pin current	ADP	CTL = 3.75V, IADP1/IADP2	1.45	2	2.55	A/A
ADP2 Pin (drive phase adjustment)						
High level output voltage	VADP2H	CTL = 5.4V	1.95	2.5	3.05	V
Low level output voltage	VADP2L	CTL = 0V	0		0.51	V
DPL Pin (drive-phase-adjustment limit setting pin)						
Lead angle limit high level voltage	VDPLH		3.3	3.5	3.8	V
Lead angle limit low level voltage	VDPLL		1.3	1.5	1.7	V

* These are design target values and no measurements are made.

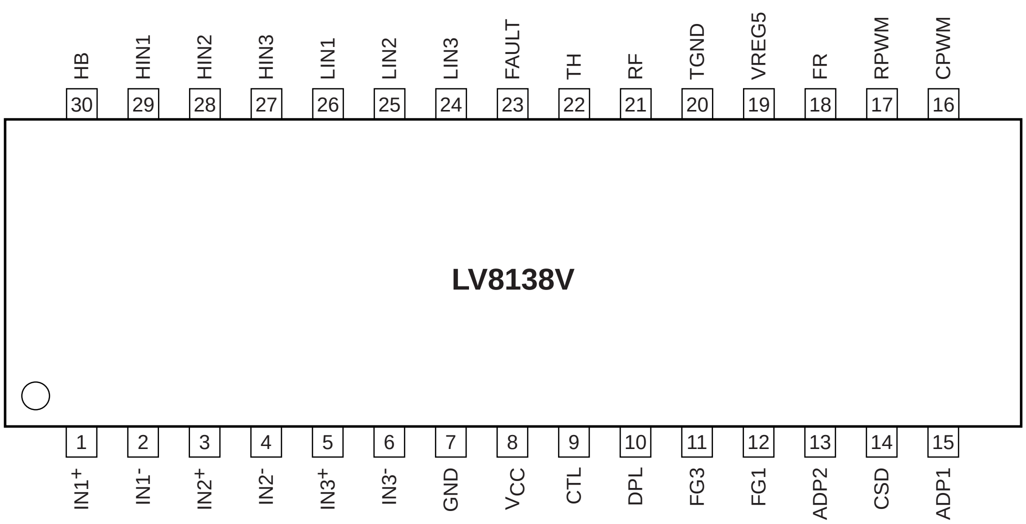
Package Dimensions

nit : mm (typ)
3191C



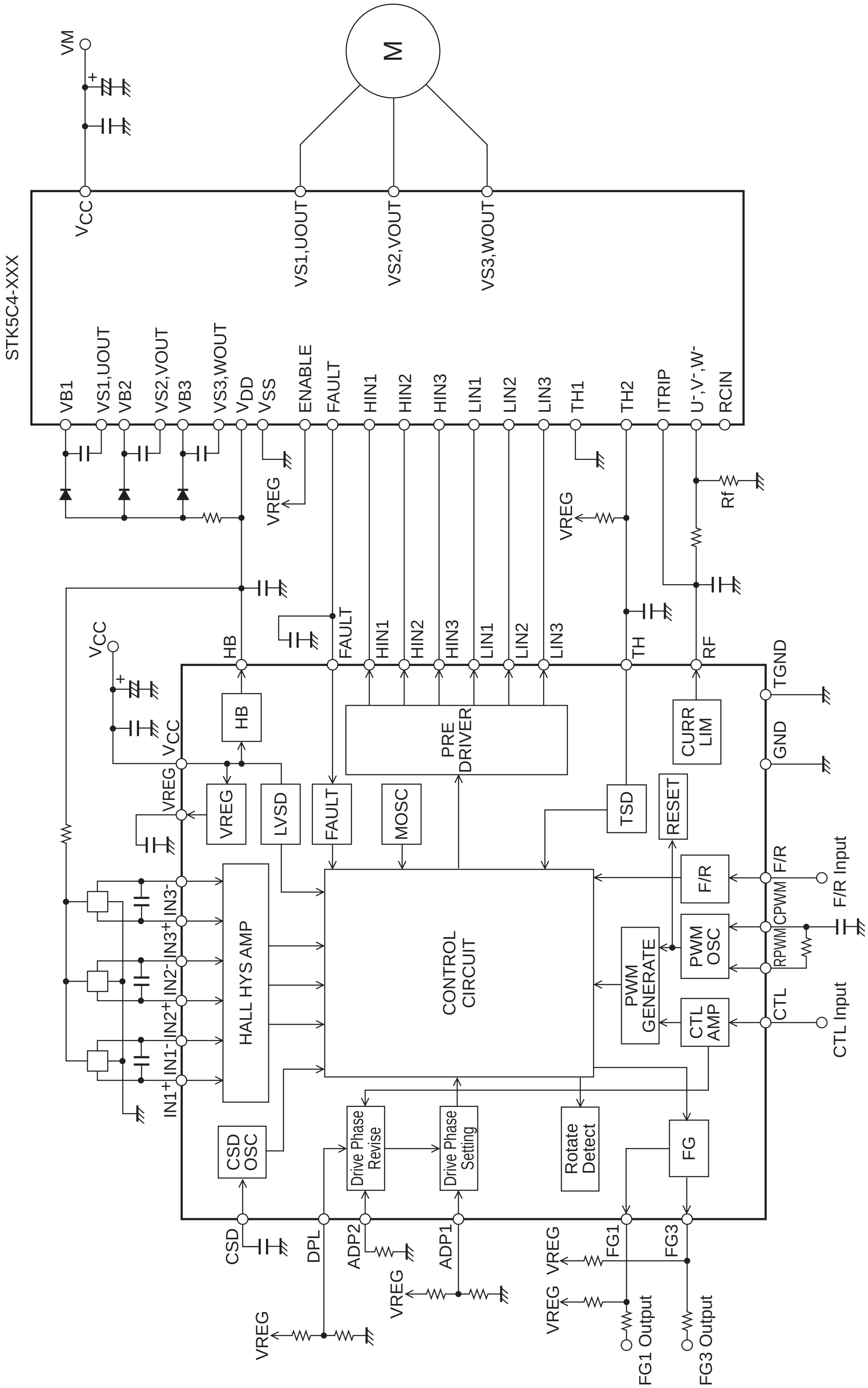


Pin Assignment



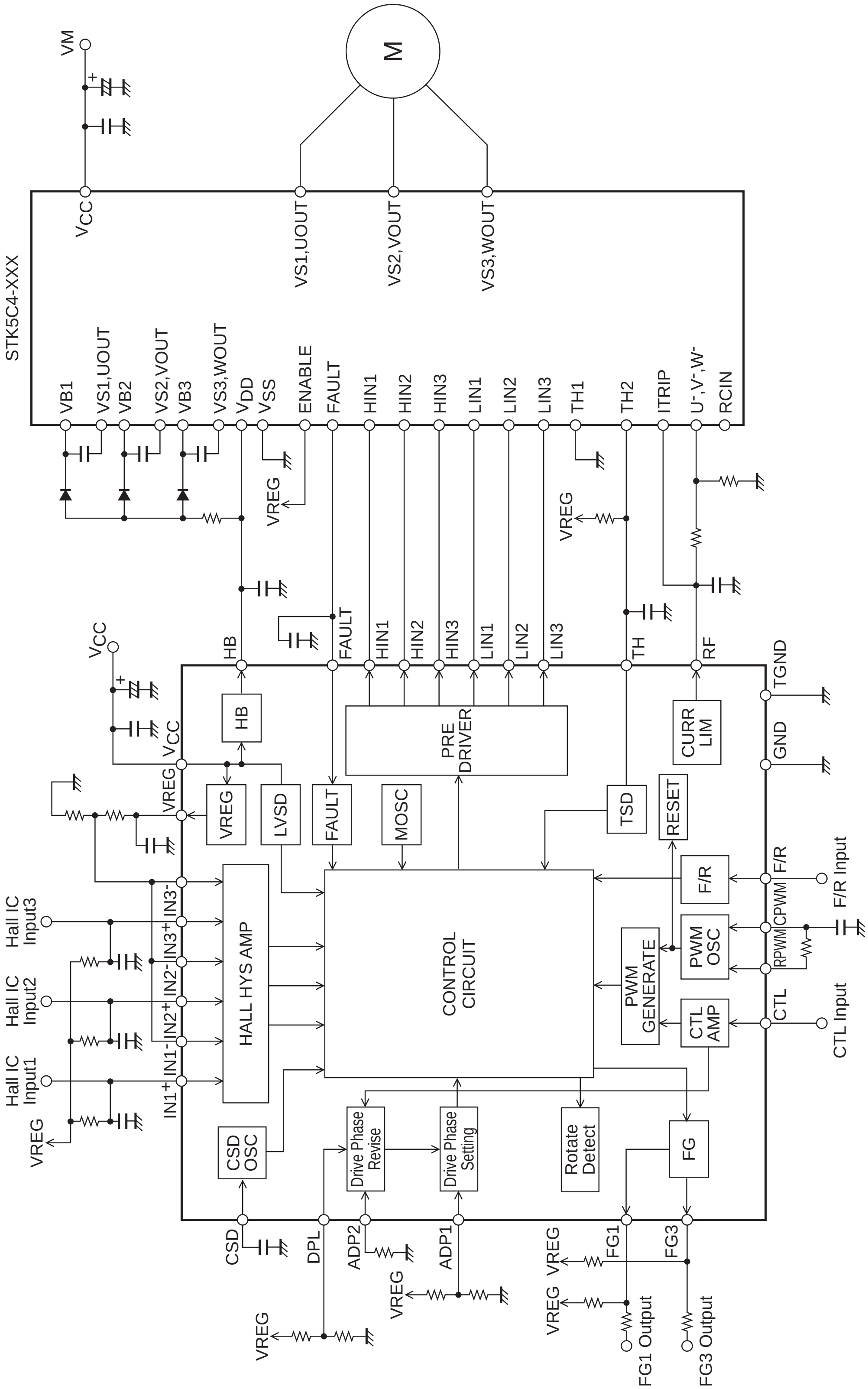
Top view

Sample Application Circuit 1 (Hall element, HIC)

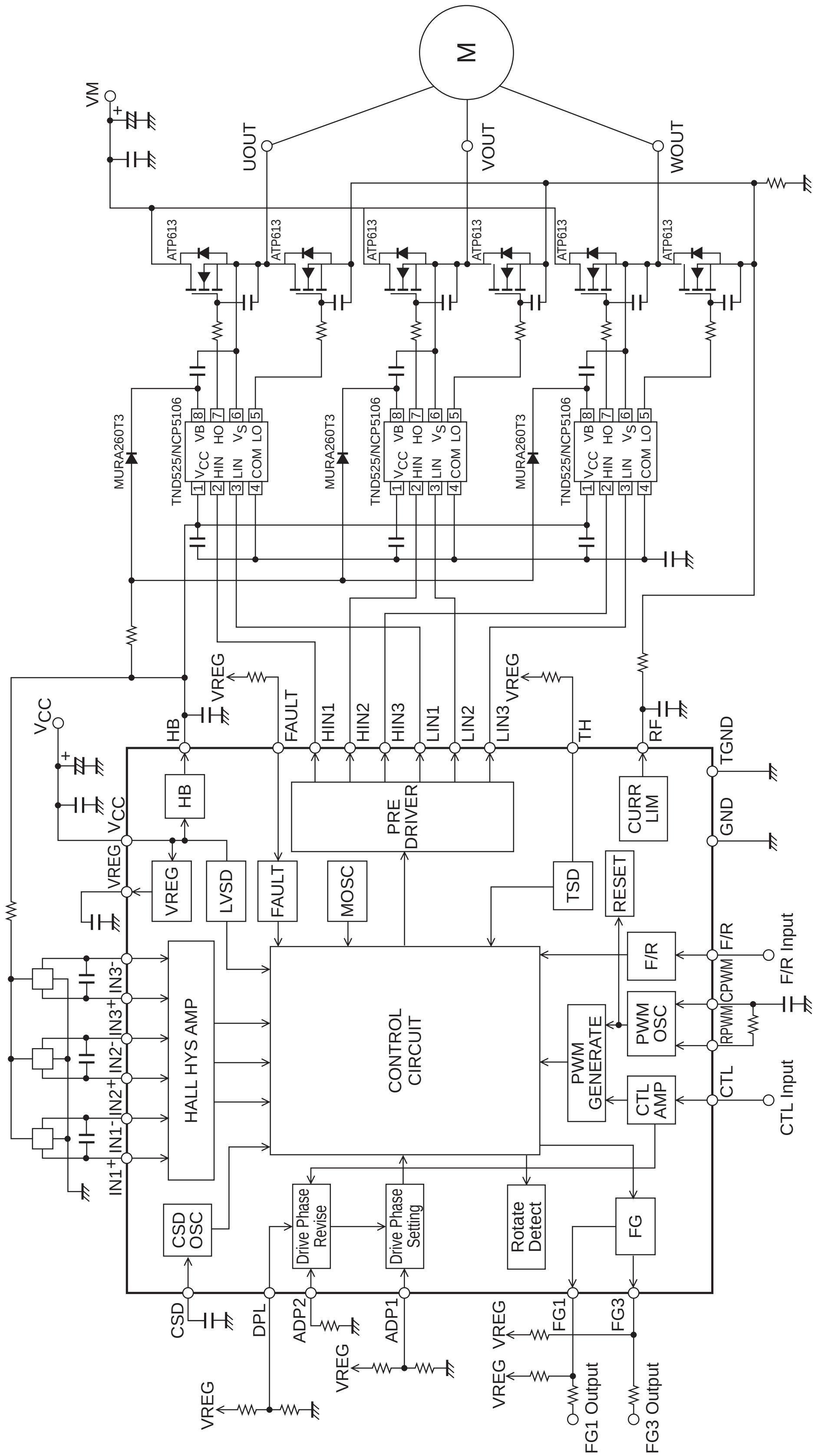


Sample Application Circuit 2 (Hall IC, HIC)

Note : The Hall IC to be used must be of open collector or open drain type (no internal pull-up resistor connected to the output).

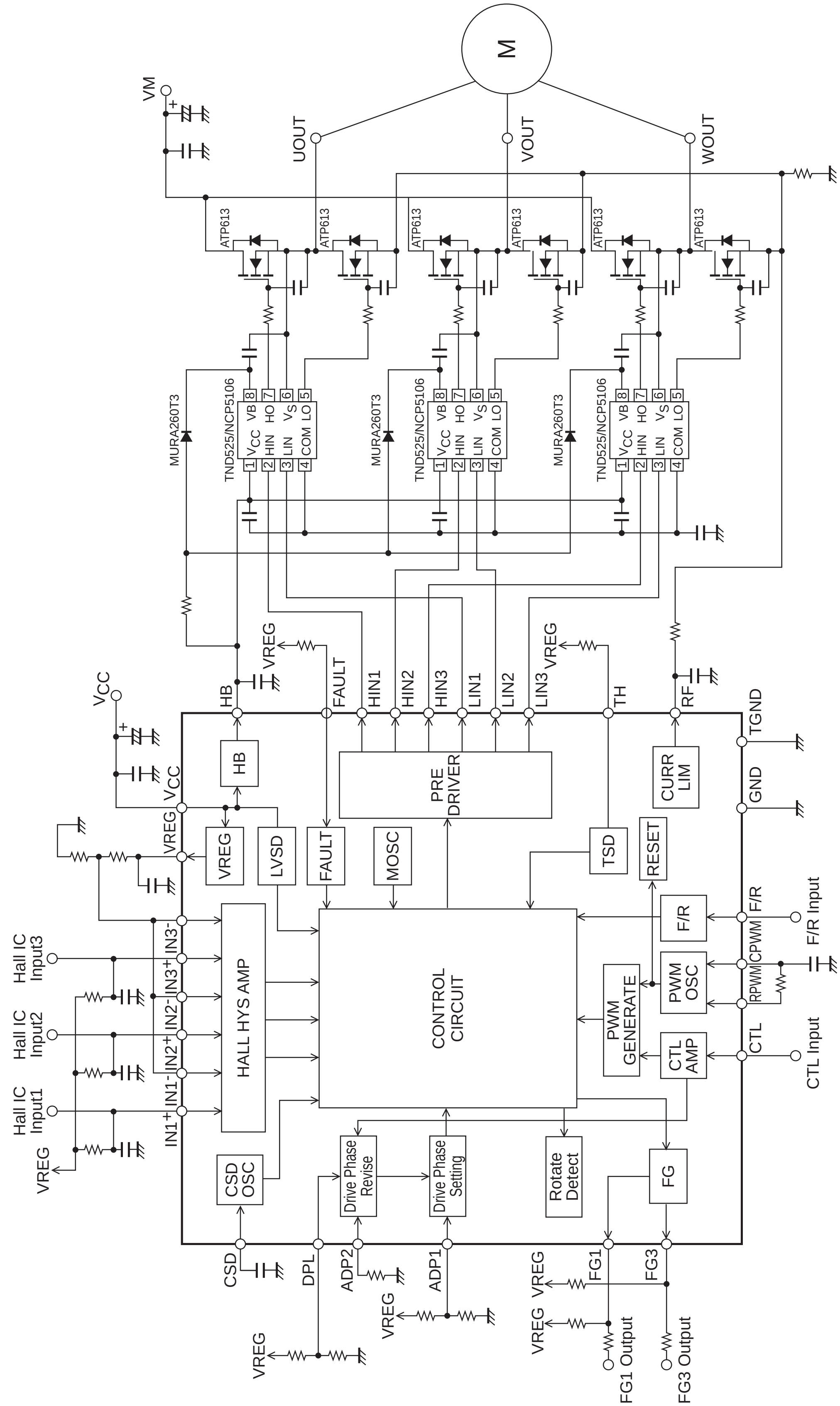


Sample Application Circuit 3 (Hall erement, FET)

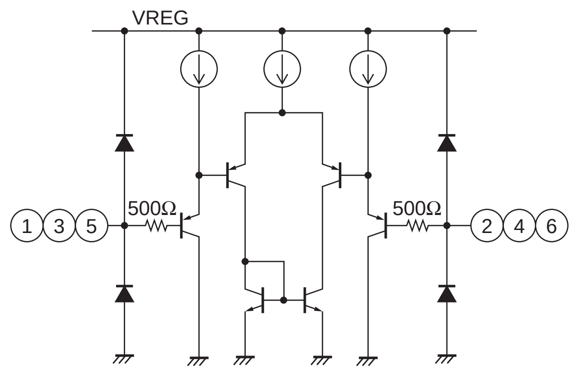
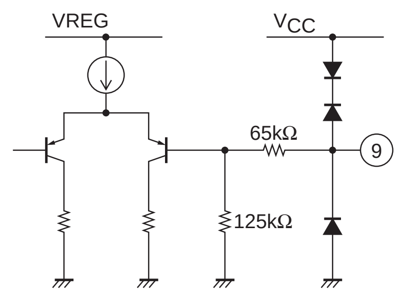
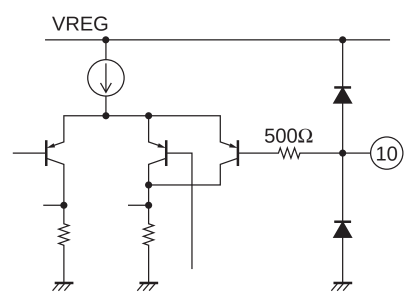
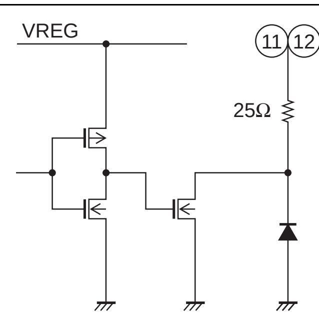


Sample Application Circuit 4 (Hall IC, FET)

Note: The Hall IC to be used must be of open collector or open drain type (no internal pull-up resistor connected to the output).



Pin Functions

Pin No.	Pin Name	Pin function	Equivalent Circuit
1 2 3 4 5 6	$IN1^+$ $IN1^-$ $IN2^+$ $IN2^-$ $IN3^+$ $IN3^-$	Hall signal input pins. The high state is when IN^+ is greater than IN^-, and the low state is the reverse. An amplitude of at least 100mVp-p (differential) is desirable for the Hall signal inputs. If noise on the Hall signals is a problem, insert capacitors between IN^+ and IN^- pins. If input is provided from a Hall IC, the common-mode input range can be expanded by biasing either + or -.	
7	GND	Ground pin of the control circuit block.	
8	V_{CC}	Power supply pin for control. Insert a capacitor between this pin and ground to prevent the influence of noise, etc.	
9	CTL	Control input pin. When CTL pin voltage rises, the IC changes the output signal PWM duty to increase the torque output.	
10	DPL	Setting pin for drive phase adjustment limit. This pin is used to limit the lead angle of the drive phase. The lead angle is limited to zero degrees when the voltage is 1.5V or lower and the limit is released when the voltage is 3.5V or higher.	
11 12	FG3 FG1	FG3 : 3-Hall FG signal output pin. 8-pole motor outputs 12 FG pulses per one rotation. In power saving mode, high-level is output. FG1 :1-Hall FG signal output pin. 8-pole motor outputs 4 pulses per one rotation. In power saving mode, high-level is output.	

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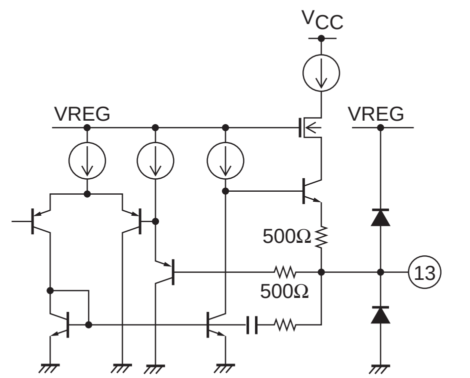
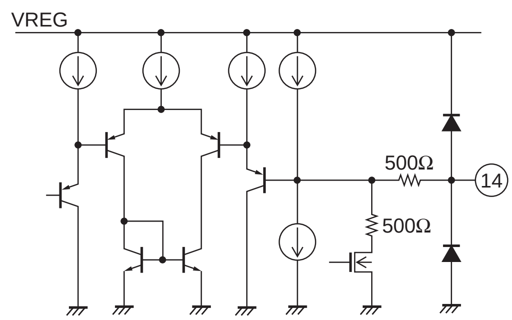
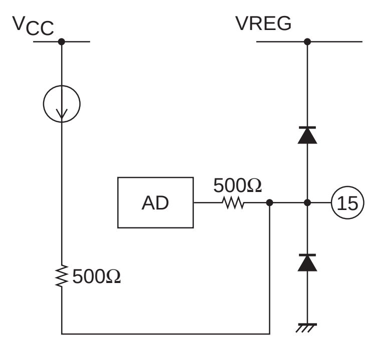
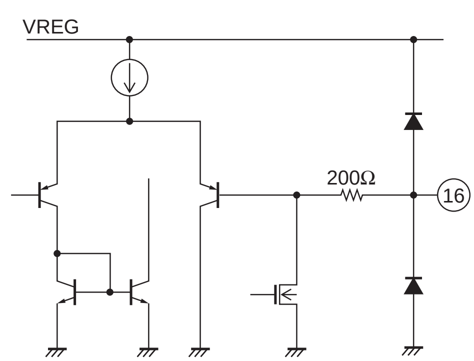
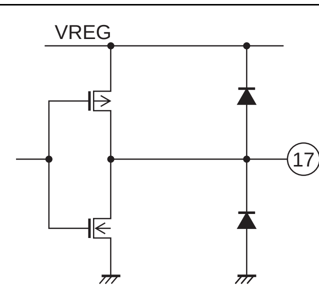
Pin No.	Pin Name	Pin function	Equivalent Circuit
13	ADP2	Setting pin for phase drive correction. This pin sets the amount of correction made to the lead angle according to the CTL input. Insert a resistor between this pin and ground to adjust the amount of correction.	
14	CSD	Pin to set the operating time of the motor constraint protection circuit. Insert a capacitor between this pin and ground. This pin must be connected to ground if the constraint protection circuit is not used.	
15	ADP1	Drive phase adjustment pin. The drive phase can be advanced from 0 to 58 degrees during 180-degree current carrying drive. The lead angle becomes 0 degrees when 0V is input and 58 degrees when 5V is input.	
16	CPWM	Triangle wave oscillation pin for PWM generation. Insert a capacitor between this pin and ground and a resistor between this pin and RPWM for triangle wave oscillation.	
17	RPWM	Oscillation pin for PWM generation. Insert a resistor between this pin and CPWM.	

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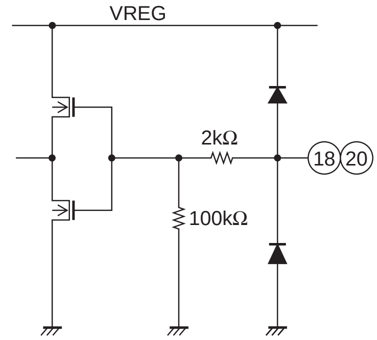
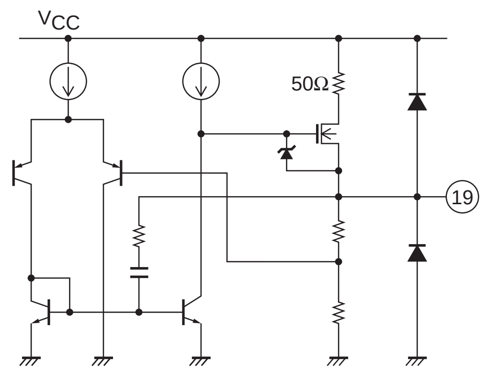
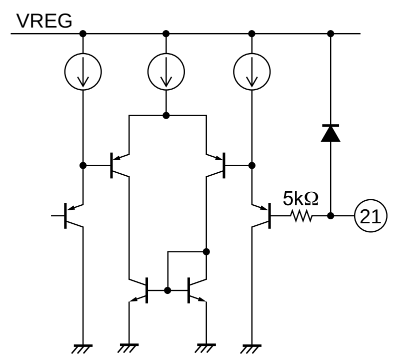
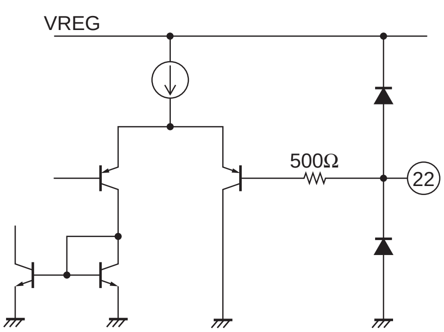
Pin No.	Pin Name	Pin function	Equivalent Circuit
18 20	FR TGND	FR Forward/reverse rotation setting pin. A low-level specifies forward rotation and a high-level specifies reverse rotation. This pin is held low when open. TGND Test pin. Connect this pin to ground.	
19	VREG5	5V regulator output pin (control circuit power supply). Insert a capacitor between this pin and ground for power stabilization. 0.1μF or so is desirable.	
21	RF	Output current detection pin. This pin is used to detect the voltage across the current detection resistor (Rf). The maximum output current is determined by the equation I_{OUT} = 0.25V/Rf.	
22	TH	Thermistor connection pin. The thermistor detects heat generated from HIC and turns off the drive output when an overheat condition occurs. If the pin voltage is 0.6V or lower, the drive output is turned off.	

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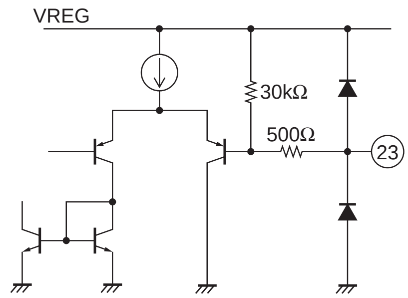
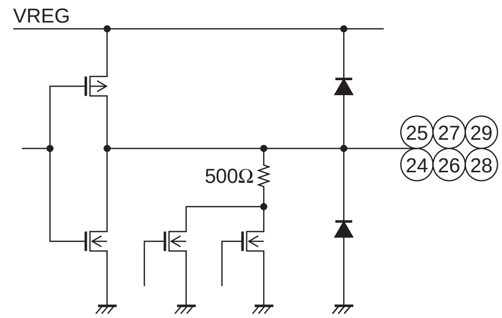
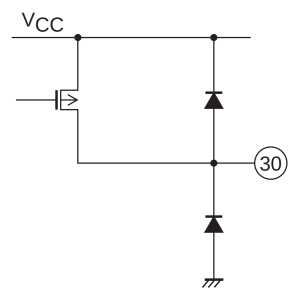
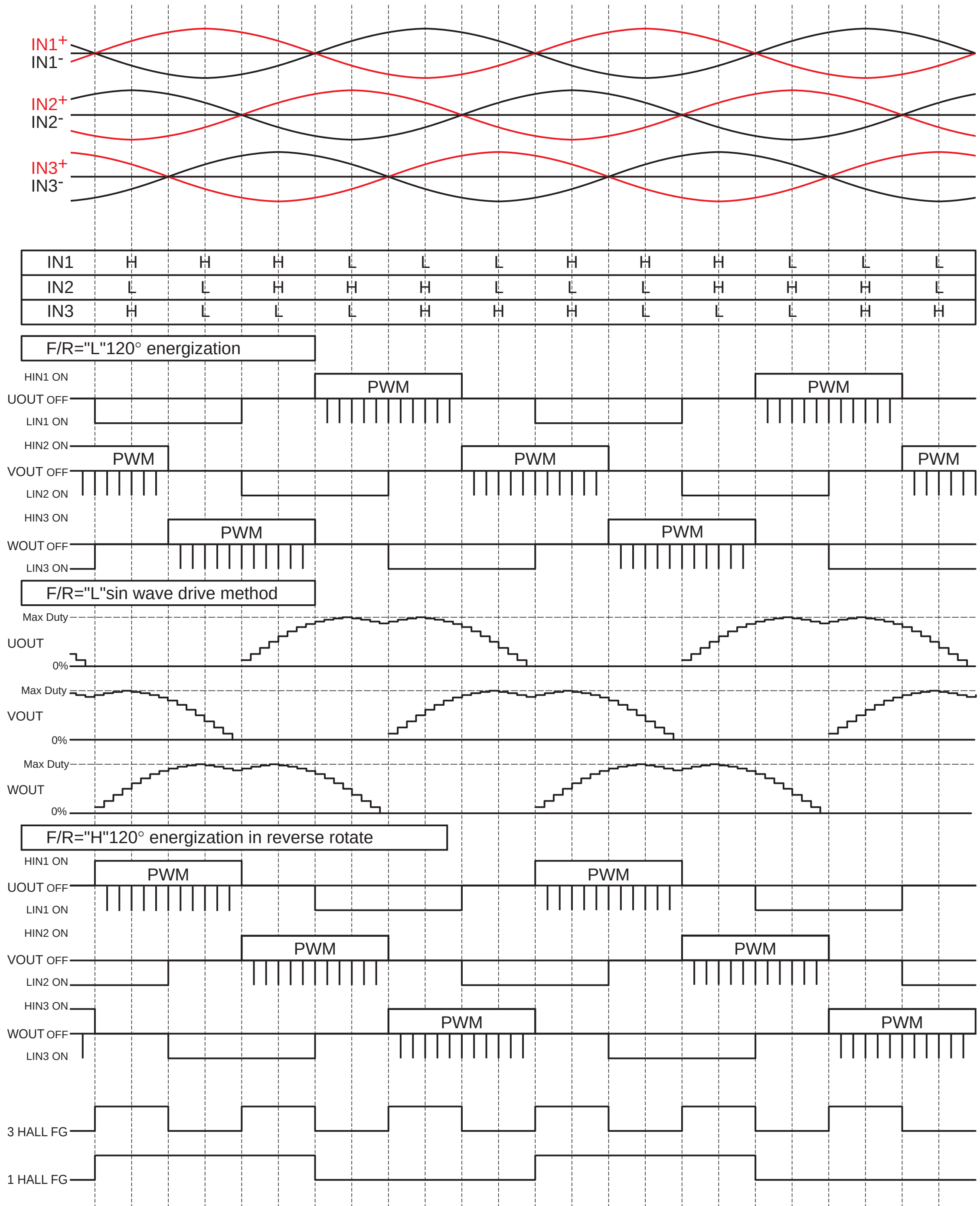
Pin No.	Pin Name	Pin function	Equivalent Circuit
23	FAULT	HIC protection signal input pin. This pin accepts an error mode detection signal generated by the HIC side. A low-level indicates that an error mode is detected and turns off the drive output.	
24 25 26 27 28 29	LIN3 LIN2 LIN1 HIN3 HIN2 HIN1	LIN1, LIN2, and LIN3 : L-side output pins. Generate 0 to VREG5 push-pull outputs. HIN1, HIN2, and HIN3 : H-side output pins. Generate 0 to VREG5 push-pull outputs.	
30	HB	Hall bias HIC power supply pin. Insert a capacitor between this pin and ground. This pin is set to high-impedance state in power saving mode. By supplying Hall bias and HIC power using this pin, the power consumption by Hall bias and HIC in power saving mode can be reduced to zero.	

Timing Chart (IN = "H"indicates the state in which IN+ is greater than IN-.)

(1) F/R pin = L

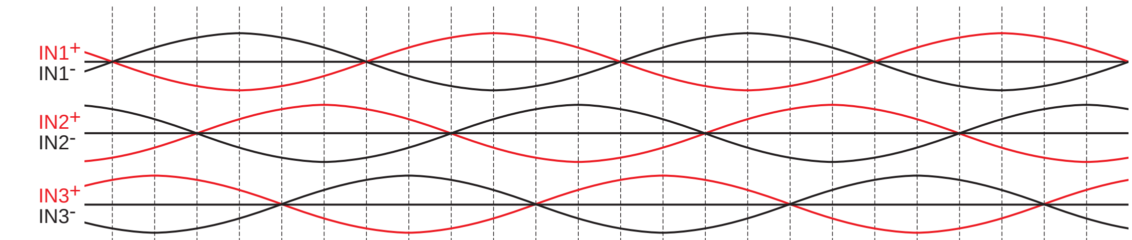
Normal hall input LA=0



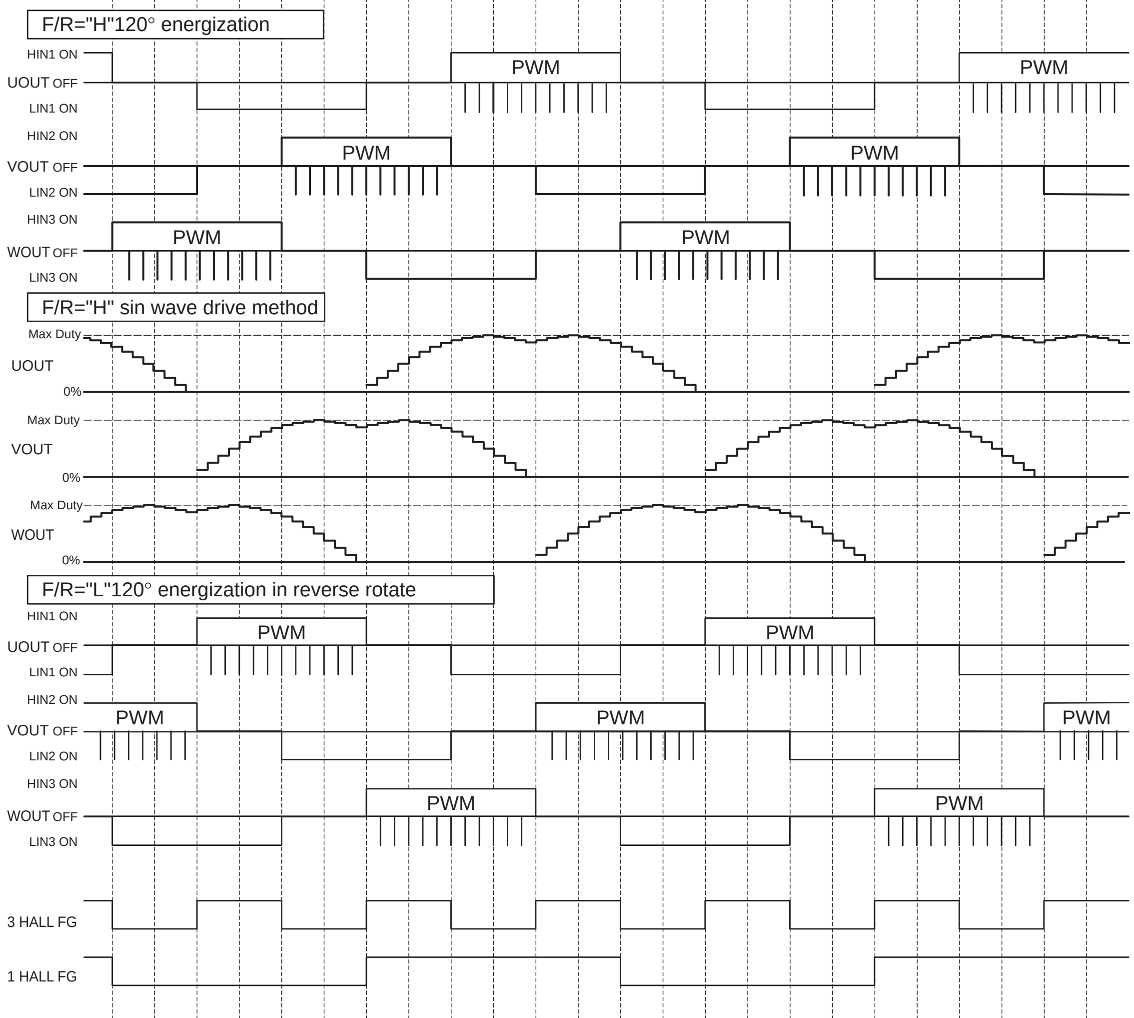
The energization is switched to 120° when 3 Hall FG frequency is 6.1Hz (TYP) or lower
A direction of rotation is detected from Hall signal according to F/R pin input
If the motor rotates in reverse against F/R pin input, 120° energization is maintained forcibly.

(2) F/R pin = H

Reverse hall input LA=0



IN1	L	L	L	H	H	H	L	L	L	H	H	H
IN2	L	H	H	H	L	L	L	H	H	H	L	L
IN3	H	H	L	L	L	H	H	H	L	L	L	H



The energization is switched to 120° when 3 Hall FG frequency is 6.1Hz (TYP) or lower
A direction of rotation is detected from Hall signal according to F/R pin input
If the motor rotates in reverse against F/R pin input, 120° energization is maintained forcibly.

Functional Description

- Basic operation of 120-degree ⇔ 180-degree current-carrying switching

  At startup, this IC starts at 120-degree current-carrying. The current-carrying is switched to 180 degrees when the 3-Hall FG frequency is 6.1Hz (typ) or above and the rising edge of the IN2 signal has been detected twice in succession.

○ Concerning the Hall signal input sequence

This IC controls the motor rotation direction commands and Hall signal input sequence in order to set the lead angle. If the motor rotation direction commands and Hall signal input sequence do not conform to what is shown on the timing chart, the motor is driven by 120-degree current-carrying.

Example 1 : When the Hall signal has been input with the following logic

IN1	H		H		H		L		L		L
IN2	L	→	L	→	H	→	H	→	H	→	L
IN3	H		L		L		L		H		H

When F/R pin input is high → 120-degree current-carrying

When F/R pin input is low → 180-degree current-carrying

Example 2 : When the Hall signal has been input with the following logic

IN1	H		L		L		L		H		H
IN2	L	→	L	→	H	→	H	→	H	→	L
IN3	H		H		H		L		L		L

When F/R pin input is high → 180-degree current-carrying

When F/R pin input is low → 120-degree current-carrying

- CTL pin input

  a) Power-saving mode $V_{CTL} < V_{IL}$ (1.0V : typ)

  When the CTL pin voltage is lower than V_{IL} (1.0V : typ), the IC enters the power-saving mode, and the following are set :

  - $L_{IN}1$ to $L_{IN}3$ and $H_{IN}1$ to $H_{IN}3$ outputs all set to low
  - I_{CC} = 0, HB pin = OFF

  The power consumption of the IC can now be set to 0, and the power consumption of the Hall element connected to the HB pin and the output block can also be set to 0.

  b) Standby mode $V_{IL} < V_{CTL} < V_{IM}$ (2.1V : typ)

  When the CTL pin voltage is $V_{IL} < V_{CTL} < V_{IM}$, the IC enters the standby mode. Low is output for the $U_{IN}1$ to $U_{IN}3$ outputs and bootstrap charge pulses (2µs pulse width: design target) are output to the $L_{IN}1$ to $L_{IN}3$ outputs to prepare for drive start.

  c) Drive mode $V_{IM} < V_{CTL} < V_{IH}$ (5.4V : typ)

  When the CTL pin voltage is $V_{IM} < V_{CTL} < V_{IH}$, the IC enters the drive mode, and the motor is driven at the PWM duty ratio corresponding to V_{CTL}. When V_{CTL} is increased, the PWM duty ratio increases, and the maximum duty ratio is reached at V_{IH}.

  d) Test mode $8V < V_{CTL} < V_{CTL}$ max (design target)

  When the CTL pin voltage is 8V or higher, the IC enters the test mode, and the motor is driven at the 120-degree current-carrying and maximum duty* ratio.

  * When the PWM oscillation frequency setting is 17kHz (*90% : typ).

- The CTL pin is pulled down by 190kΩ : typ inside the IC. Caution is required when the control input voltage input is subjected to resistance division, for example.

- Bootstrap capacitor initial charging mode

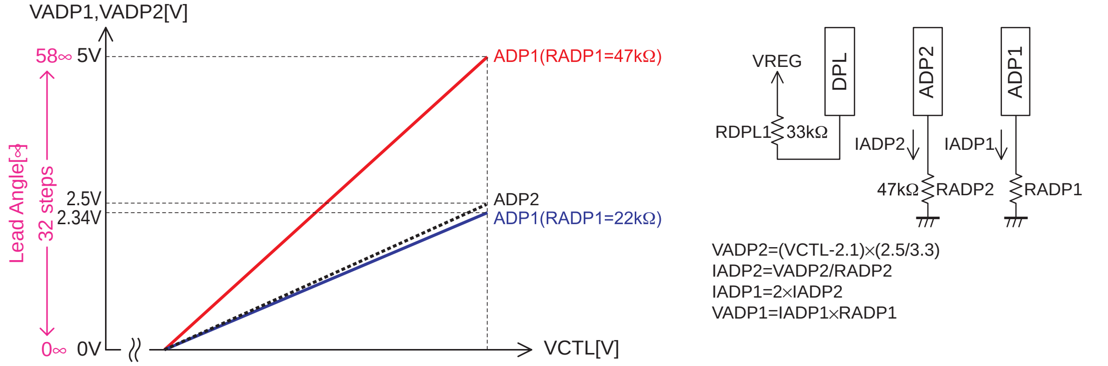
  When the mode is switched from the power-saving mode to the standby mode and then to the drive mode, the IC enters the bootstrap capacitor charging mode (UH, VH, WH pins = L UL, VL, WL pins = H 3.84ms typ) in order to charge the bootstrap capacitor.

- Drive phase adjustment

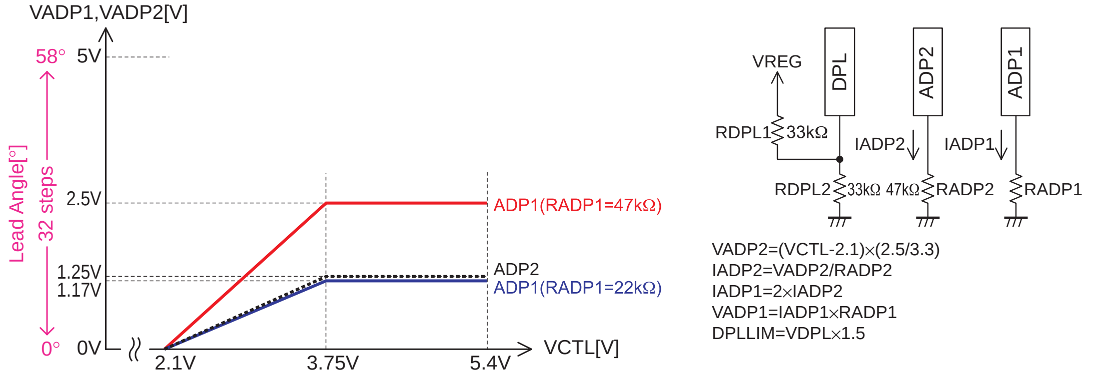
  During 180-degree current-carrying drive, any lead angle from 0 to 58 degrees can be set using the ADP1 pin voltage (lead angle control). This setting can be adjusted in 32 steps (in 1.875-degree increments) from 0 to 58 degrees using the ADP1 pin voltage, and it is updated every Hall signal cycle (it is sampled at the rising edge of the IN3 input and updated at its falling edge).

  A number of lead angle adjustments proportionate to the CTL pin voltage can be undertaken by adjusting the resistance levels of resistors connected to the ADP1 pin, ADP2 pin and DPL pin. When these pins are not going to be used, reference must be made to section 4.5, and the pins must not be used in the open status. Furthermore, a resistance of 47kΩ or more must be used for the resistor (RADP2) that is connected to the ADP2 pin.

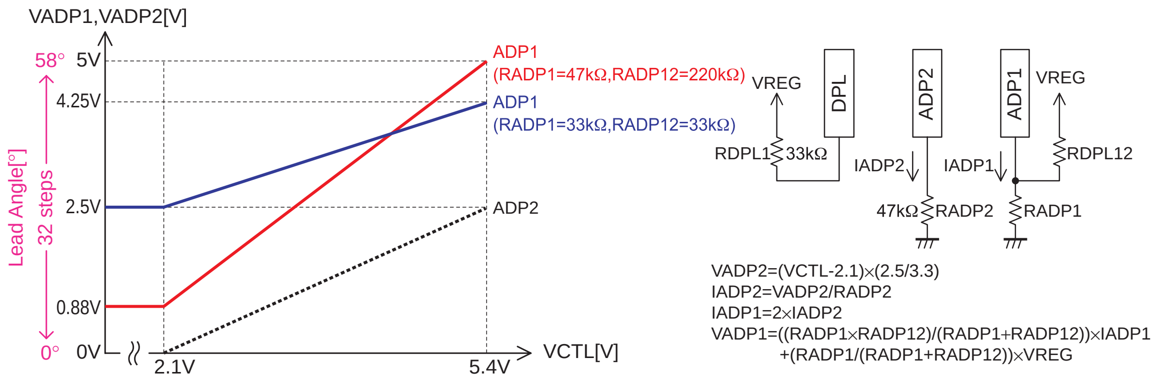
1. The slopes of V_{CTL} and VADP1 can be adjusted by setting the resistance level of the resistor (RADP1) connected to ADP1 (pin 15).



2. The ADP2 pin rise can be halted (a limit on the lead angle adjustment can be set by means of the CTL voltage) by setting DPL (pin 10).



3. The offset and slope can be adjusted as desired by setting RADP1 and RADP12 of ADP1 (pin 15). (It is also possible to set a limit on the lead angle adjustment by means of the CTL voltage by setting DPL.)



4. When the lead angle is not adjusted

   ADP1 pin: shorted to ground; ADP2 pin and DPL pin: pulled down to ground using the resistors

5. When the lead angle is not adjusted by means of the CTL pin voltage (for use with a fixed lead angle)

   ADP1 pin: lead angle setting by resistance division from VREG; ADP2 pin and DPL pin: pulled down to ground by the resistors

Description of LV8138V

1. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation $I = V_{RF}/Rf$ (where V_{RF} = 0.25V typ, Rf is the value of the current detection resistor). The current limiter operates by reducing the output on duty to suppress the current.

The current limiter circuit detects the reverse recovery current of the diode due to PWM operation. To assure that the current limiting function does not malfunction, its operation has a delay of approx. 1μs. If the motor coils have a low resistance or a low inductance, current fluctuation at startup (when there is no back electromotive force in the motor) will be rapid. The delay in this circuit means that at such times the current limiter circuit may operate at a point well above the set current. Application must take this increase in the current due to the delay into account when the current limiter value is set.

2. Power Saving Circuit (CTL pin)

This IC goes into the power saving mode that stops operation of all the circuits to reduce the power consumption. If the HB pin is used for the Hall element bias and the output block, the current consumption in the power-saving mode is zero.

3. Hall Input Signal

Signals with an amplitude in excess of the hysteresis is required for the Hall inputs. However, considering the influence of noise and phase displacement, an amplitude of over 100mV is desirable.

If noise disrupts the output waveform (at phase change), this must be prevented by inserting capacitors or other devices across the Hall inputs. The constraint protection circuit uses the Hall inputs to discriminate the motor constraint state. Although the circuit is designed to tolerate a certain amount of noise, care is required.

If all three phases of the Hall input signal go to the same input state (HHH or LLL), the outputs are all set to the off state.

If the outputs from a Hall IC are used, fixing one side of the inputs (either the + or –side) at a voltage within the common-mode input voltage range (0.3V to VREG-1.7V) allows the other input side to be used as an input over the 0V to VREG range.

4. Constraint Protection Circuit

This IC goes into the power saving mode that stops operation of all the circuits to reduce the power consumption. If the HB pin is used for the Hall element bias and the output block, the current consumption in the power-saving mode is zero.

This IC provides an on-chip constraint protection circuit to protect the IC itself and the motor when the motor is constrained.

If the Hall input signals do not change for over a fixed period when the motor is in operation, this circuit operates. Also, the upper-side output transistor is turned off while the constraint protection circuit is operating. This time is determined by the capacitance of the capacitor connected to the CSD pin.

$$\text{Set time (in seconds)} \approx 90 \times C\ (\mu F)$$

If a 0.022μF capacitor is used, the protection time will be about 2.0 seconds.

The set time must be selected to have an adequate margin with respect to the motor startup time

Conditions to clear the constraint protection state :

CTL pin when a low-level voltage is input → Release protection and reset count

When TSD protection is detected → Stop count

5. Power Supply Stabilization

Since this IC adopts a switching drive technique, the power-supply line level can be disrupted easily. Thus capacitors large enough to stabilize the power supply voltage must be inserted between the V_{CC} pins and ground. If the electrolytic capacitors cannot be connected close to their corresponding pins, ceramic capacitors of about 0.1μF must be connected near these pins.

If diodes are inserted in the power-supply line to prevent destruction of the device when the power supply is connected with reverse polarity, the power supply line levels will be even more easily disrupted, and even larger capacitors must be used.

6. VREG Stabilization
A capacitor of at least 0.1μF must be used to stabilize the VREG voltage, which is the control circuit power supply. The ground lead of that capacitor must be located as close as possible to the control system ground (SGND) of the IC.

7. Forward/Reverse Switching (F/R pin)
Switching between forward rotation and reverse rotation must not be undertaken while the motor is running.

8. TH Pin
The TH pin must normally be pulled up to the 5V regulator for use. When it has been set to low, the outputs are low.

9. FAULT Pin
The FAULT pin must normally be pulled up to the 5V regulator for use. When it has been set to low, the outputs are low. In addition, the FG output does OFF, too

10. PWM Frequency Setting

$$fCPWM \approx 1/(1.78CR)$$

Components with good temperature characteristics must be used.
An oscillation frequency of about 17kHz is obtained when a 2200pF capacitor and 15kΩ resistor are used. If the PWM frequency is too low, switching noise will be heard from the motor; conversely, if it is too high, the output power loss will increase. For this reason, a frequency between 15kHz and 30kHz or so is desirable. The capacitor ground must be connected as close as possible to the control system ground (SGND pin) of the IC to minimize the effects of the outputs.

This catalog provides information as of February, 2012. Specifications and information herein are subject to change without notice.