

RELIABILITY REPORT
FOR
MAX3283EAUT
PLASTIC ENCAPSULATED DEVICES

February 14, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3283E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3283E is a single receiver designed for RS-485 and RS-422 communication. This device's guarantee data rates up to 52Mbps, even with a 3V power supply. Excellent propagation delay (15ns max) and package-to-package skew time (8ns max) make this device ideal for multidrop clock distribution applications.

The MAX3283E has true fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are opened or shorted. The receiver output will be a logic high if all transmitters on a terminated bus are disabled (high impedance). This device features 1/4-unit-load receiver input impedance, allowing up to 128 receivers on the same bus.

The MAX3283E single receivers have a receiver enable (EN or EN-bar) function and are offered in a 6-pin SOT23 package.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
(All Voltages Referenced to GND)	
Supply Voltage (VCC)	-0.3V to +6V
Control Input Voltage (EN, EN)	-0.3V to +6V
VL Input Voltage	-0.3V to +6V
Receiver Input Voltage (A, B)	-7.5V to +12.5V
Receiver Output Voltage (RO)	-0.3V to (VCC + 0.3V)
Receiver Output Short-Circuit Current	Continuous
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
6-Pin SOT23	696mW
Derates above +70°C	
6-Pin SOT23	8.7mW/°C

II. Manufacturing Information

- A. Description/Function: $\pm 15\text{kV}$ ESD-Protected 52Mbps, 3V to 5.5V, RS-485/RS-422 True Fail-Safe Receivers
- B. Process: S8 - Standard 8 micron silicon gate CMOS
- C. Number of Device Transistors: 233
- D. Fabrication Location: California, USA
- E. Assembly Location: Malaysia or Thailand
- F. Date of Initial Production: January, 2002

III. Packaging Information

- A. Package Type: **6-Lead SOT23**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Silver-Filled Epoxy
- E. Bondwire: Gold (1.0 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: Buildsheet # 05-9000-0327
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

- A. Dimensions: 43 X 35 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: TiW/ AlCu/ TiWN
- D. Backside Metallization: None
- E. Minimum Metal Width: .8 microns (as drawn)
- F. Minimum Metal Spacing: .8 microns (as drawn)
- G. Bondpad Dimensions: 2.7 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 240 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 4.52 \times 10^{-9} \quad \lambda = 4.52 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-5867) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at <http://www.maxim-ic.com>.

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RT33-3 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Additionally, the MAX3283E has achieved $\pm 15\text{kV}$ ESD protection using both methods 3015 and IEC 801-2 (air-gap discharge) on the I/O pins. Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$ and/or $\pm 20\text{V}$.

Table 1
Reliability Evaluation Test Results

MAX3283EAUT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	240	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

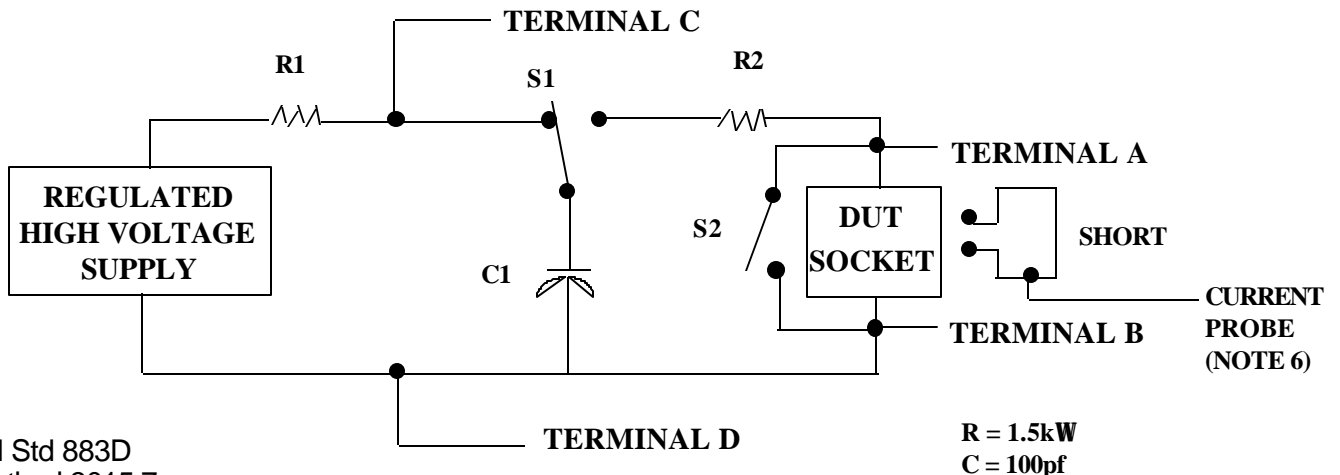
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

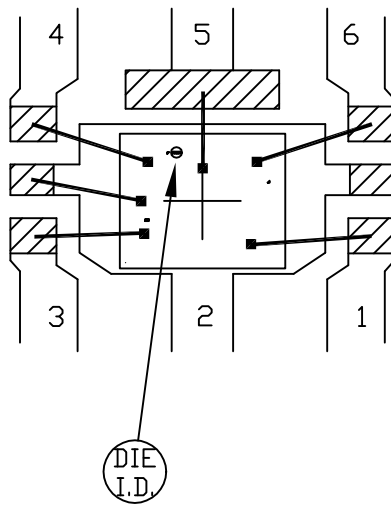
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



NOTE: CAVITY DOWN

PKG. CODE: U6-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 64x39	PKG. DESIGN			BOND DIAGRAM #: 05-9000-0327	REV: A

