VOICE OTP IC

aP8821 – 21" VOICE OTP

APLUS INTEGRATED CIRCUITS INC.

Address:
3 F-10, No. 32, Sec. 1, Chenggung Rd., Taipei,
Taiwan 115, R.O.C.
(115)台北市南港區成功路一段 32 號 3 樓之 10.

TEL: 886-2-2782-9266

FAX: 886-2-2782-9255

WEBSITE : http: //www.aplusinc.com.tw

Sales E-mail:
sales@aplusinc.com.tw

Technology E-mail:
service@aplusinc.com.tw

21 sec VOICE OTP

Features

- 21 Sec Voice Length at 6 KHz
- Combination of voice building blocks extends the duration of playback
- Voice data re-use saves memory space
- Maximum 14 voice groups
- 4 trigger pins, S1 to S4 for the 4 voice groups (group1 ~ 4)
- SBT for sequential playblack for the rest of voice groups & CPU mode trigger
- CPU trigger mode for all 14 voice groups
- Holdable, Unholdable, Edge, Level triggering option
- Debounce time : 21ms (Key mode) / 85us (CPU mode) - 6K sampling rate
- IRP interrupt pin for master reset
- 3 programmable Outputs for STP stop pulse, BUSY and LED
- Built-in oscillator with a single external resistor to determine the sampling rate
- Built-in D/A converter, EPROM
- ADPCM data compression provides high sound quality
- Optional POP noise elimination function
- C_{OUT} pin drives speaker with a transistor
- V_{OUT1} and V_{OUT2} drives buzzer or speaker directly
- Auto-power down
- 2.4V – 4.8V single power supply operation
- Low standby current (<5uA at 3V)
- Development Tools Support

General Description

***a*P8821** is a high quality voice synthesizer capable of varying playback duration. A proprietary ADPCM algorithm is used. The audio message is stored in a 512K bits on-chip EPROM which can store up to 21 seconds of voice data at 6 KHz sample rate.

The ***a*P8821** eliminates the need of complicated circuitry in voice playback but still achieves high voice quality for different kind of sounds. Combinations in sections achieve longer playback duration.

A pair of PWM output pins, V_{OUT1} and V_{OUT2} provides direct drive to buzzer or speaker.

A current output pin, C_{OUT}, enables the device to drive a speaker through a low cost NPN transistor. No complex filtering or amplifier circuit is needed. An automatic ramp-down function eliminates undesired noise at the end of playback.

Group of sections

The voice memory of the **aP8821** can be subdivided into 126 memory blocks. Any combination of playback of these memory blocks will form an individual voice group. A maximum of 14 groups are available with triggering S1 to S4 pins together with the SBT pin sequential playback pin.

Group Configuration

Data within each group are combinations of different fixed memory blocks of up to 126 blocks. They are the fundamental building blocks for arranging playback without limiting sequencing. This provides flexibility and allows data to be re-used, beneficial for applications with many repeated sounds or words.

An example of group configuration is illustrated below:

Group no.	Section entry
Group 1	Block 1 + Block 2 + Block 3 ……. Block 109
Group 2	Block 3 + Block 2
Group 3	Block 10 + Block 11 + Block 12
Group 4	Block 10 + Block 10 + Block 5

The entries of blocks for each group is truly random and without limitation. However, there is a limit in the total number of entries for 14 voice groups, which is 960 entries in **aP8821**. It is acceptable to allocate all entries into only one group or distribute out to other groups. It depends on how many groups of messages are required.

Programmable Options

Each groups in **aP8821** can have independent options. They include:

- Edge or Level trigger
- Unholdable or Holdable trigger
- Re-triggerable or non-retriggerable
- Outputs are programmable to LED1, LED2, BUSY and STOP pulse

Options that affect all voice groups are called whole chip options. They include:

- Key trigger mode or CPU trigger mode
- Ramp enable or Ramp disable

Output Selections

There are three independent output pins OUT1, OUT2 and OUT3, available for four combinations of LED1, LED2, STOP and BUSY signals for each voice group.

	OUT1	OUT2	OUT3
1.	LED2	LED1	BUSY
2.	STOP	LED1	LED2
3.	LED1	BUSY	STOP
4.	LED1	BUSY	/BUSY

LED1 and LED2 are complemented outputs flashing at a fix interval. STOP pulse gives a long enough positive pulse at the end of the playback for each group with option to enable or disable it.

BUSY is active high depends on voice Block setting. That means BUSY signal can be set to high when some voice Blocks are being played but set to low for the others.

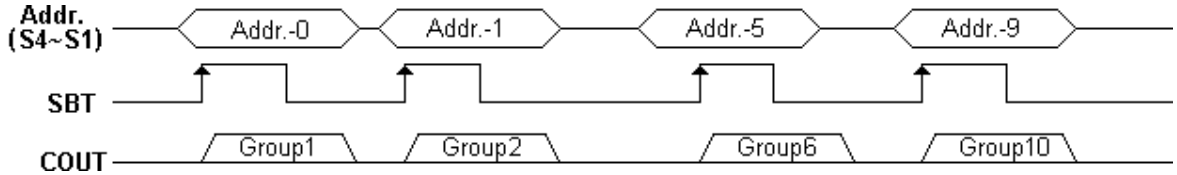
Software Support

All those Options and Output selections can be set with a dedicated OTP compiler and programmer software supplied by APLUS.

Key trigger mode and CPU trigger mode

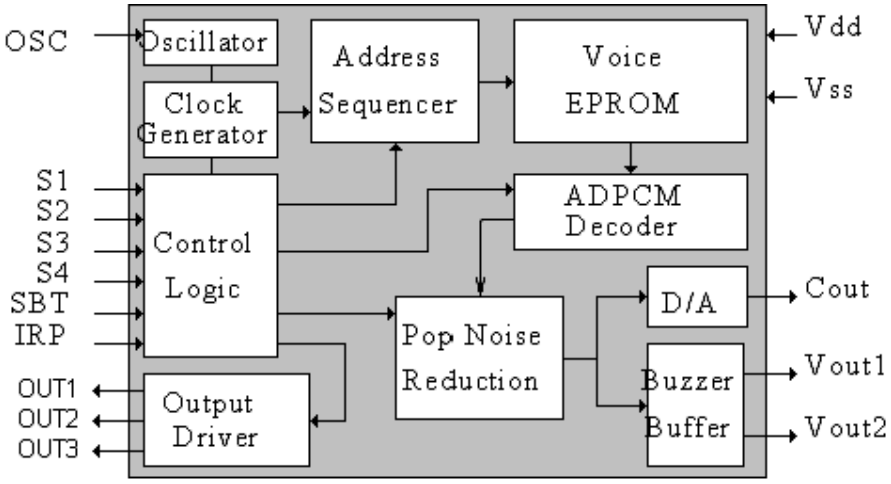
In Key trigger mode, S1 to S4 will trigger four voice groups. The rest of the voice groups can only be triggered by SBT sequential trigger pin.

In CPU trigger mode, binary data is input to S4~S1. A high pulse is input to SBT pin with pulse width equal to or longer than the debounce time to strobe the data to initial the playblack. Data patterns “1110” and “1111” is not allowed.



Group-n	S4	S3	S2	S1	Group-n	S4	S3	S2	S1
Group1	0	0	0	0	Group9	1	0	0	0
Group2	0	0	0	1	Group10	1	0	0	1
Group3	0	0	1	0	Group11	1	0	1	0
Group4	0	0	1	1	Group12	1	0	1	1
Group5	0	1	0	0	Group13	1	1	0	0
Group6	0	1	0	1	Group14	1	1	0	1
Group7	0	1	1	0	X	1	1	1	0
Group8	0	1	1	1	X	1	1	1	1

■ Block Diagram



■ Absolute Maximum Rating

Symbol	Rating	Unit
V_{DD} - V_{SS}	-0.5 ~ +5.0	V
V_{IN}	V_{SS} - 0.3<V_{IN}<V_{DD} + 0.3	V
V_{OUT}	V_{SS} <V_{OUT}<V_{DD}	V
T (Operating)	-10 ~ +60	℃
T (Storage)	-55 ~ +125	℃

■ Pin Description

Pin No.	Name	I/O/P	Function
1	OUT3	O	Programmable output 3
2	V_{OUT1}	O	PWM audio signal output 1 for buzzer & speaker
3	V_{OUT2}	O	PWM audio signal output 2 for buzzer & speaker
4	V_{SS}	P	Power ground
5	OUT1	O	Programmable output 1
6	OUT2	O	Programmable output 2
7	C_{OUT}	O	Current output from internal DAC for speaker playback
8	OSC	I	Oscillator resistor pin to control sampling frequency
9	VPP	P	Program power, must connect to VDD when playback
10	S1	I	Trigger switch 1 / CPU Addr.1(LSB), internal pull low, active high
11	S2	I	Trigger switch 2 / CPU Addr.2, internal pull low, active high
12	V_{DD}	P	Positive power supply
13	S3	I	Trigger switch 3 / CPU Addr.3, internal pull low, active high
14	S4	I	Trigger switch 4 / CPU Addr.4 (MSB), internal pull low, active high
15	SBT	I	Key Sequential/CPU trigger, internal pull low, active high
16	IRP	I	Interrupt to stop playback, internal pull low, active high

Note: The following pins are used to program data into the memory:
pin 4, 5, 6, 8, 9, 12,15 and16.

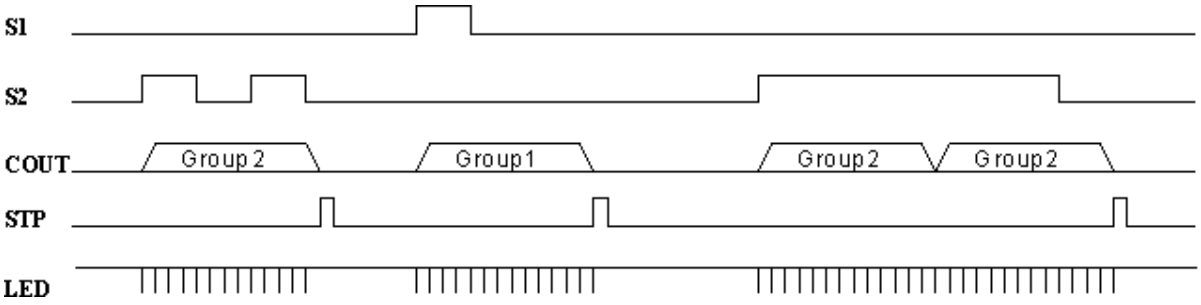
■ DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	2.4	3.0	4.8	V	
I_{SB}	Standby current	—	1	5	μA	V_{DD}=3.0V, I/O open
I_{OP}	Operating current	—	—	15	mA	V_{DD}=3.0V, I/O open
V_{IH}	"H" Input Voltage	2.5	3.0	3.5	V	V_{DD}=3.0V
V_{IL}	"L" Input Voltage	-0.3	0	0.5	V	V_{DD}=3.0V
I_{OH}	V_{OUT} low O/P Current	—	70	—	mA	V_{DD}=3.0V, Vout=0.3V
I_{OL}	V_{OUT} high O/P Current	—	-40	—	mA	V_{DD}=3.0V, Vout=2.5V
I_{CO}	C_{OUT} O/P Current	—	-3	—	mA	V_{DD}=3.0V,V_{COUT}=1.0V
I_{OH}	O/P high Current	—	-8	—	mA	V_{DD}=3.0V, V_{OH}=2.5V
I_{OL}	O/P low Current	—	8	—	mA	V_{DD}=3.0V, V_{OL}=0.3V
ΔF/F	Frequency Stability	-5	—	+5	%	$\frac{Fosc(2.7V) - Fosc(3.4V)}{Fosc(3V)}$

■ Timing Diagram

1. Level, Unholdable, Non-retriggerable

a. Trigger is shorter than a Group output



b. Trigger is longer than a Group output

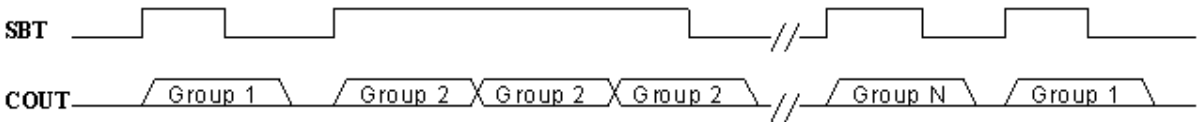
2. Level Holdable

a. Trigger is shorter than a Group output

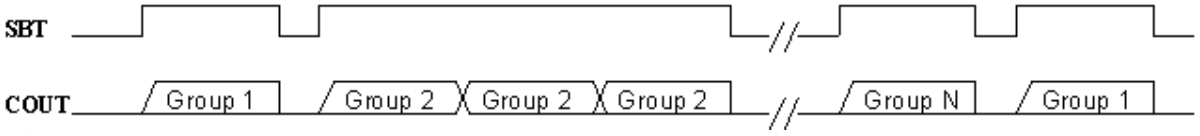
b. Trigger is longer than a Group output

3. Single Button Trigger(SBT), Sequential

a. Level Unholdable



b. Level Holdable

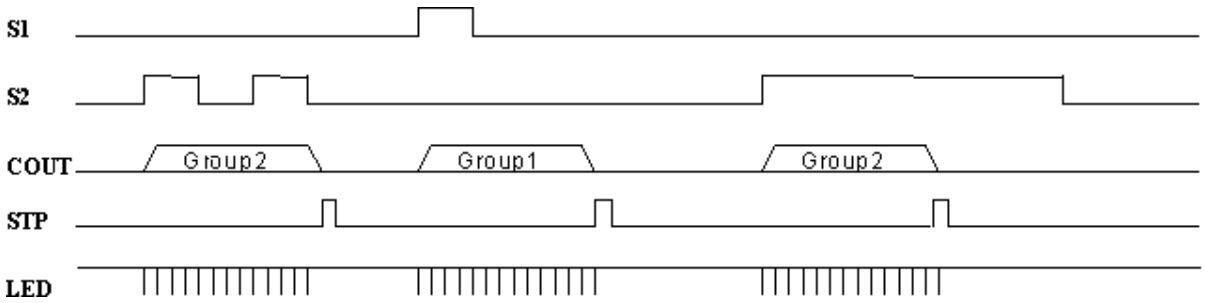


where N is up to 14.

4. Edge, Unholdable, Non-retriggerable

a. Trigger is shorter than a Group output

b. Trigger is longer than a Group output



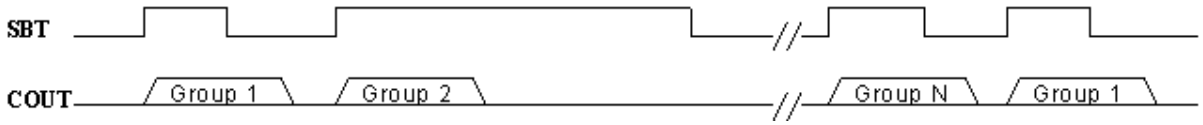
5. Edge Holdable

a. Trigger is shorter than a Group output

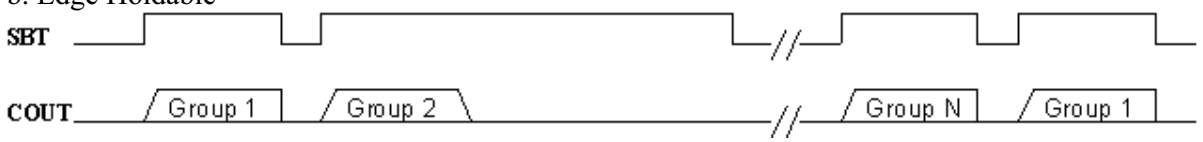
b. Trigger is longer than a Group output

6. Single Button Trigger(SBT), Sequential

a. Edge Unholdable



b. Edge Holdable



where N is up to 14.

■ Application Circuits

1. Typical Application

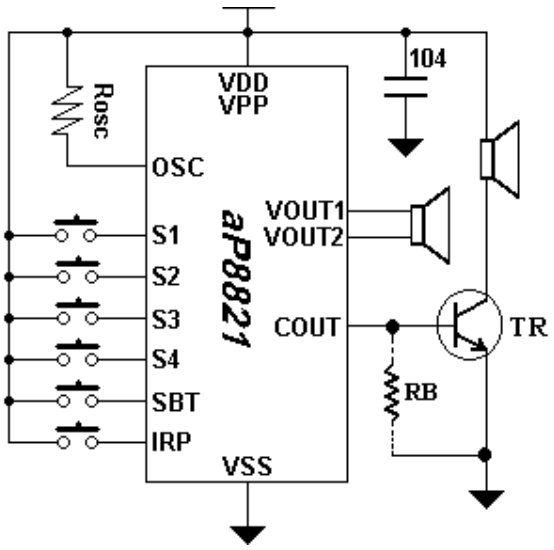


Fig. 1 a

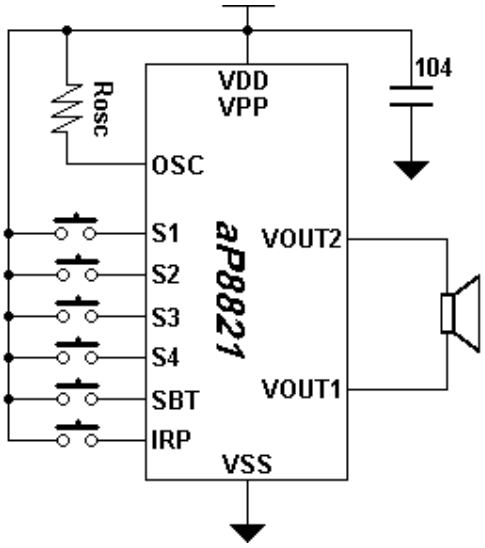
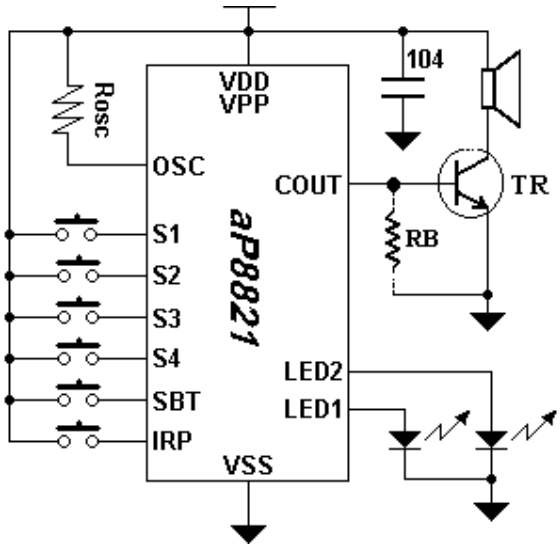


Fig. 1 b

2. LED Application



3. CPU Mode control

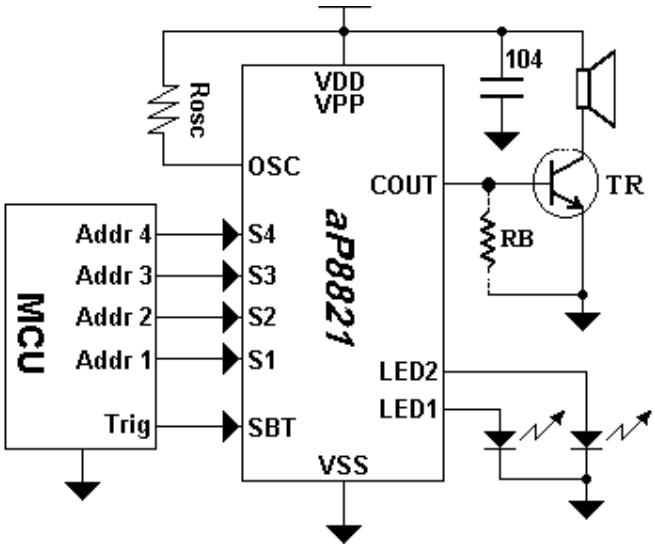
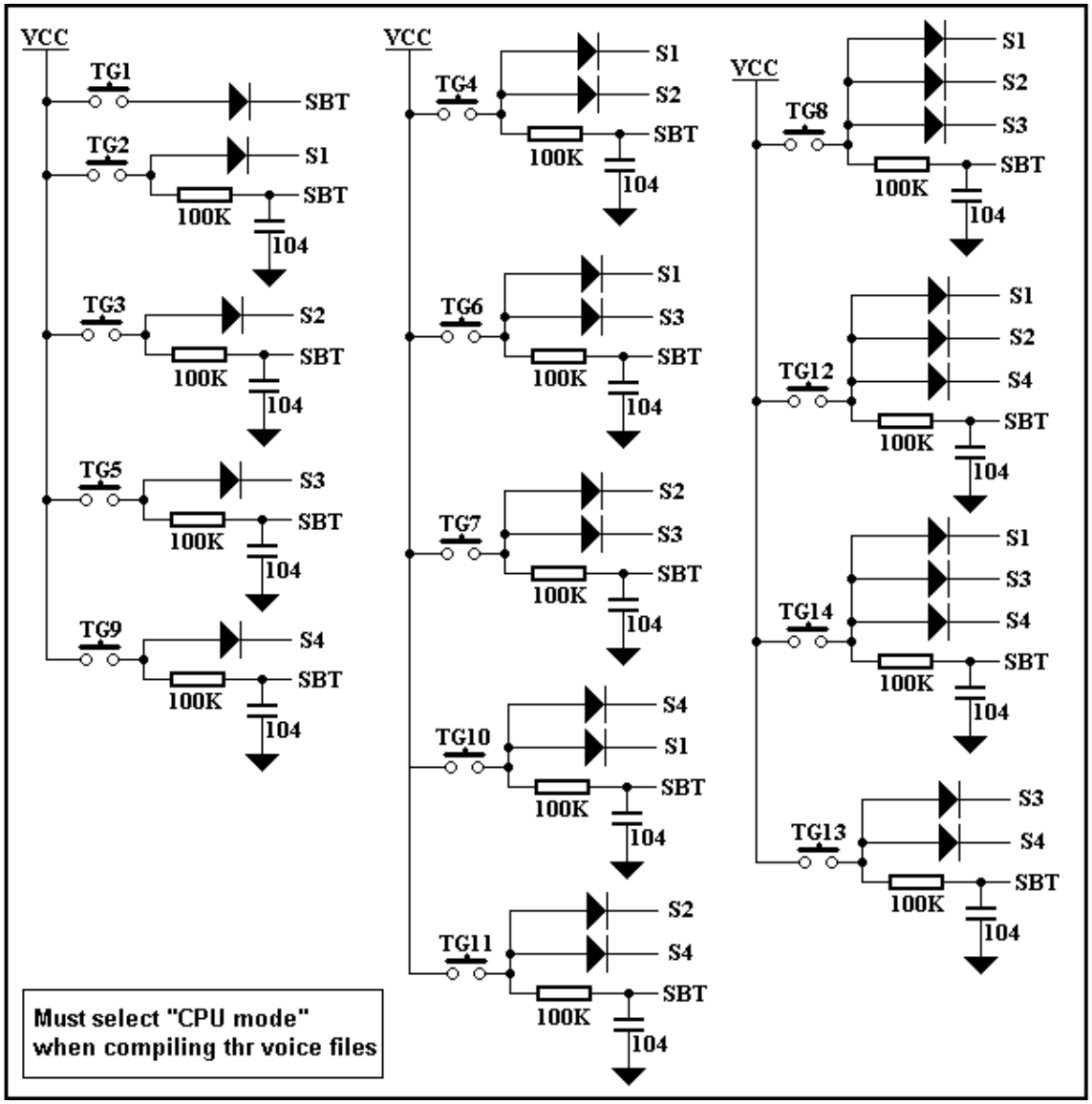
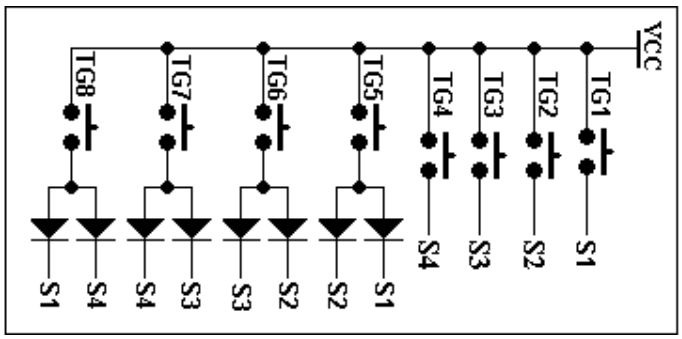


Fig. 2

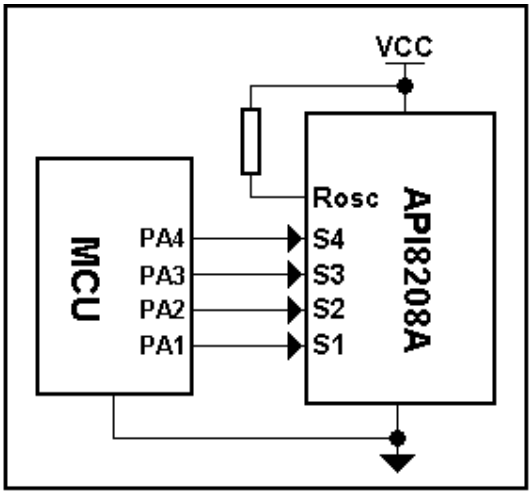
4. aP8821 Individually key application :

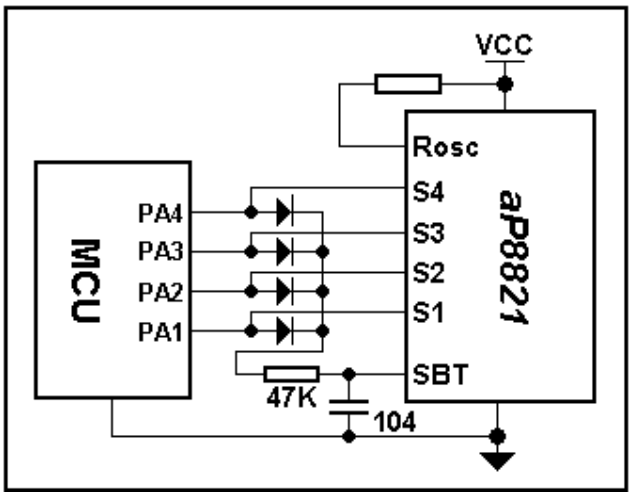


- **API8208A ALONE KEY TRIGGER APPLICATION :**



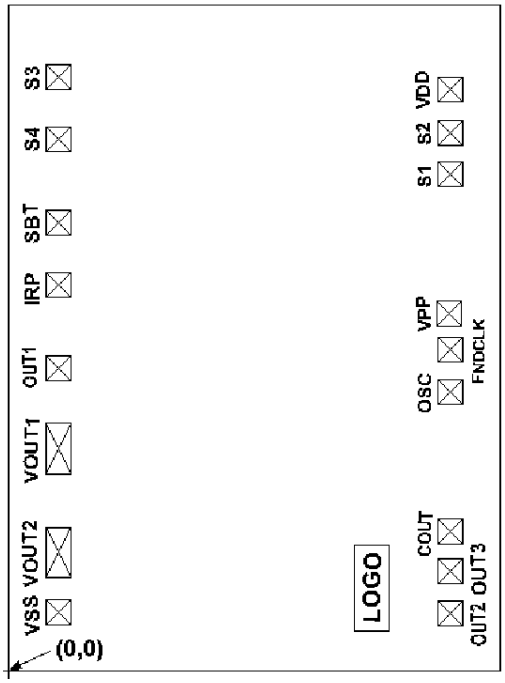
5. aP8821 & API8208A MCU CONTROL APPLICATION COMPARE :





	API8208A				aP8821 (CPU Mode)					
	S4	S3	S2	S1		S4	S3	S2	S1	SBT
					TG1	0	0	0	0	↑
TG1	0	0	0	1	**TG2**	**0**	**0**	**0**	**1**	↑
TG2	0	0	1	0	**TG3**	**0**	**0**	**1**	**0**	↑
TG3	0	1	0	0	**TG5**	**0**	**1**	**0**	**0**	↑
TG4	1	0	0	0	**TG9**	**1**	**0**	**0**	**0**	↑
TG5	0	0	1	1	**TG4**	**0**	**0**	**1**	**1**	↑
TG6	0	1	1	0	**TG7**	**0**	**1**	**1**	**0**	↑
TG7	1	1	0	0	**TG13**	**1**	**1**	**0**	**0**	↑
TG8	1	0	0	1	**TG10**	**1**	**0**	**0**	**1**	↑
					TG4	0	0	1	1	↑
					TG5	0	1	0	0	↑
					TG8	0	1	1	1	↑
					TG11	1	0	1	0	↑
					TG12	1	0	1	1	↑
					TG14	1	1	0	1	↑

Pin	Name	X	Y
1	OUT1	180	1100
2	VOUT1	180	800
3	VOUT2	180	430
4	VSS	180	213
5	OUT2	1600	208
6	OUT3	1600	360
7	COUT	1600	507
8	OSC	1600	1014
9	VPP	1600	1300
10	S1	1600	1800
11	S2	1600	1955
12	VDD	1600	2114
13	S3	180	2160
14	S4	180	1932
15	SBT	180	1630
16	IRP	180	1402



Note:Substrate must be connected to V_{SS}
Pad size = 90um x 90um