AP7217

500mA CMOS LDO

Features

- Very Low Dropout Voltage
- Low Current Consumption: Typ. 50μA
- Output Voltage: 3.3V
- Guaranteed 500mA (min) Output
- Input Range up to 5.5V
- Current Limiting
- Stable with either electrolytic capacitor or low-ESR MLCC (multi-layer ceramic capacitor) Low Temperature Coefficient
- SOP-8L: Available in "Green" Molding Compound (no Br, Sb)
- Lead Free Finish / RoHS Compliant (Note 1)

General Description

The AP7217 low-dropout linear regulator operates from a 3.3V to 5.5V supply and delivers a guaranteed 500mA (min) continuous load current.

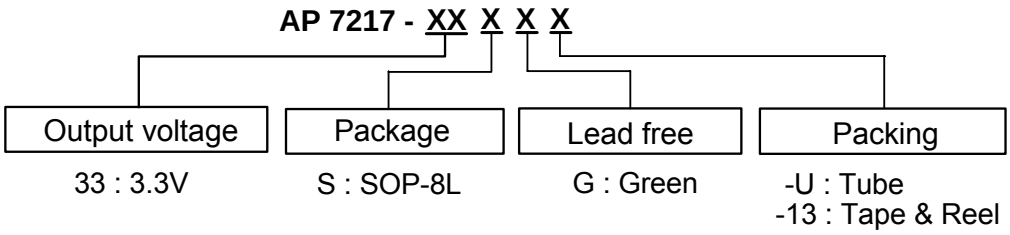
The high-accuracy output voltage is preset to an internally trimmed voltage. An active-low open-drain reset output remains asserted for at least 20ms (TYP) after output voltage reaches V_{DF}.

The space-saving SOP-8L package is suitable for "pocket" and hand-held applications.

Applications

- HD/BlueRay DVD & MP3/4 Players
- Mobile Handsets and Smartphones
- Digital Still Camera
- Hand-Held Computers

Ordering Information

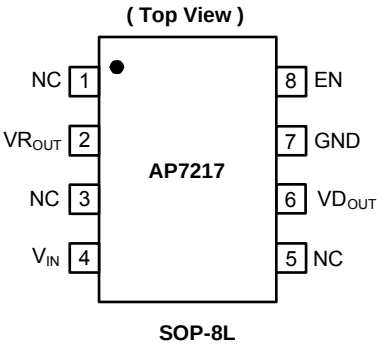


Note: 1. RoHS revision 13.2.2003. Glass and High Temperature Solder Exemptions Applied, see *EU Directive Annex Notes 5 and 7.*

Device	Package Code	Packaging (Note 2)	Tube		13" Tape and Reel	
			Quantity	Part Number Suffix	Quantity	Part Number Suffix
AP7217-XXS	S	SOP-8L	100	-U	2500/Tape & Reel	-13

Note: 2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be on our website at http://www.diodes.com/datasheets/ap02001.pdf.

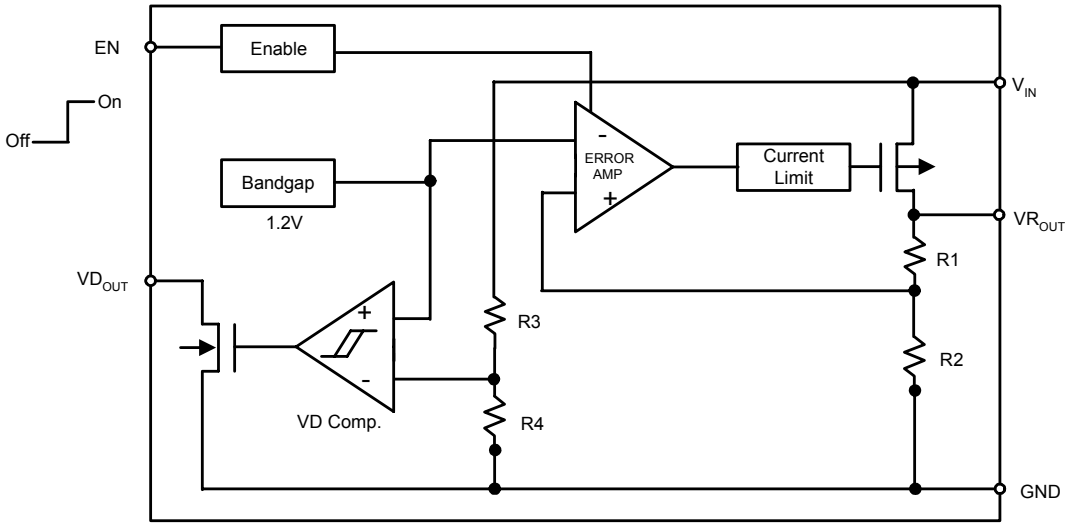
Pin Assignments



Pin Descriptions

Pin Name	Pin No.	Function
NC	1	No Connection
VR_{OUT}	2	Voltage Output
NC	3	No Connection
V_{IN}	4	Supply Voltage
NC	5	No connection
VD_{OUT}	6	V_D Output (Reset on I/P)
GND	7	Ground
EN	8	Enable (V_R On/Off)

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD MM	Machine Model ESD Protection	450	V
V_{IN}	Input Voltage	+6	V
I_{OUT}	Output Current	$P_D/ (V_{IN}-V_O)$	mA
VR_{OUT}	Output Voltage	GND - 0.3 ~ V_{IN}+ 0.3	V
T_J	Operating Junction Temperature Range	-40 to +125	ºC
$T_{J(MAX)}$	Maximum Junction Temperature	150	ºC
P_D	Internal Power Dissipation	1.2	W

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	3.3	5.5	V
I_{OUT}	Output Current	0	500	mA
T_A	Operating Ambient Temperature	-40	85	°C

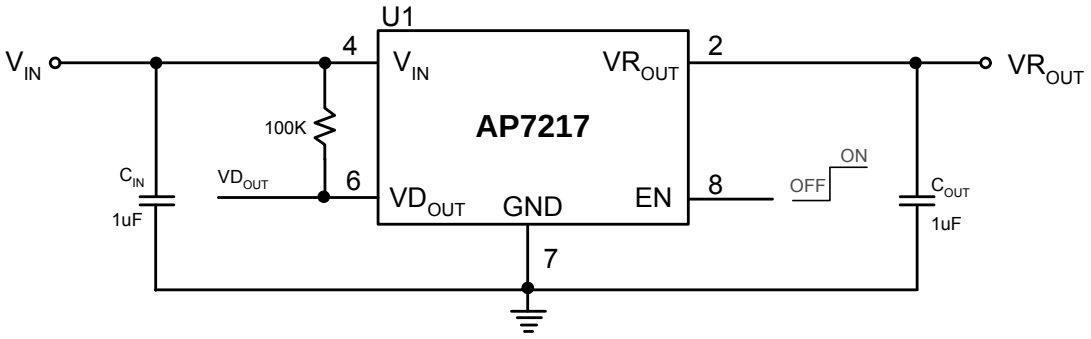
Electrical Characteristics

(T_A = 25°C, C_{IN} = 1μF, C_{OUT} = 1μF, V_{EN} = 2V, unless otherwise noted)

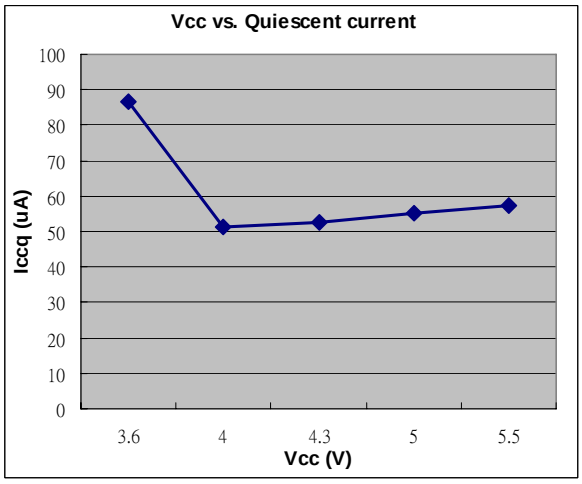
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_Q	Quiescent Current	I_O = 0mA	-	50	70	μA
I_{STB}	Standby Current	VEN = Off V_{IN} = 5.0V		15	30	μA
VR_{OUT}	Output Voltage Accuracy	I_O = 30mA, V_{IN} = 5V	3.234	3.300	3.366	V
	VR_{OUT} Temperature Coefficient	-40°C to 85°C, I_{OUT} = 30mA		±100		ppm / °C
$V_{DROPOUT}$	Dropout Voltage	I_{OUT} = 100mA		100	250	mV
I_{OUT}	Output Current	V_{IN} = 5.3V	500			mA
I_{LIMIT}	Current Limit	V_{IN} = 5.3V		600		mA
I_{short}	Short Circuit Current	V_{IN} = 5.3V		50		mA
$\Delta V_{LINE}/\Delta V_{IN}/VR_{OUT}$	Line Regulation	4.3V ≤ V_{IN} ≤ 5.5V; I_{OUT} = 30mA		0.01	±0.2	%/V
ΔVR_{OUT}	Load Regulation	1mA ≤ I_{OUT} ≤ 100mA, V_{IN} = 5.3V		15	50	mV
PSRR	Power Supply Rejection	V_{IN} = 4.3V+0.5Vp-pAC, F= 1KHz I_{OUT} = 50mA		55		dB
V_{EH}	EN Input Threshold	Output ON	1.6			V
V_{EL}		Output OFF			0.25	V
I_{EN}	Enable Pin Current		-0.1		0.1	μA
V_{DF}	Detect fall voltage		3.83	3.91	3.98	V
$V_{Hysteresis}$	V_D Hysteresis Range		V_{DF} x1.02	V_{DF} x1.05	V_{DF} x1.08	V
IVD_{OUT}	VD Supply Current	VD_{OUT} = 0.5V V_{IN} = 2.0V 3.0V		 20 30		mA
t_{RP}	V_{DOUT} Delay Time	V_{IN} = 1.8V to VDF+1V	10	20	40	mSec
θ_{JA}	Thermal Resistance	SOP-8L (Note 3)		134		°C/W
θ_{JC}	Thermal Resistance	SOP-8L (Note 3)		28		°C/W

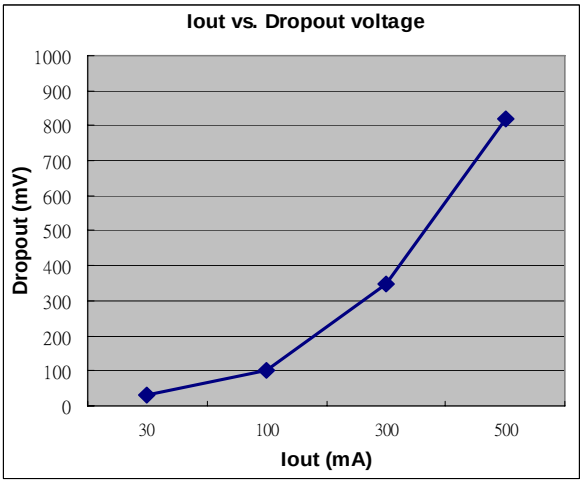
Note: 3. Test conditions for SOP-8L: Devices mounted on FR-4 PC board, MRP, 2oz copper layout, calibrate at T_J=150 °C, measure at T_A=25°C, minimum recommended pad layout

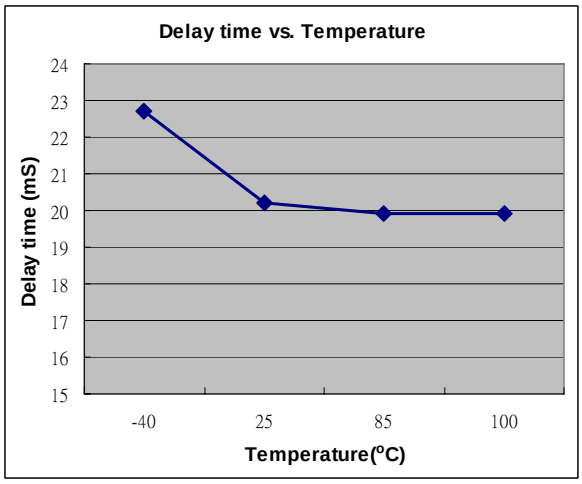
Typical Application

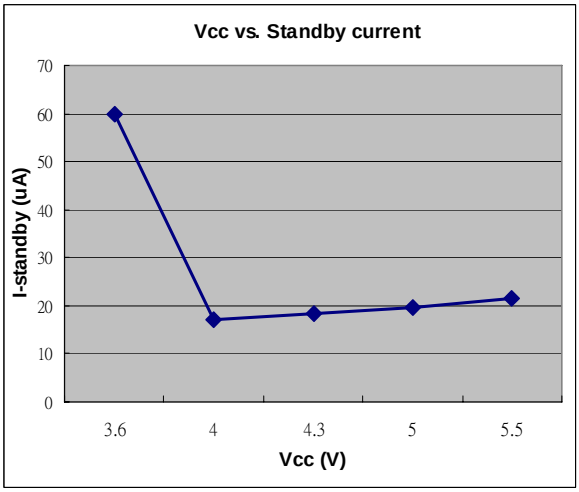


Typical Performance Characteristics



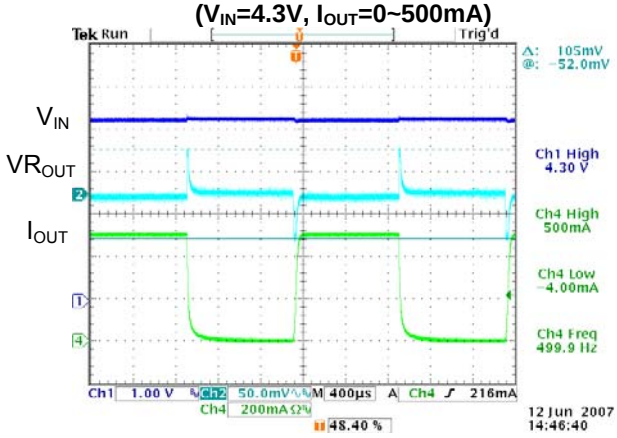




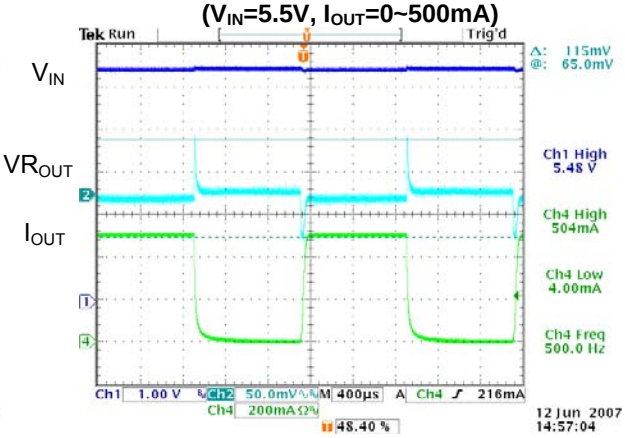


Typical Performance Characteristics (Continued)

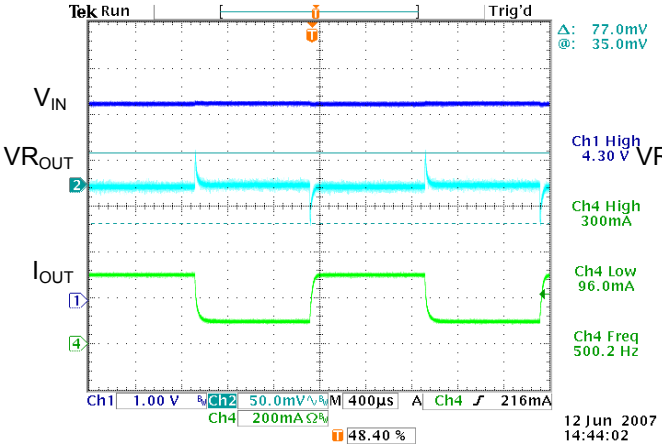
Load Transient Response
(V_{IN}=4.3V, I_{OUT}=0~500mA)



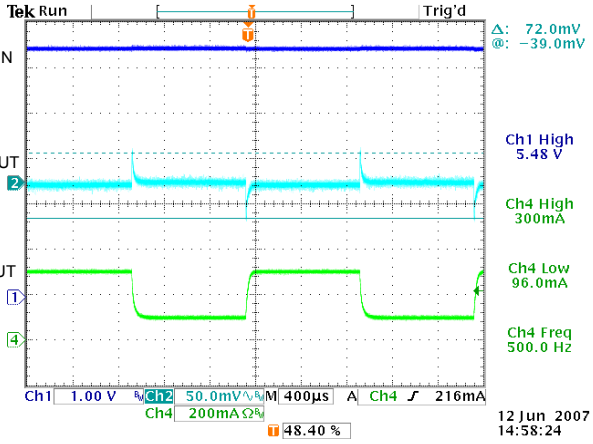
Load Transient Response
(V_{IN}=5.5V, I_{OUT}=0~500mA)



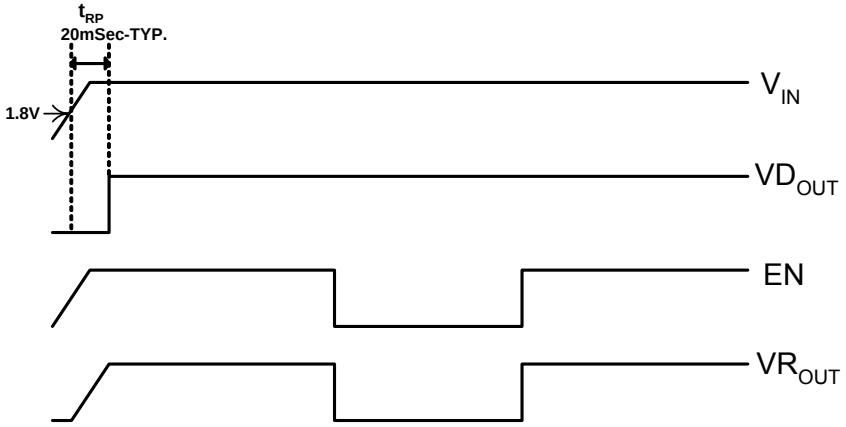
Load Transient Response
(V_{IN}=4.3V, I_{OUT}=100~300mA)



Load Transient Response
(V_{IN}=5.5V, I_{OUT}=100~300mA)



Timing Diagram



Application Note

Input Capacitor
A 1μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. A lower ESR (Equivalent Series Resistance) capacitor allows the use of less capacitance, while higher ESR type requires more capacitance. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor
The output capacitor is required to stabilize and help the transient response of the LDO. The AP7217 is designed to have excellent transient response for most applications with a small amount of output capacitance. The AP7217 is stable with any small ceramic output capacitors of 1.0μF or higher value, and the temperature coefficients of X7R or X5R type. Additional capacitance helps to reduce undershoot and overshoot during transient. For PCB layout, the output capacitor must be placed as close as possible to OUT and GND pins, and keep the leads as short as possible.

ENABLE/SHUTDOWN Operation
The AP7217 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

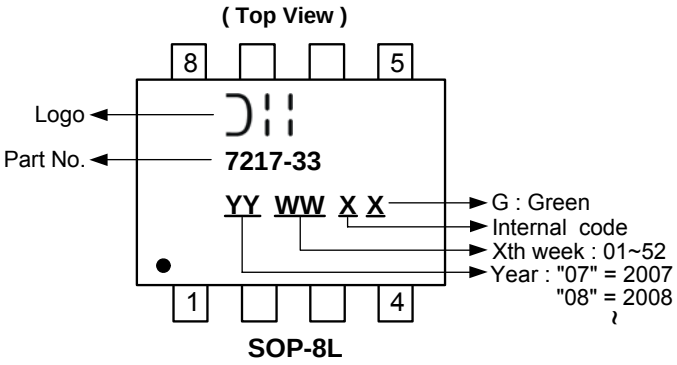
	VR_{OUT}	VD_{OUT}
EN=0	0V	Φ
EN=1	3.3V	Φ

Current Limit Protection
When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 600mA to prevent over-current and to protect the regulator from damage due to overheating.

Short circuit protection
When VRout pin is shorted to GND or VRout voltage is less than 200mV, short circuit protection will be triggered and clamp the output current to approximately 50mA.

VD_{OUT} (reset output)
---Open-Drain Active-Low reset output---
In general, VD_{OUT} is pulled up by a resistor (100Kohm) to V_{IN}. The AP7217 microprocess (uP) supervisory circuitry asserts a guaranteed logic-low reset during power-up and power-down. Reset is asserted asserts when V_{IN} is below the reset threshold and remain asserted for at least t_{RP} after V_{IN} rises above the reset threshold.
As long as V_{IN} is lower than the reset threshold, VD_{OUT} remains at logic "0". When V_{IN} become higher than V_{TH}, a logic "1" is asserted after a time delay defined by t_{RP}.

Marking Information



Package Information (unit: mm)

Package type: SOP-8L