18-Mbit (512K x 36/1M x 18) Pipelined SRAM

Features

- Supports bus operation up to 250 MHz
- Available speed grades are 250, 200 and 167 MHz
- Registered inputs and outputs for pipelined operation
- 3.3V core power supply
- 2.5V / 3.3V I/O operation
- Fast clock-to-output times
  - — 2.6 ns (for 250-MHz device)
  - — 3.0 ns (for 200-MHz device)
  - — 3.4 ns (for 167-MHz device)
- Provide high-performance 3-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- Single Cycle Chip Deselect
- Offered in JEDEC-standard lead-free 100-pin TQFP, 119-ball BGA and 165-Ball fBGA packages
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- "ZZ" Sleep Mode Option

Functional Description[1]

The CY7C1380D/CY7C1382D SRAM integrates 524,288 x 36 and 1,048,576 x 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE_1}$), depth-expansion Chip Enables (CE_2 and $\overline{CE_3}$[2]), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW_X}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle.This part supports Byte Write operations (see Pin Descriptions and Truth Table for further details). Write cycles can be one to two or four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ when active LOW causes all bytes to be written.

The CY7C1380D/CY7C1382D operates from a +3.3V core power supply while all outputs may operate with either a +2.5 or +3.3V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

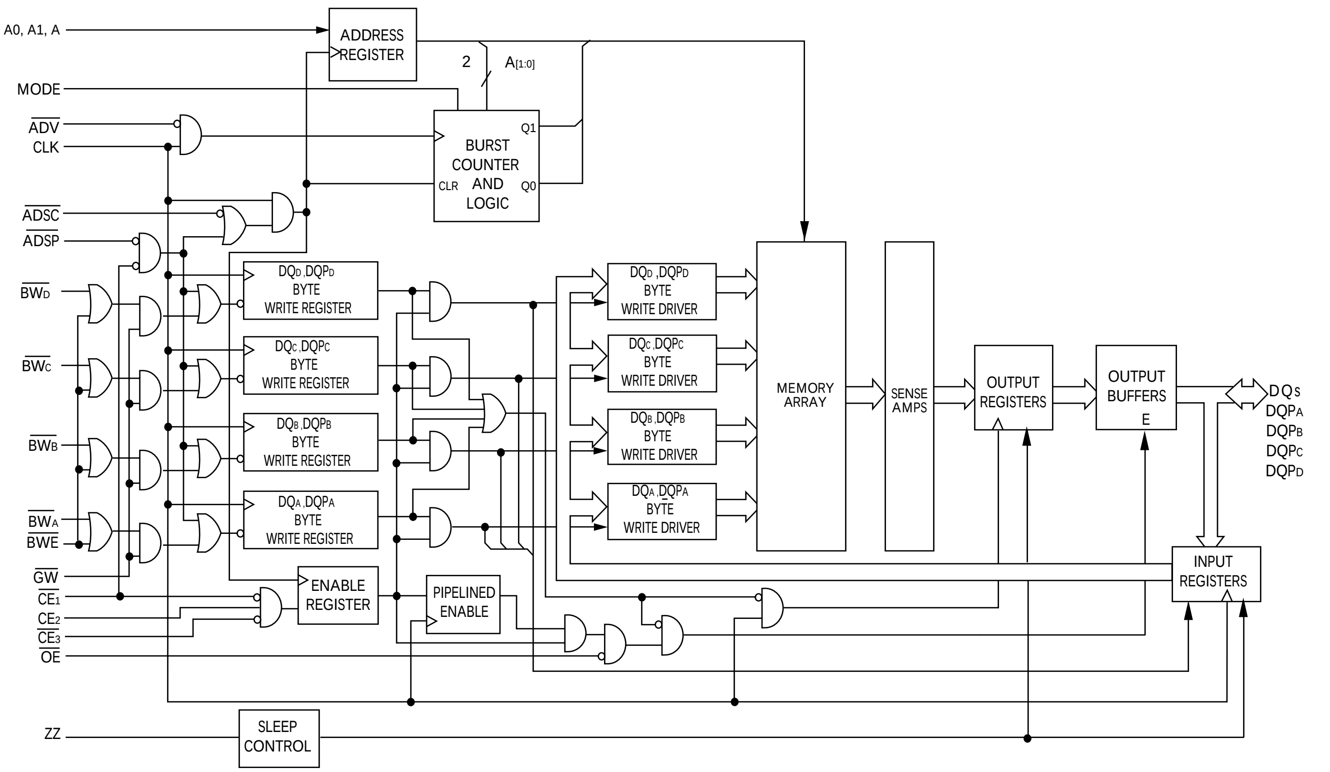
Selection Guide

	250 MHz	200 MHz	167 MHz	Unit
Maximum Access Time	2.6	3.0	3.4	ns
Maximum Operating Current	350	300	275	mA
Maximum CMOS Standby Current	70	70	70	mA

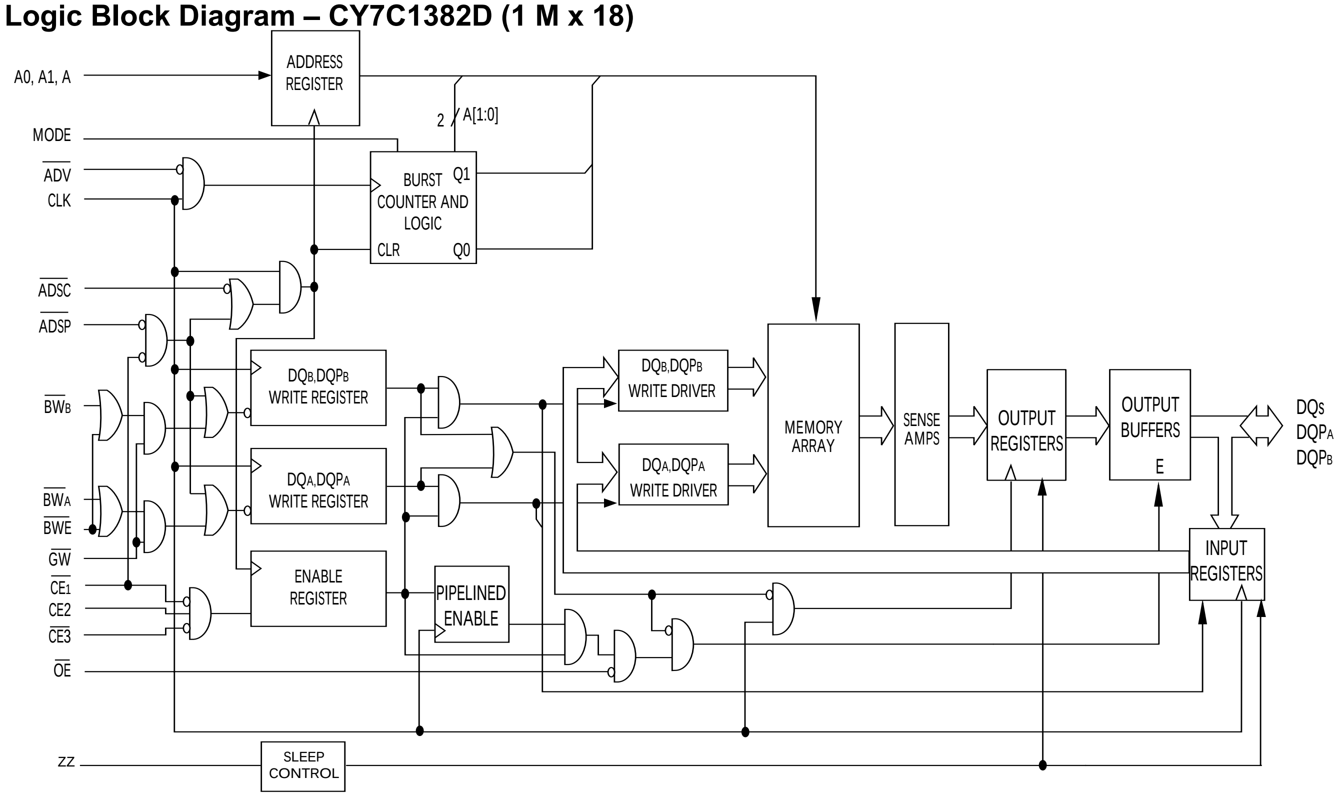
Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

Notes:
1. For best–practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.
2. $\overline{CE_3}$, CE_2 are for TQFP and 165 fBGA package only. 119 BGA is offered only in 1 Chip Enable.

Logic Block Diagram – CY7C1380D (512K x 36)

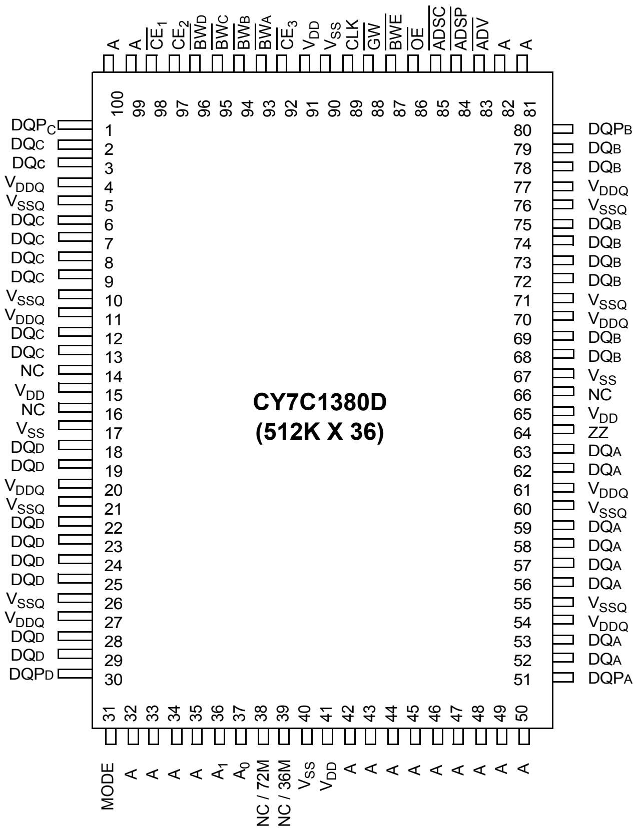


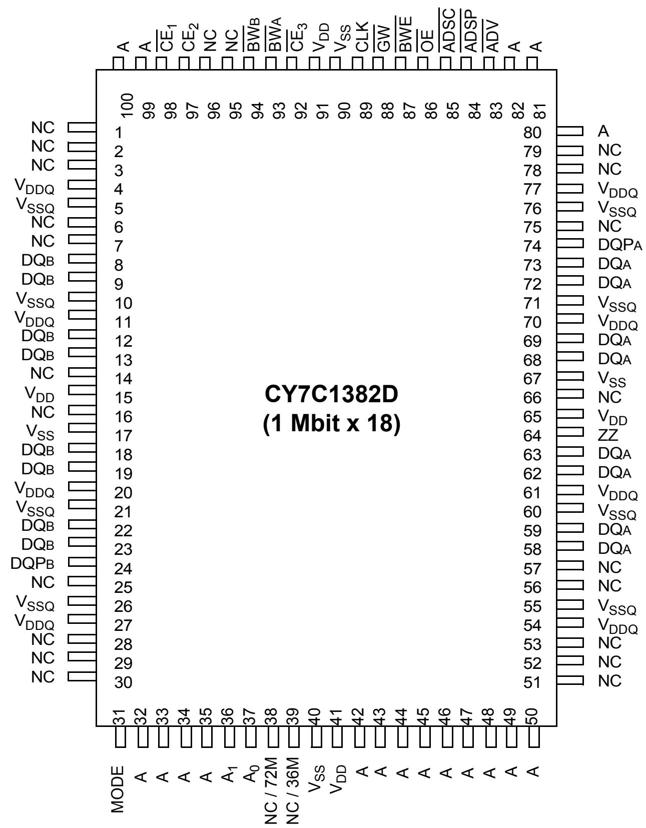
Logic Block Diagram – CY7C1382D (1 M x 18)



Pin Configurations

100-pin TQFP Pinout





Pin Configurations (continued)

119-ball BGA (1 Chip Enable with JTAG)

CY7C1380D (512K x 36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	A	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE}_1$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW}_C$	$\overline{ADV}$	$\overline{BW}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW}_D$	NC	$\overline{BW}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BWE}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC / 72M	A	A	A	NC / 36M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1382D (512K x 18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	A	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_B	NC	V_{SS}	NC	V_{SS}	DQP_A	NC
E	NC	DQ_B	V_{SS}	$\overline{CE}_1$	V_{SS}	NC	DQ_A
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_A	V_{DDQ}
G	NC	DQ_B	$\overline{BW}_B$	$\overline{ADV}$	NC	NC	DQ_A
H	DQ_B	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_A	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_B	V_{SS}	CLK	V_{SS}	NC	DQ_A
L	DQ_B	NC	NC	NC	$\overline{BW}_A$	DQ_A	NC
M	V_{DDQ}	DQ_B	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	DQ_B	NC	V_{SS}	A1	V_{SS}	DQ_A	NC
P	NC	DQP_B	V_{SS}	A0	V_{SS}	NC	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC / 72M	A	A	NC / 36M	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations (continued)

165-ball fBGA
CY7C1380D (512K x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC / 288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC / 144M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC / 72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC / 36M	A	A	TMS	A0	TCK	A	A	A	A

CY7C1382D (1M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC / 288M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC	A	CE2	NC	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC / 144M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_A
D	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
E	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
F	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
G	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
K	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
L	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
M	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
N	DQP_B	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC / 72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC / 36M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE_1, CE_2, and CE_3 [2] are sampled active. A1: A0 are fed to the two-bit counter..
BWA,BWB BWC,BWD	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with BWE to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
GW	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on BW_X and BWE).
BWE	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
CE_1	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and CE_3 to select/deselect the device. ADSP is ignored if CE_1 is HIGH.
CE_2[2]	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with CE_1 and CE_3 to select/deselect the device.
CE_3[2]	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_1 and CE_2 to select/deselect the device.Not available for AJ package version.Not connected for BGA. Where referenced, CE_3 is assumed active throughout this document for BGA.
OE	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. OE is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
ADSP	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDP is ignored when CE_1 is deasserted HIGH.
ADSC	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ	Input-Asynchronous	**ZZ "sleep" Input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs, DQP_X	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tri-state condition.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{SSQ}	I/O Ground	**Ground for the I/O circuitry**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
MODE	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be disconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.

Pin Definitions (continued)

Name	I/O	Description
TMS	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not being utilized, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No Connects**. Not internally connected to the die

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.6 ns (250-MHz device).

The CY7C1380D/CY7C1382D supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BW_X) inputs. A Global Write Enable (GW) overrides all Byte Write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed Write circuitry.

Three synchronous Chip Selects (CE_1, CE_2, CE_3) and an asynchronous Output Enable (OE) provide for easy bank selection and output tri-state control. ADSP is ignored if CE_1 is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) CE_1, CE_2, CE_3 are all asserted active, and (3) the Write signals (GW, BWE) are all deserted HIGH. ADSP is ignored if CE_1 is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the Address Register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 2.6 ns (250-MHz device) if OE is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single Read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output will tri-state immediately.

Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) CE_1, CE_2, CE_3 are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The Write signals (GW, BWE, and BW_X) and ADV inputs are ignored during this first cycle.

ADSP-triggered Write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If GW is HIGH, then the Write operation is controlled by BWE and BW_X signals. The CY7C1380D/CY7C1382D provides Byte Write capability that is described in the Write Cycle Descriptions table. Asserting the Byte Write Enable input (BWE) with the selected Byte Write (BW_X) input, will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1380D/CY7C1382D is a common I/O device, the Output Enable (OE) must be deserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

ADSC Write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deserted HIGH, (3) CE_1, CE_2, CE_3 are all asserted active, and (4) the appropriate combination of the Write inputs (GW, BWE, and BW_X) are asserted active to conduct a Write to the desired byte(s). ADSC-triggered Write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The ADV input is ignored during this cycle. If a global Write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a Byte Write is conducted, only the selected bytes are written. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1380D/CY7C1382D is a common I/O device, the Output Enable (OE) must be deserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1380D/CY7C1382D provides a two-bit wraparound counter, fed by A1: A0, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

Interleaved Burst Address Table (MODE = Floating or VDD)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE_1}$, CE_2, $\overline{CE_3}$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2V$		80	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ Active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

Truth Table [3, 4, 5, 6, 7, 8]

Operation	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	H	L	X	X	X	L-H	Tri-State
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-State
WRITE Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-State
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-State

Notes:

3. X = “Don't Care.” H = Logic HIGH, L = Logic LOW.
4. $\overline{WRITE}$ = L when any one or more Byte Write enable signals and $\overline{BWE}$ = L or $\overline{GW}$= L. $\overline{WRITE}$ = H when all Byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
5. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
6. $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are available only in the TQFP package. BGA package has only two chip selects $\overline{CE_1}$ and CE_2.
7. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
8. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are Tri-State when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).
9. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write will be done based on which byte write is active.

Truth Table (continued)[3, 4, 5, 6, 7, 8]

Operation	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-State
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-State
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-State
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Truth Table for Read/Write[5,9]

Function (CY7C1380D)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	H	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C – (DQ_C and DQP_C)	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D – (DQ_D and DQP_D)	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Truth Table for Read/Write[5,9]

Function (CY7C1382D)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	L	H
Write Bytes B, A	H	L	L	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

IEEE 1149.1 Serial Boundary Scan (JTAG)

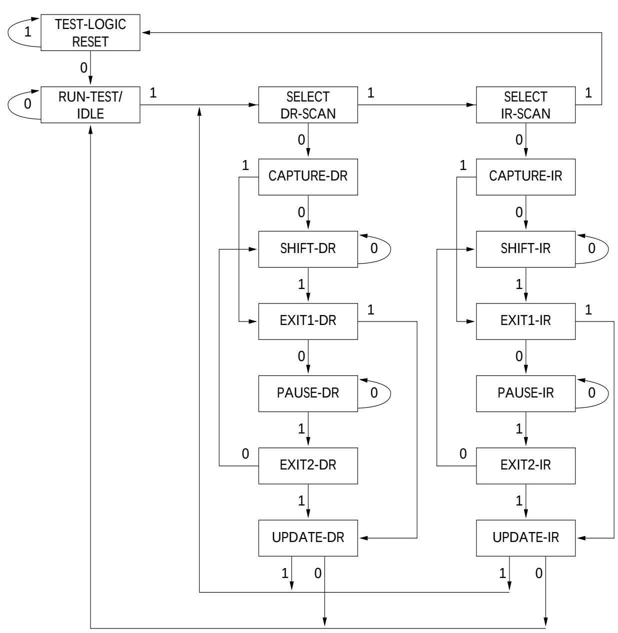
The CY7C1380D/CY7C1382D incorporates a serial boundary scan test access port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This part operates in accordance with IEEE Standard 1149.1-1900, but doesn't have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. . The TAP operates using JEDEC-standard 3.3V or 2.5V I/O logic levels.

The CY7C1380D/CY7C1382D contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

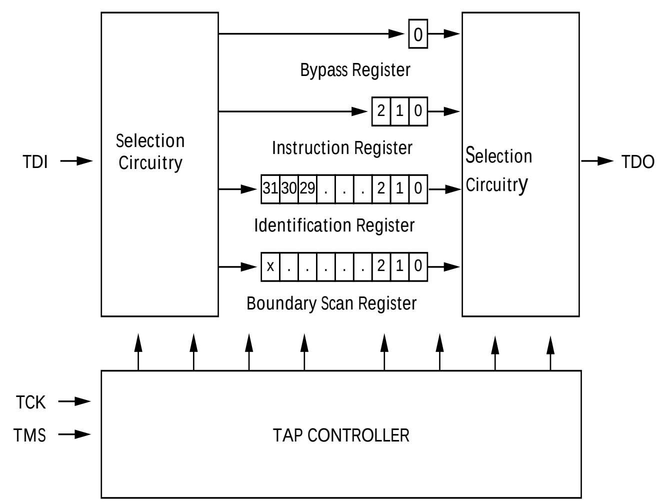
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Tap Controller Block Diagram.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Tap Controller State Diagram.)

TAP Controller Block Diagram



Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the

TDI and TDO balls as shown in the Tap Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant with 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required - that is, while data captured is shifted out, the preloaded data can be shifted in.

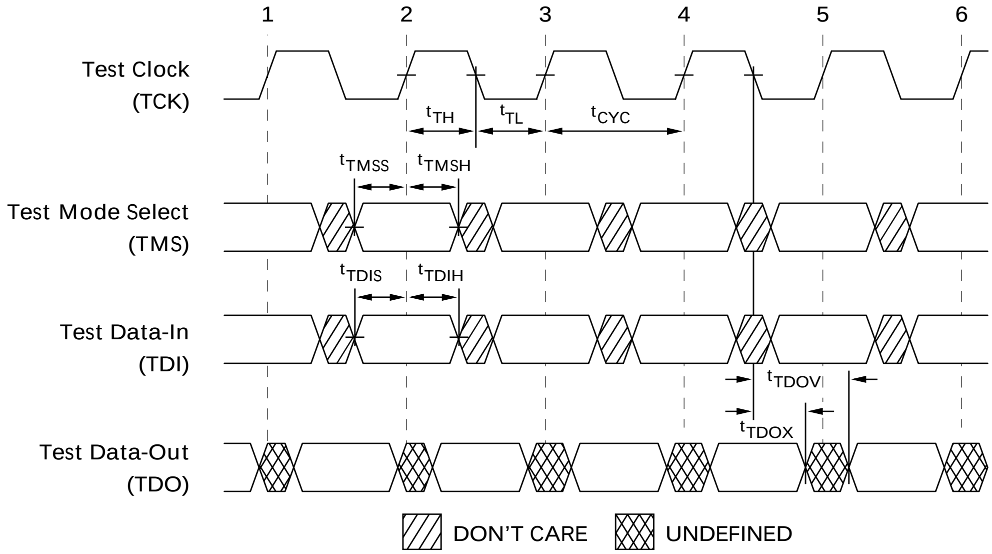
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing



TAP AC Switching Characteristics Over the Operating Range[10, 11]

Parameter	Description	Min.	Max.	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH time	25		ns
t_{TL}	TCK Clock LOW time	25		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		5	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	5		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	5		ns
t_{CS}	Capture Set-up to TCK Rise	5		
Hold Times				
t_{TMSH}	TMS hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

Notes:

10. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1ns.

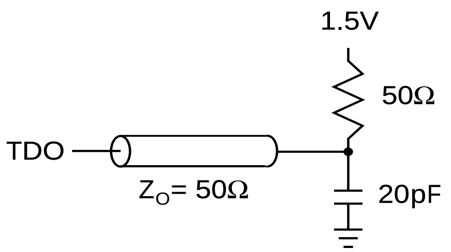
3.3V TAP AC Test Conditions

Input pulse levels .... VSS to 3.3V
Input rise and fall times ....1 ns
Input timing reference levels 1.5V
Output reference levels...1.5V
Test load termination supply voltage 1.5V

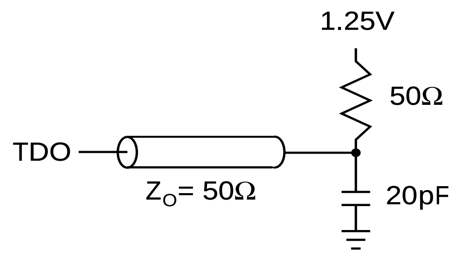
2.5V TAP AC Test Conditions

Input pulse levels .... VSS to 2.5V
Input rise and fall time ....1 ns
Input timing reference levels.................. ....1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

3.3V TAP AC Output Load Equivalent



2.5V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics And Operating Conditions

(0°C < TA < +70°C; Vdd = 3.3V ±0.165V unless otherwise noted)[12]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA, V_{DDQ} = 3.3V		2.4		V
		I_{OH} = –1.0 mA, V_{DDQ} = 2.5V		2.0		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3V	2.9		V
			V_{DDQ} = 2.5V	2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3V		0.4	V
			V_{DDQ} = 2.5V		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3V		0.2	V
			V_{DDQ} = 2.5V		0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 3.3V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 3.3V	–0.3	0.8	V
			V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Identification Register Definitions

Instruction Field	CY7C1380D (512K x 36)	CY7C1382D (1 Mbit x 18)	Description
Revision Number (31:29)	000	000	Describes the version number.
Device Depth (28:24)[13]	01011	01011	Reserved for Internal Use
Device Width (23:18)	000000	000000	Defines memory type and architecture
Cypress Device ID (17:12)	100101	010101	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register.

Notes:
12. All voltages referenced to VSS (GND).
13. Bit #24 is “1” in the Register Definitions for both 2.5v and 3.3v versions of this device.

Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order (119-ball BGA package)	85	85
Boundary Scan Order (165-ball fBGA package)	89	89

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

119-Ball BGA Boundary Scan Order [14, 15]

CY7C1380D (256K x 36)			
Bit#	**Ball ID**	**Bit#**	**Ball ID**
1	H4	44	E4
2	T4	45	G4
3	T5	46	A4
4	T6	47	G3
5	R5	48	C3
6	L5	49	B2
7	R6	50	B3
8	U6	51	A3
9	R7	52	C2
10	T7	53	A2
11	P6	54	B1
12	N7	55	C1
13	M6	56	D2
14	L7	57	E1
15	K6	58	F2
16	P7	59	G1
17	N6	60	H2
18	L6	61	D1
19	K7	62	E2
20	J5	63	G2
21	H6	64	H1
22	G7	65	J3
23	F6	66	K2
24	E7	67	L1
25	D7	68	M2
26	H7	69	N1
27	G6	70	P1
28	E6	71	K1
29	D6	72	L2
30	C7	73	N2
31	B7	74	P2
32	C6	75	R3
33	A6	76	T1
34	C5	77	R1
35	B5	78	T2
36	G5	79	L3
37	B6	80	R2
38	D4	81	T3
39	B4	82	L4
40	F4	83	N4
41	M4	84	P4
42	A5	85	Internal
43	K4		

CY7C1382D (512K x 18)			
Bit#	**Ball ID**	**Bit#**	**Ball ID**
1	H4	44	E4
2	T4	45	G4
3	T5	46	A4
4	T6	47	G3
5	R5	48	C3
6	L5	49	B2
7	R6	50	B3
8	U6	51	A3
9	R7	52	C2
10	T7	53	A2
11	P6	54	B1
12	N7	55	C1
13	M6	56	D2
14	L7	57	E1
15	K6	58	F2
16	P7	59	G1
17	N6	60	H2
18	L6	61	D1
19	K7	62	E2
20	J5	63	G2
21	H6	64	H1
22	G7	65	J3
23	F6	66	K2
24	E7	67	L1
25	D7	68	M2
26	H7	69	N1
27	G6	70	P1
28	E6	71	K1
29	D6	72	L2
30	C7	73	N2
31	B7	74	P2
32	C6	75	R3
33	A6	76	T1
34	C5	77	R1
35	B5	78	T2
36	G5	79	L3
37	B6	80	R2
38	D4	81	T3
39	B4	82	L4
40	F4	83	N4
41	M4	84	P4
42	A5	85	Internal
43	K4		

Notes:
14. Balls that are NC (No Connect) are preset LOW.
15. Bit# 85 is preset HIGH.

165-Ball BGA Boundary Scan Order [14, 16]

CY7C1380D (256K x 36)			
Bit#	Ball ID	Bit#	Ball ID
1	N6	37	A9
2	N7	38	B9
3	10N	39	C10
4	P11	40	A8
5	P8	41	B8
6	R8	42	A7
7	R9	43	B7
8	P9	44	B6
9	P10	45	A6
10	R10	46	B5
11	R11	47	A5
12	H11	48	A4
13	N11	49	B4
14	M11	50	B3
15	L11	51	A3
16	K11	52	A2
17	J11	53	B2
18	M10	54	C2
19	L10	55	B1
20	K10	56	A1
21	J10	57	C1
22	H9	58	D1
23	H10	59	E1
24	G11	60	F1
25	F11	61	G1
26	E11	62	D2
27	D11	63	E2
28	G10	64	F2
29	F10	65	G2
30	E10	66	H1
31	D10	67	H3
32	C11	68	J1
33	A11	69	K1
34	B11	70	L1
35	A10	71	M1
36	B10	72	J2

CY7C1380D (256K x 36)	
Bit#	Ball ID
73	K2
74	L2
75	M2
76	N1
77	N2
78	P1
79	R1
80	R2
81	P3
82	R3
83	P2
84	R4
85	P4
86	N5
87	P6
88	R6
89	Internal

Note:
16. Bit# 89 is preset HIGH.

165-Ball BGA Boundary Scan Order [14, 16]

CY7C1382D (512K x 18)			
Bit#	Ball ID	Bit#	Ball ID
1	N6	37	A9
2	N7	38	B9
3	10N	39	C10
4	P11	40	A8
5	P8	41	B8
6	R8	42	A7
7	R9	43	B7
8	P9	44	B6
9	P10	45	A6
10	R10	46	B5
11	R11	47	A5
12	H11	48	A4
13	N11	49	B4
14	M11	50	B3
15	L11	51	A3
16	K11	52	A2
17	J11	53	B2
18	M10	54	C2
19	L10	55	B1
20	K10	56	A1
21	J10	57	C1
22	H9	58	D1
23	H10	59	E1
24	G11	60	F1
25	F11	61	G1
26	E11	62	D2
27	D11	63	E2
28	G10	64	F2
29	F10	65	G2
30	E10	66	H1
31	D10	67	H3
32	C11	68	J1
33	A11	69	K1
34	B11	70	L1
35	A10	71	M1
36	B10	72	J2

CY7C1382D (512Kx18)	
Bit#	Ball ID
73	K2
74	L2
75	M2
76	N1
77	N2
78	P1
79	R1
80	R2
81	P3
82	R3
83	P2
84	R4
85	P4
86	N5
87	P6
88	R6
89	Internal

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND........ –0.3V to +4.6V

DC Voltage Applied to Outputs in Tri-State .... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage .... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)... 20 mA

Static Discharge Voltage.. >2001V (per MIL-STD-883, Method 3015)

Latch-up Current.. >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V – 5%/+10%	2.5V – 5% to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics Over the Operating Range [17, 18]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	V_{DDQ} = 3.3V		3.135	V_{DD}	V
		V_{DDQ} = 2.5V		2.375	2.625	V
V_{OH}	Output HIGH Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OH} = –4.0 mA		2.4		V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OL} = 8.0 mA			0.4	V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OL} = 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage[17]	V_{DDQ} = 3.3V		2.0	V_{DD} + 0.3V	V
		V_{DDQ} = 2.5V		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[17]	V_{DDQ} = 3.3V		–0.3	0.8	V
		V_{DDQ} = 2.5V		–0.3	0.7	V
I_X	Input Load Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
	Input Current of ZZ	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4.0-ns cycle, 250 MHz		350	mA
			5.0-ns cycle, 200 MHz		300	mA
			6.0-ns cycle, 167 MHz		275	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	4.0-ns cycle, 250 MHz		160	mA
			5.0-ns cycle, 200 MHz		150	mA
			6.0-ns cycle, 167 MHz		140	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All speeds		70	mA
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V f = f_{MAX} = $1/t_{CYC}$	4.0-ns cycle, 250 MHz		135	mA
			5.0-ns cycle, 200 MHz		130	mA
			6.0-ns cycle, 167 MHz		125	mA
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speeds		80	mA

Shaded areas contain advance information.

Notes:
17. Overshoot: $V_{IH}(AC) < V_{DD}$ +1.5V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC)$ > -2V (Pulse width less than $t_{CYC}/2$).
18. TPower-up: Assumes a linear ramp from 0v to V_{DD}(min.) within 200ms. During this time $V_{IH} \leq V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

Thermal Resistance[19]

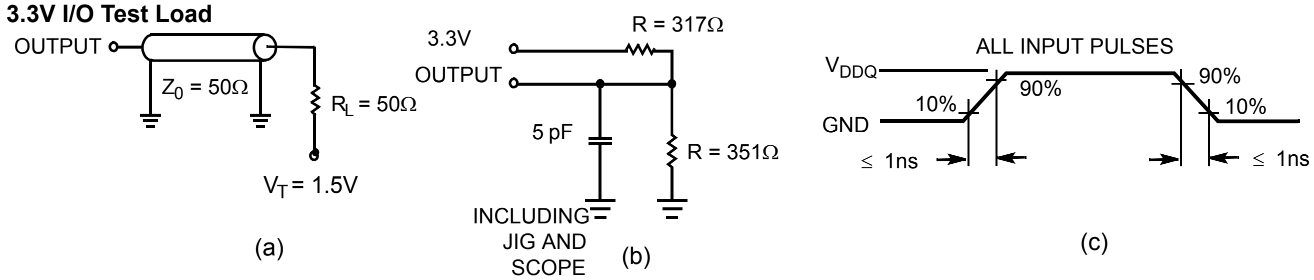
Parameter	Description	Test Conditions	TQFP Package	BGA Package	fBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	31	45	46	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		6	7	3	°C/W

Capacitance[19]

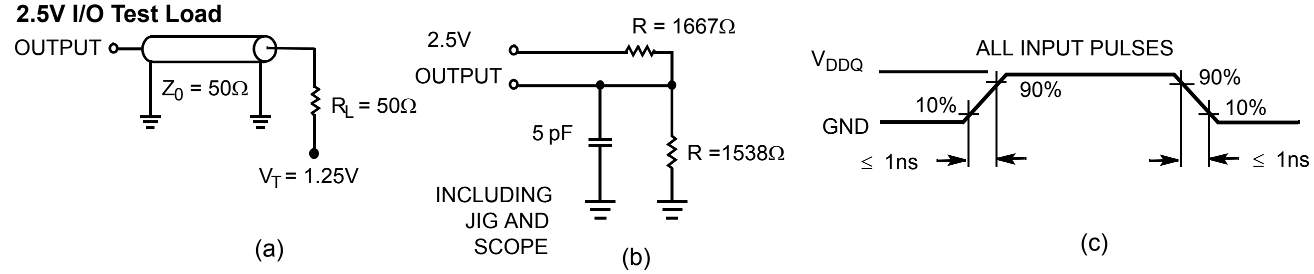
Parameter	Description	Test Conditions	TQFP Package	BGA Package	fBGA Package	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V. V_{DDQ} = 2.5V	5	8	9	pF
C_{CLK}	Clock Input Capacitance		5	8	9	pF
$C_{I/O}$	Input/Output Capacitance		5	8	9	pF

AC Test Loads and Waveforms

3.3V I/O Test Load



2.5V I/O Test Load



Notes:

19. Tested initially and after any design or process change that may affect these parameters

Switching Characteristics Over the Operating Range[24, 25]

Parameter	Description	250 MHz		200 MHz		167 MHz		Unit
		Min.	Max			Min.	Max	
t_{POWER}	V_{DD}(Typical) to the first Access[20]	1		1		1		ms
Clock								
t_{CYC}	Clock Cycle Time	4.0		5		6		ns
t_{CH}	Clock HIGH	1.7		2.0		2.2		ns
t_{CL}	Clock LOW	1.7		2.0		2.2		ns
Output Times								
t_{CO}	Data Output Valid After CLK Rise		2.6		3.0		3.4	ns
t_{DOH}	Data Output Hold After CLK Rise	1.0		1.3		1.3		ns
t_{CLZ}	Clock to Low-Z[21, 22, 23]	1.0		1.3		1.3		ns
t_{CHZ}	Clock to High-Z[21, 22, 23]		2.6		3.0		3.4	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		2.6		3.0		3.4	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low-Z[21, 22, 23]	0		0		0		ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High-Z[21, 22, 23]		2.6		3.0		3.4	ns
Setup Times								
t_{AS}	Address Set-up Before CLK Rise	1.2		1.4		1.5		ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ Set-up Before CLK Rise	1.2		1.4		1.5		ns
t_{ADVS}	$\overline{ADV}$ Set-up Before CLK Rise	1.2		1.4		1.5		ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_X$ Set-up Before CLK Rise	1.2		1.4		1.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	1.2		1.4		1.5		ns
t_{CES}	Chip Enable Set-Up Before CLK Rise	1.2		1.4		1.5		ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.3		0.4		0.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.3		0.4		0.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.3		0.4		0.5		ns
t_{WEH}	$\overline{GW}$,$\overline{BWE}$, $\overline{BW}_X$ Hold After CLK Rise	0.3		0.4		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.3		0.4		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.3		0.4		0.5		ns

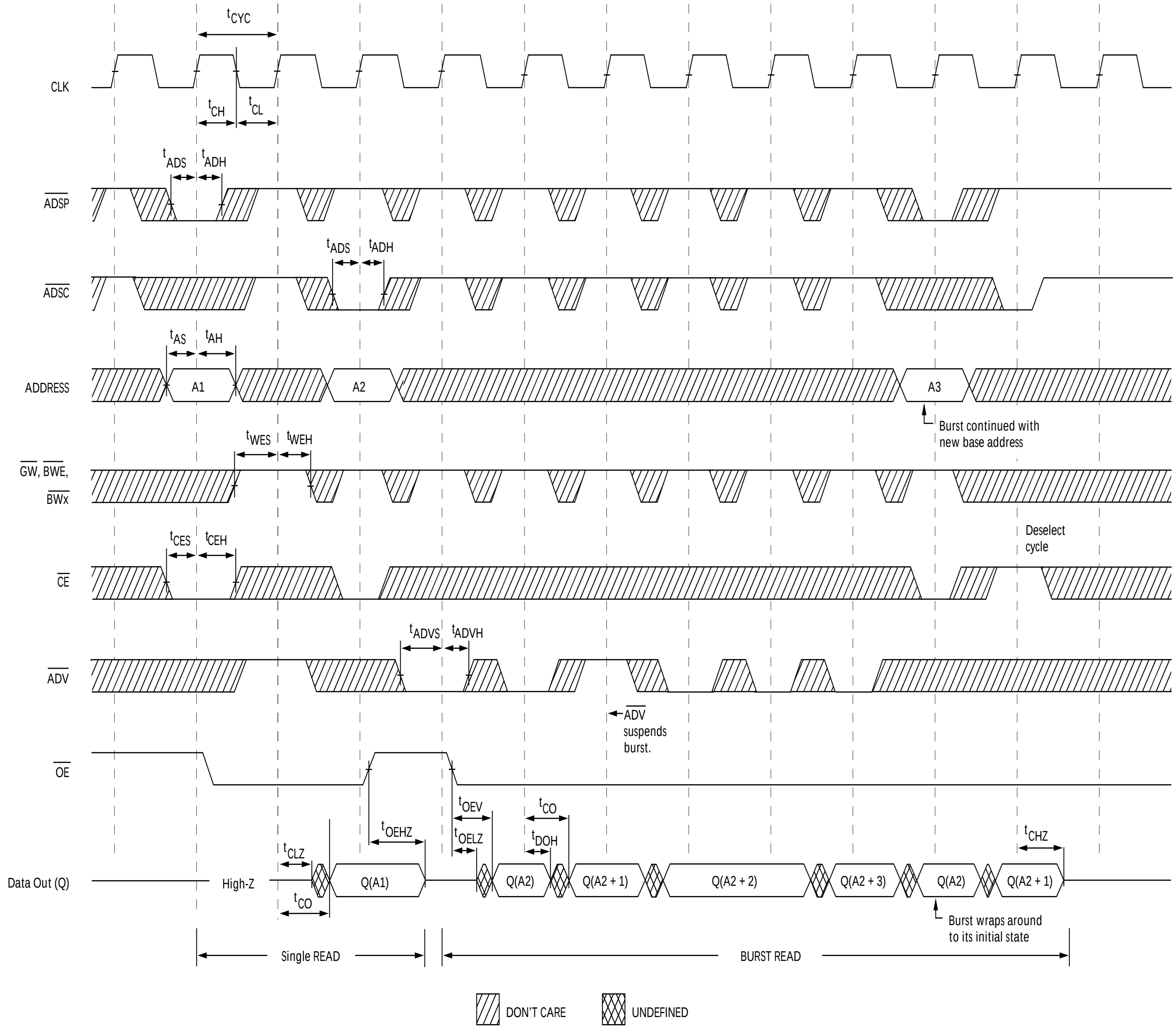
Shaded areas contain advance information.

Notes:

20. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially before a read or write operation can be initiated.
21. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
22. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions
23. This parameter is sampled and not 100% tested.
24. Timing reference level is 1.5V when V_{DDQ} = 3.3V and is 1.25V when V_{DDQ} = 2.5V.
25. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

Switching Waveforms

Read Cycle Timing[26]

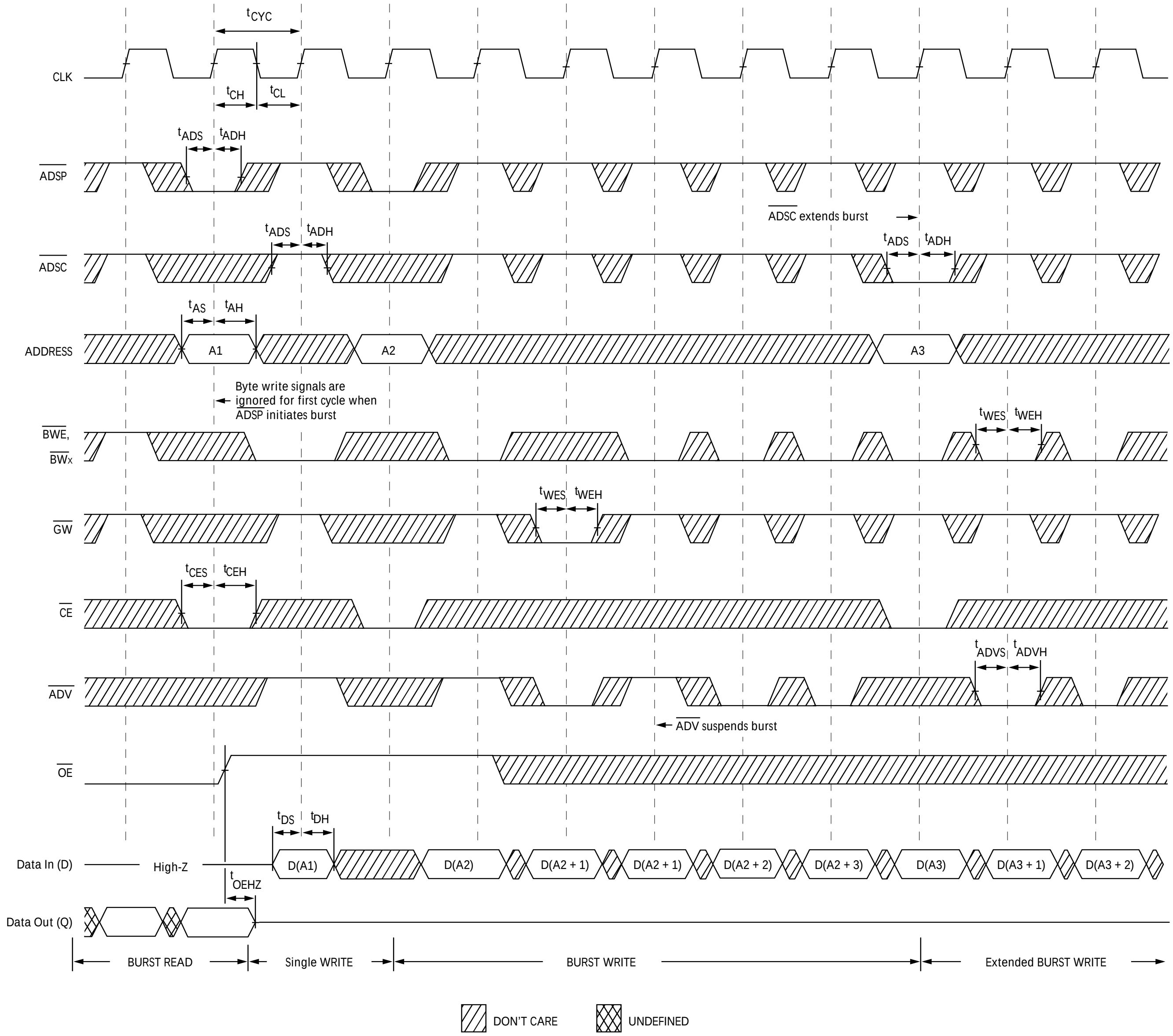


Notes:

26. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
27. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW.

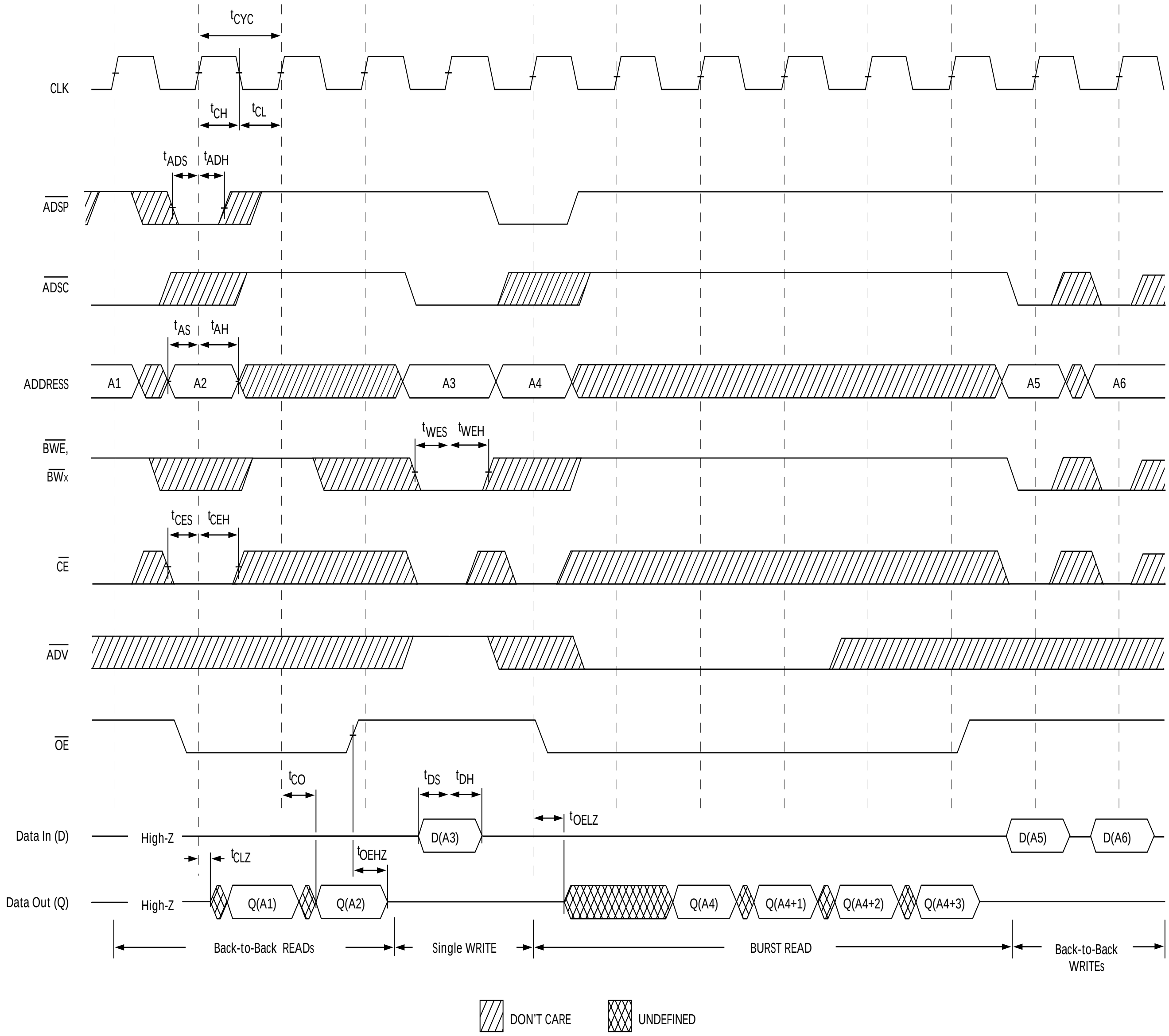
Switching Waveforms (continued)

Write Cycle Timing[26, 27]



Switching Waveforms (continued)

Read/Write Cycle Timing[26, 28, 29]

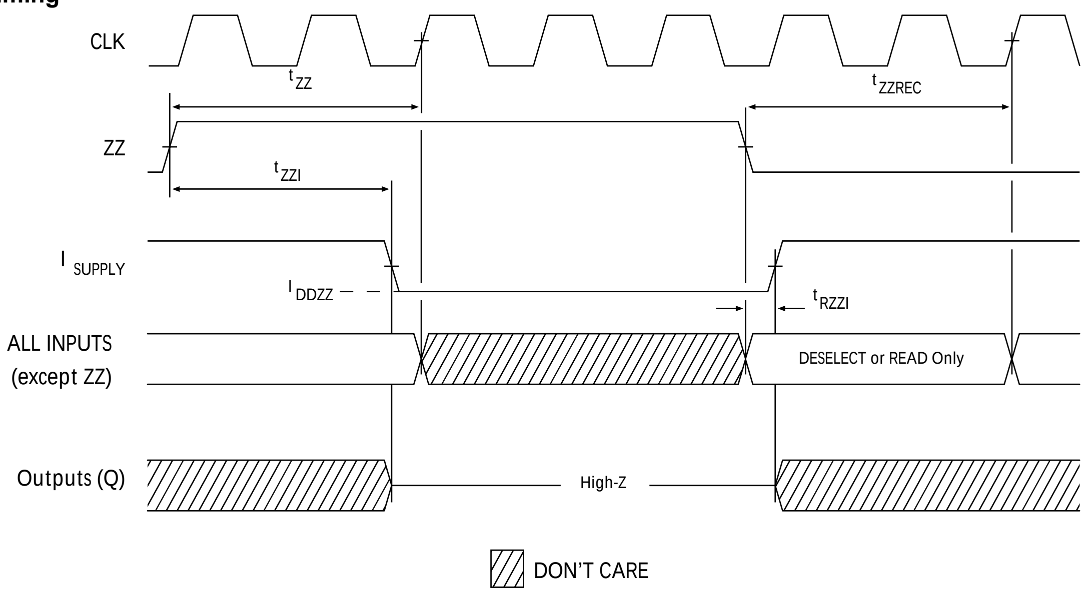


Notes:

28. The data bus (Q) remains in high-Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
29. GW is HIGH.

Switching Waveforms (continued)

ZZ Mode Timing [30, 31]



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Part and Package Type	Operating Range
250	CY7C1380D-250AXC CY7C1382D-250AXC	A101	Lead-Free 100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	Commercial
	CY7C1380D-250BGC CY7C1382D-250BGC	BG119	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1380D-250BZC CY7C1382D-250BZC	BB165D	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1380D-250BGXC CY7C1382D-250BGXC	BG119	Lead-Free 119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1380D-250BZXC CY7C1382D-250BZXC	BB165D	Lead-Free 165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
200	CY7C1380D-200AXC CY7C1382D-200AXC	A101	Lead-Free 100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	
	CY7C1380D-200BGC CY7C1382D-200BGC	BG119	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1380D-200BZC CY7C1382D-200BZC	BB165D	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1380D-200BGXC CY7C1382D-200BGXC	BG119	Lead-Free 119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1380D-200BZXC CY7C1382D-200BZXC	BB165D	Lead-Free 165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
167	CY7C1380D-167AXC CY7C1382D-167AXC	A101	Lead-Free 100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	
	CY7C1380D-167BGC CY7C1382D-167BGC	BG119	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1380D-167BZC CY7C1382D-167BZC	BB165D	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	

Ordering Information (continued)

Speed (MHz)	Ordering Code	Package Name	Part and Package Type	Operating Range
	CY7C1380D-167BGXC CY7C1382D-167BGXC	BG119	Lead-Free 119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1380D-167BZXC CY7C1382D-167BZXC	BB165D	Lead-Free 165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
167	CY7C1380D-167AXI CY7C1382D-167AXI	A101	Lead-Free 100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm)	Industrial
	CY7C1380D-167BGI CY7C1382D-167BGI	BG119	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1380D-167BZI CY7C1382D-167BZI	BB165D	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1380D-167BGXI CY7C1382D-167BGXI	BG119	Lead-Free 119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1380D-167BZXI CY7C1382D-167BZXI	BB165D	Lead-Free 165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm)	

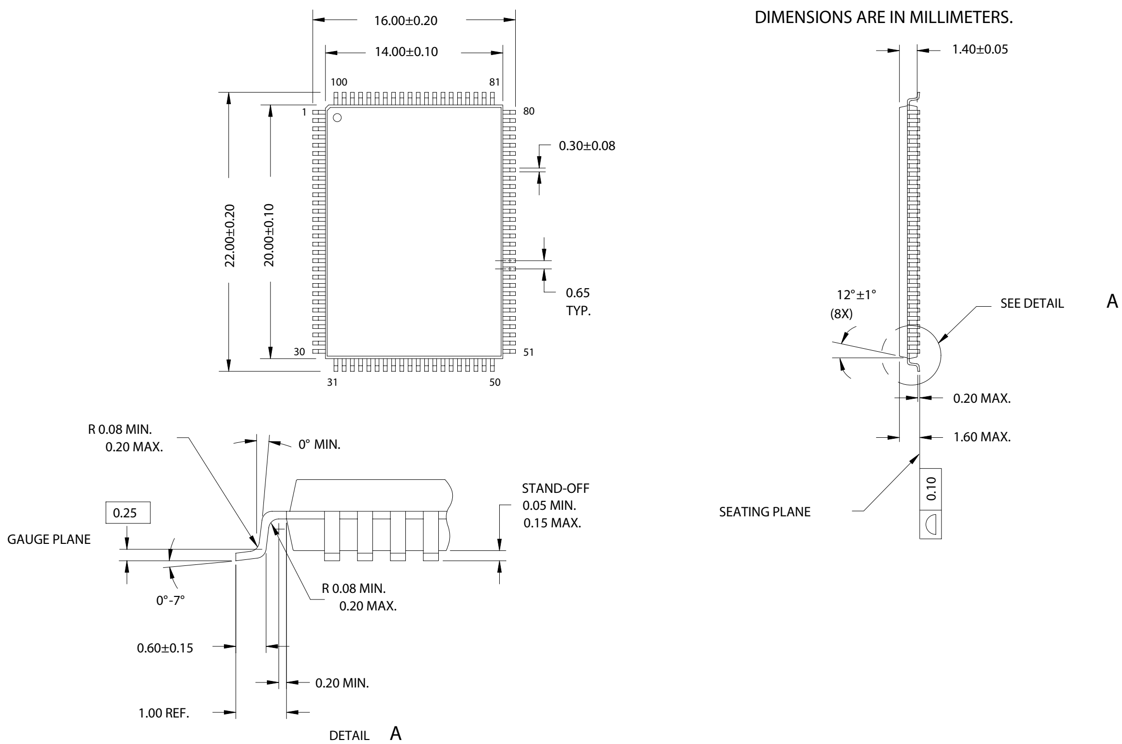
Shaded areas contain advance information. Please contact your local sales representative for availability of these parts. Lead-free BG packages (Ordering Code: BGX) will be available in 2005.

Notes:

30. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
31. DQs are in high-Z when exiting ZZ sleep mode.

Package Diagrams

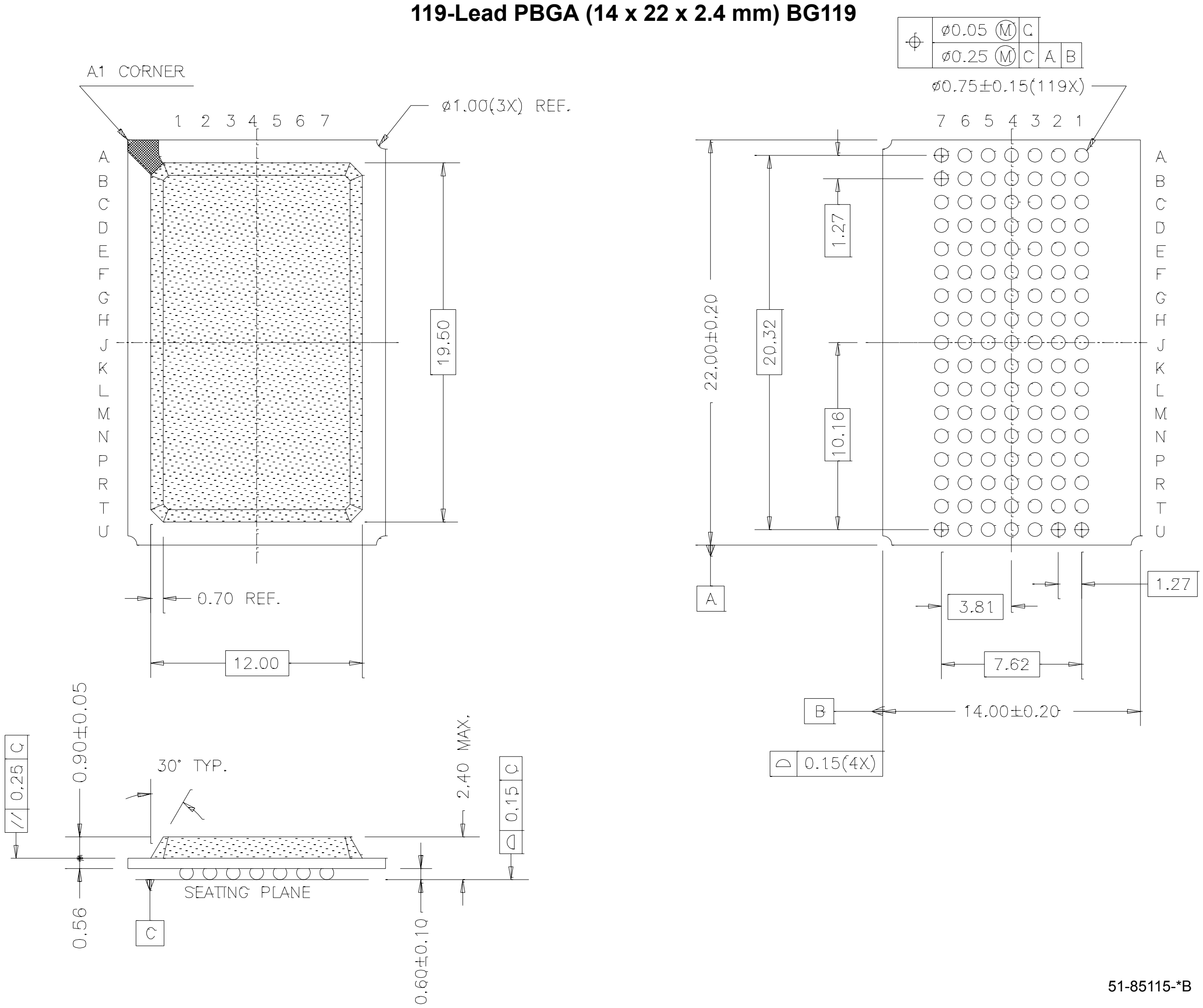
100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



51-85050-*A

Package Diagrams (continued)

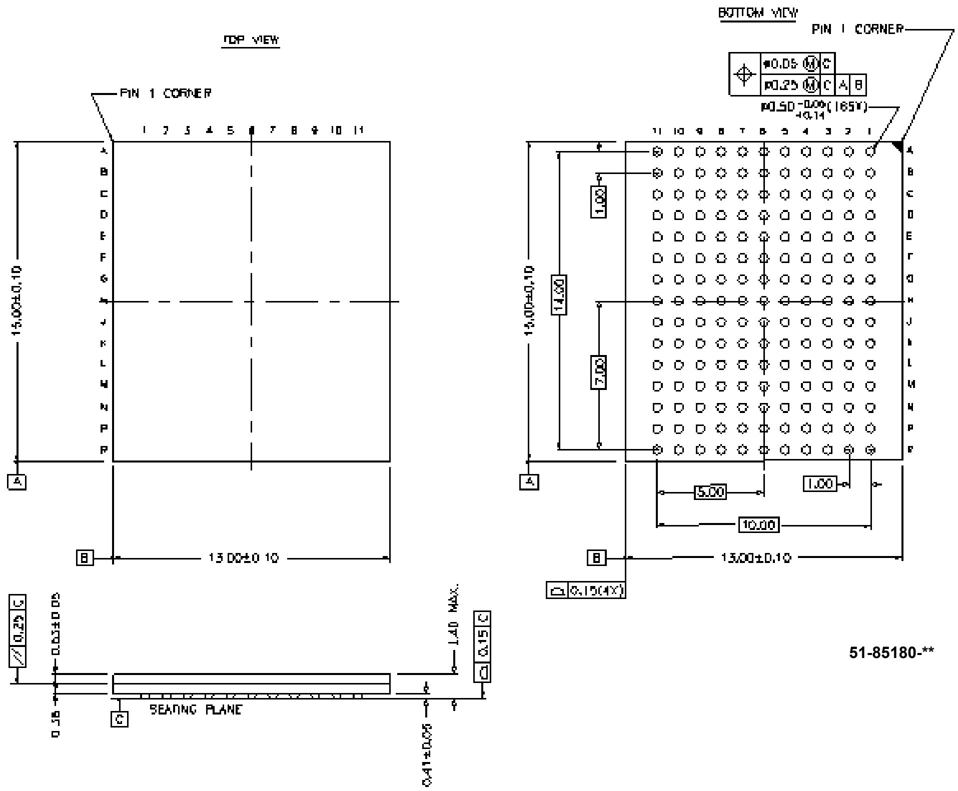
119-Lead PBGA (14 x 22 x 2.4 mm) BG119



51-85115-*B

Package Diagrams (continued)

165 FBGA 13 x 15 x 1.40 MM BB165D



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Document History Page

Document Title: CY7C1380D/CY7C1382D 18-Mbit (512K x 36/1M x 18) Pipelined SRAM Document Number: 38-05543				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	254515	See ECN	RKF	New data sheet
*A	288531	See ECN	SYT	Edited description under "IEEE 1149.1 Serial Boundary Scan (JTAG)" for non-compliance with 1149.1 Removed 225Mhz and 133Mhz Speed Bins Added lead-free information for 100-Pin TQFP , 119 BGA and 165 FBGA Packages Added comment of 'Lead-free BG packages availability' below the Ordering Information