Integrated Circuit Systems, Inc.

ICS9159-20

Frequency Generator for SIS551X and SIS6205 Chip Set Systems

General Description

The **ICS9159-20** is a low-cost frequency generator designed specifically for SIS551X chip set and SIS6205 VGA controller. The integrated buffer minimizes skew. A 14.31818 MHz XTAL oscillator provides the reference clock to generate standard Pentium™ frequencies. The CPU clock makes gradual frequency transitions without violating the PLL timing of internal microprocessor clock multipliers.

Both synchronous and asynchronous bus designs are supported. For chip sets that require an early CPU clock, the buffers are driven by the CPU clock. In this configuration, the CPU clock becomes the early clock and the output of the uncommitted buffers become the bus synchronized bus clocks.

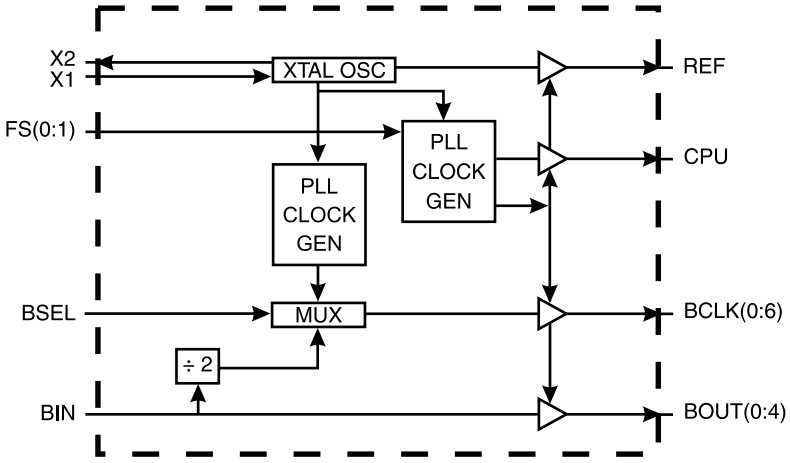
Features

- One selectable CPU clocks operate up to 66.66 MHz
- 5 uncommitted buffers
- Maximum CPU jitter of ±200ps
- 7 BUS clocks support sync or async bus operation
- 500ps skew window for all synchronous clock edges
- Integrated buffer outputs drive up to 30pF loads
- 3.1V - 3.5V supply range
- 28-pin 300-mil SOIC package
- Supports chip sets requiring early CPU clocking

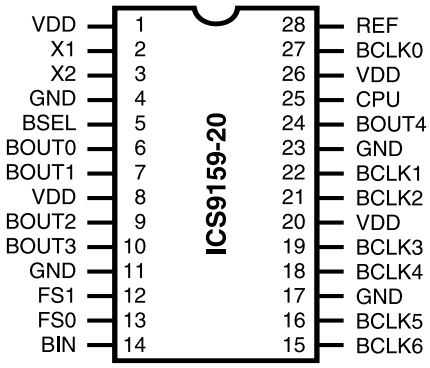
Applications

- Ideal for green Pentium and P6 PCI systems based on the SIS5596 chip set

Block Diagram



Pin Configuration



28-Pin SOIC

Functionality

3.3V±10%, 0-70°C
Crystal (X1, X2) = 14.318181 MHz

FS1	FS0	REF (MHz)	CPU (MHz)	BCLK (MHz) BSEL=1	BCLK (MHz) BSEL=0
0	0	Tistate	Tristate	Tristate	Tristate
0	1	14.318	50	25	33.33
1	0	14.318	60	30	33.33
1	1	14.318	66.66	33.33	33.33

All frequencies in MHz, assuming 14.318 MHz input.

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 8, 20, 26	VDD	PWR	Power for logic, PCLK and fixed frequency output buffers.
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12 - 16 MHz crystal, nominally 14.31818 MHz.
3	X2	OUT	XTAL output which includes XTAL load capacitance.
4, 11, 17, 23	GND	PWR	Ground for logic, PCLK and fixed frequency output buffers.
5	BSEL	IN	The DISK controller clock is fixed at 33 MHz (with 14.318 MHz input).
6, 7, 9, 10, 24	BOUT(0:4)	OUT	Uncommitted clock buffer outputs.
13, 12	FS(0:1)	IN	Frequency multiplier select pins. See table above. These inputs have internal pull-up devices. 14 BIN IN Uncommitted buffered inputs.
15, 16, 18, 19, 21, 22, 27	BCLK(0:6)	OUT	Bus clock outputs are fixed at 33.3 MHz or one half the CPU frequency. 25 CPU OUT Processor clock outputs which are a multiple of the input reference frequency as shown in the table above.
28	REF	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.

Note: BCLK buffers cannot be supplied with 5 volts (Pins 14 and 20) if CPU and fixed frequencies (Pins 1, 8 and 26) are being supplied with 3.3 volts.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-28.0	-10.5	-	µA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	-5.0	-	5.0	µA
Output Low Current[1]	I_{OL}	V_{OLT}=0.8V; for CPU, BOUT & BUS	30.0	47.0	-	mA
Output High Current[1]	I_{OH}	V_{OH}=2.0V; for CPU, BOUT & BUSes	-	-66.0	-42.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for REF CLKs	25.0	38.0	-	mA
Output High Current[1]	I_{OH}	V_{OH}=2.0V; for REF CLKs	-	-47.0	-30.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL}=15mA; for CPUs & BUSes	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA; for CPUs & BUSes	2.4	2.8	-	V
Output Low Voltage[1]	V_{OL}	I_{OL}=12.5mA; for REF CLKS	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-20mA; for REF CLKs	2.4	2.8	-	V
Supply Current	I_{DD}	@66.5 MHz; all outputs unloaded	-	90	150	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.1 – 3.7 V, T_A = 0 – 70° C

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V CPU, BOUT & BUS	-	0.9	1.5	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V CPU, BOUT & BUS	-	0.8	1.4	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% CPU, BOUT & BUS	-	1.5	2.5	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% CPU, BOUT & BUS	-	1.4	2.4	ns
Duty Cycle[1]	D_t	20pF load @j V_{OUT}=1.4V	45	50	55	%
Jitter, One Sigma[1]	T_{j1s1}	CPU Load=20pF Bin=EXTCLK	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	CPU Load=20pF Bin=EXTCLK	-250	-	250	ps
Jitter, One Sigma[1]	T_{j1s2}	BUS; Load=20pF	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	BUS; Load=20pF	-5	2	5	%
Input Frequency[1]	F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	t_{on}	From V_{DD}=1.6V to 1 st crossing of 66.5 MHz V_{DD} supply ramp < 40ms	-	2.5	4.5	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	2.0	4.0	ms
Clock Skew Window[1]	T_{sk1}	BOUT to BOUT; Load=20pF; @1.4V	-	150	250	ps
Clock Skew Window[1]	T_{sk2}	BUS to BUS; Load=20pF; @1.4V	-	300	500	ps
Clock Skew Window[1]	T_{sk3}	BOUT to BUS; Load=20pF; @1.4V	1	2.6	5	ps

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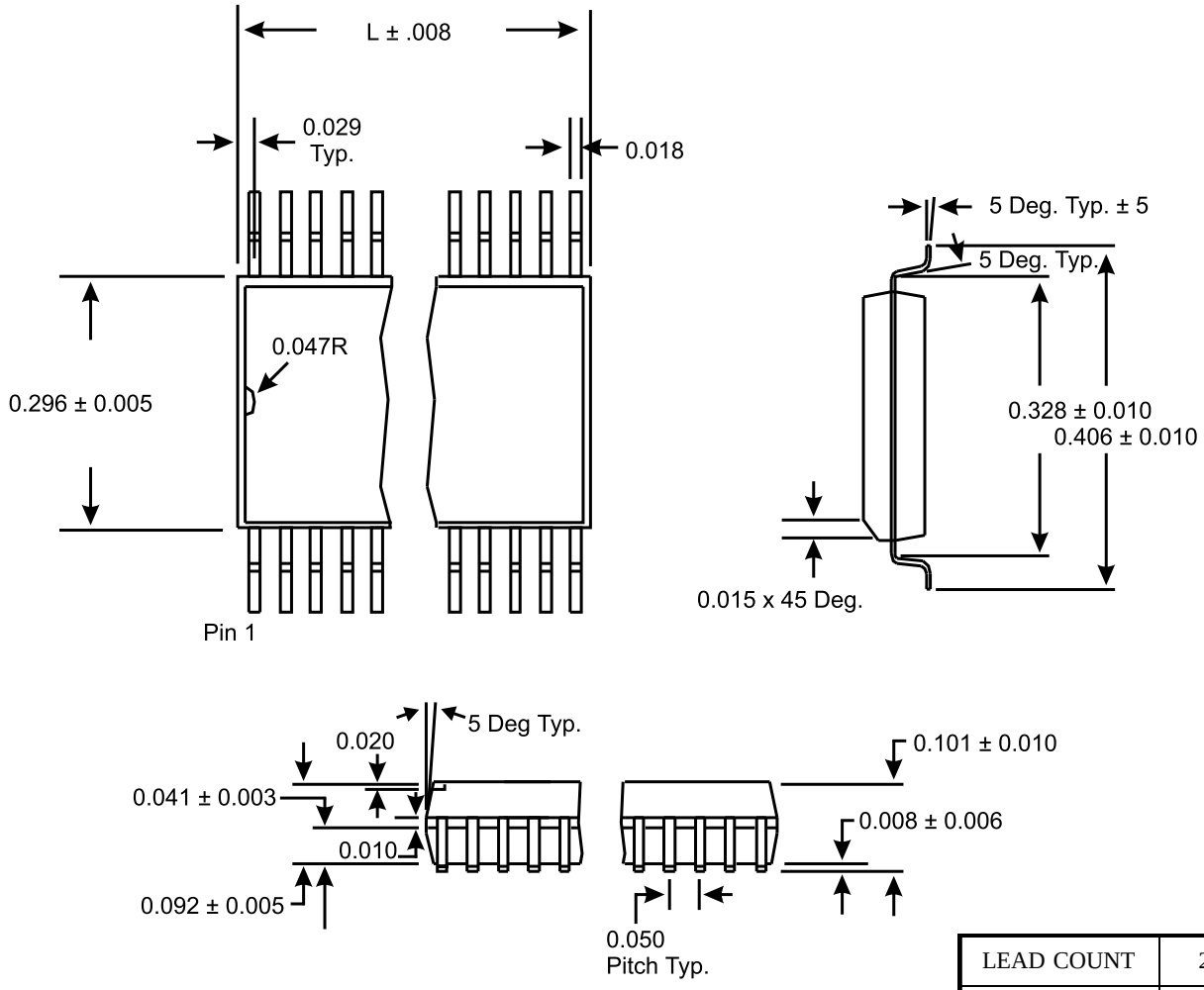

LEAD COUNT	28L
DIMENSIONL	0.704

SOIC Package

Ordering Information

ICS9159M-20

Example:

ICS XXXX M-PPP

- **Pattern Number(2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC, SOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS=Standard Device