



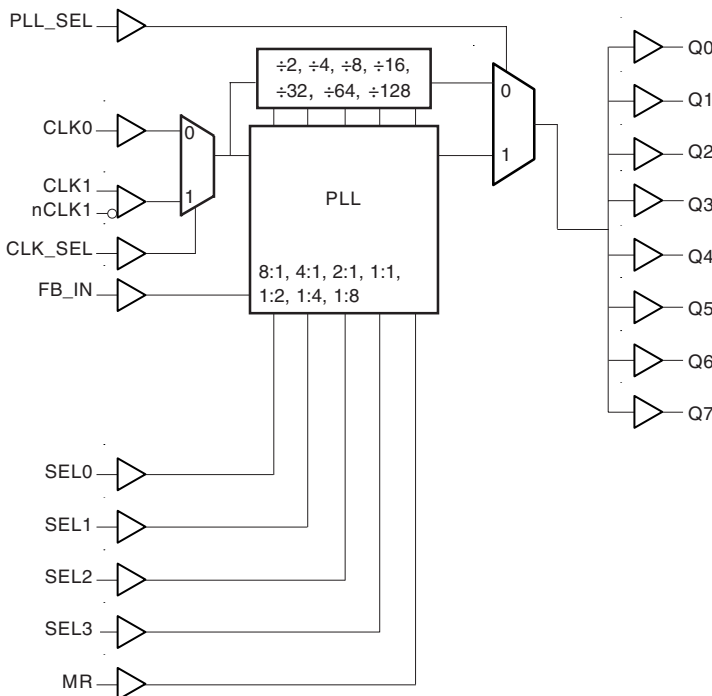
### GENERAL DESCRIPTION

The ICS8705 is a highly versatile 1:8 Differential-to-LVCMOS/LVTTL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8705 has two selectable clock inputs. The CLK1, nCLK1 pair can accept most standard differential input levels. The single ended CLK0 input accepts LVCMOS or LVTTL input levels. The ICS8705 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider and has an input and output frequency range of 15.625MHz to 250MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL\_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

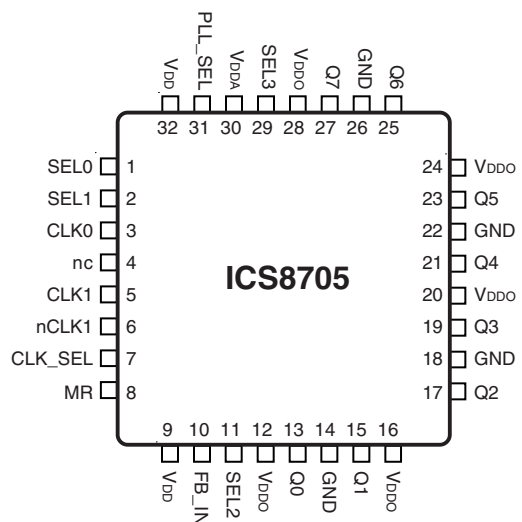
### FEATURES

- 8 LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Selectable CLK1, nCLK1 or LVCMOS/LVTTL clock inputs
- CLK1, nCLK1 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- CLK0 input accepts LVCMOS or LVTTL input levels
- Output frequency range: 15.625MHz to 250MHz
- Input frequency range: 15.625MHz to 250MHz
- VCO range: 250MHz to 500MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Fully integrated PLL
- Cycle-to-cycle jitter: 45ps (maximum)
- Output skew: CLK0, 65ps (maximum)  
CLK1, nCLK1, 55ps (maximum)
- Static Phase Offset: 25 ±125ps (maximum), CLK0
- Full 3.3V or 2.5V operating supply
- Lead-Free package available
- Industrial temperature information available upon request

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**32-Lead LQFP**

7mm x 7mm x 1.4 mm  
**Y Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

| Number                         | Name                           | Type   |          | Description   |
|--------------------------------|--------------------------------|--------|----------|---|
| 1, 2, 11                       | SEL0, SEL1, SEL2               | Input  | Pulldown | Determines output divider values in Table 3. LVCMOS/LVTTL interface levels.   |
| 3                              | CLK0                           | Input  | Pulldown | Clock input. LVCMOS/LVTTL interface levels.   |
| 4                              | nc                             |        |          | No connect.   |
| 5                              | CLK1                           | Input  | Pulldown | Non-inverting differential clock input.   |
| 6                              | nCLK1                          | Input  | Pullup   | Inverting differential clock input.   |
| 7                              | CLK_SEL                        | Input  | Pulldown | Clock select input. When HIGH, selects differential CLK1, nCLK1. When LOW, selects LVCMOS CLK0. LVCMOS/LVTTL interface levels.  |
| 8                              | MR                             | Input  | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 9, 32                          | V <sub>DD</sub>                | Power  |          | Core supply pins.   |
| 10                             | FB_IN                          | Input  | Pulldown | LVCMOS/LVTTL feedback input to phase detector for regenerating clocks with "zero delay". Connect to one of the outputs. LVCMOS/LVTTL interface levels.  |
| 12, 16, 20, 24, 28             | V <sub>DDO</sub>               | Power  |          | Output supply pins.   |
| 13, 15, 17, 19, 21, 23, 25, 27 | Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | Output |          | Clock output. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.   |
| 14, 18, 22, 26                 | GND                            | Power  |          | Power supply ground.  |
| 29                             | SEL3                           | Input  | Pulldown | Determines output divider values in Table 3. LVCMOS/LVTTL interface levels.   |
| 30                             | V <sub>DDA</sub>               | Power  |          | Analog supply pin.  |
| 31                             | PLL_SEL                        | Input  | Pullup   | Selects between the PLL and reference clock as input to the dividers. When LOW, selects the reference clock (PLL Bypass). When HIGH, selects PLL (PLL Enabled). LVCMOS/LVTTL interface levels.              |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol                | Parameter                                  | Test Conditions  | Minimum | Typical | Maximum | Units |
|-----------------------|--|--|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance                          |  |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor                      |  |         | 51      |         | KΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor                    |  |         | 51      |         | KΩ    |
| C <sub>PD</sub>       | Power Dissipation Capacitance (per output) | V <sub>DD</sub> , V <sub>DDO</sub> , V <sub>DDA</sub> = 3.465V |         | 23      |         | pF    |
| R <sub>OUT</sub>      | Output Impedance                           |  |         | 7       |         | Ω     |



**TABLE 3A. PLL ENABLE FUNCTION TABLE**

| Inputs |      |      |      |                                 | Outputs<br>PLL_SEL = 1<br>PLL Enable Mode |
|--------|------|------|------|---------------------------------|---|
| SEL3   | SEL2 | SEL1 | SEL0 | Reference Frequency Range (MHz) | Q0:Q7                                     |
| 0      | 0    | 0    | 0    | 125 - 250                       | ÷ 1                                       |
| 0      | 0    | 0    | 1    | 62.5 - 125                      | ÷ 1                                       |
| 0      | 0    | 1    | 0    | 31.25 - 62.5                    | ÷ 1                                       |
| 0      | 0    | 1    | 1    | 15.625 - 31.25                  | ÷ 1                                       |
| 0      | 1    | 0    | 0    | 125 - 250                       | ÷ 2                                       |
| 0      | 1    | 0    | 1    | 62.5 - 125                      | ÷ 2                                       |
| 0      | 1    | 1    | 0    | 31.25 - 62.5                    | ÷ 2                                       |
| 0      | 1    | 1    | 1    | 125 - 250                       | ÷ 4                                       |
| 1      | 0    | 0    | 0    | 62.5 - 125                      | ÷ 4                                       |
| 1      | 0    | 0    | 1    | 125 - 250                       | ÷ 8                                       |
| 1      | 0    | 1    | 0    | 62.5 - 125                      | x 2                                       |
| 1      | 0    | 1    | 1    | 31.25 - 62.5                    | x 2                                       |
| 1      | 1    | 0    | 0    | 15.625 - 31.25                  | x 2                                       |
| 1      | 1    | 0    | 1    | 31.25 - 62.5                    | x 4                                       |
| 1      | 1    | 1    | 0    | 15.625 - 31.25                  | x 4                                       |
| 1      | 1    | 1    | 1    | 15.625 - 31.25                  | x 8                                       |

**TABLE 3B. PLL BYPASS FUNCTION TABLE**

| Inputs |      |      |      | Outputs<br>PLL_SEL = 0<br>PLL Bypass Mode |
|--------|------|------|------|---|
| SEL3   | SEL2 | SEL1 | SEL0 | Q0:Q7                                     |
| 0      | 0    | 0    | 0    | ÷ 8                                       |
| 0      | 0    | 0    | 1    | ÷ 8                                       |
| 0      | 0    | 1    | 0    | ÷ 8                                       |
| 0      | 0    | 1    | 1    | ÷ 16                                      |
| 0      | 1    | 0    | 0    | ÷ 16                                      |
| 0      | 1    | 0    | 1    | ÷ 16                                      |
| 0      | 1    | 1    | 0    | ÷ 32                                      |
| 0      | 1    | 1    | 1    | ÷ 32                                      |
| 1      | 0    | 0    | 0    | ÷ 64                                      |
| 1      | 0    | 0    | 1    | ÷ 128                                     |
| 1      | 0    | 1    | 0    | ÷ 4                                       |
| 1      | 0    | 1    | 1    | ÷ 4                                       |
| 1      | 1    | 0    | 0    | ÷ 8                                       |
| 1      | 1    | 0    | 1    | ÷ 2                                       |
| 1      | 1    | 1    | 0    | ÷ 4                                       |
| 1      | 1    | 1    | 1    | ÷ 2                                       |



**ABSOLUTE MAXIMUM RATINGS**

|  |                           |
|--|---------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                      |
| Inputs, $V_i$                            | -0.5V to $V_{DD} + 0.5V$  |
| Outputs, $V_o$                           | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm)         |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C            |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDA}$ | Analog Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$  | Power Supply Current  |                 |         |         | 96      | mA    |
| $I_{DDA}$ | Analog Supply Current |                 |         |         | 15      | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         |         | 20      | mA    |

**TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol   | Parameter                   | Test Conditions  | Minimum | Typical | Maximum        | Units   |
|----------|-----------------------------|--|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage          | PLL_SEL, CLK_SEL, SEL0, SEL1, SEL2, SEL3, FB_IN, MR                                | 2       |         | $V_{DD} + 0.3$ | V       |
|          |                             | CLK0   | 2       |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage           | PLL_SEL, CLK_SEL, SEL0, SEL1, SEL2, SEL3, FB_IN, MR                                | -0.3    |         | 0.8            | V       |
|          |                             | CLK0   | -0.3    |         | 1.3            | V       |
| $I_{IH}$ | Input High Current          | CLK0, CLK_SEL, MR, FB_IN, SEL0, SEL1, SEL2, SEL3<br>$V_{DD} = V_{IN} = 3.465V$     |         |         | 150            | $\mu A$ |
|          |                             | PLL_SEL<br>$V_{DD} = V_{IN} = 3.465V$  |         |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current           | CLK0, CLK_SEL, MR, FB_IN, SEL0, SEL1, SEL2, SEL3<br>$V_{DD} = 3.465V, V_{IN} = 0V$ | -5      |         |                | $\mu A$ |
|          |                             | PLL_SEL<br>$V_{DD} = 3.465V, V_{IN} = 0V$  | -150    |         |                | $\mu A$ |
| $V_{OH}$ | Output High Voltage; NOTE 1 |  | 2.6     |         |                | V       |
| $V_{OL}$ | Output Low Voltage; NOTE 1  |  |         |         | 0.5            | V       |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . In the Parameter Measurement Information Section, see "3.3V Output Load Test Circuit".



**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter                               | Test Conditions | Minimum                        | Typical | Maximum         | Units   |
|-----------|---|-----------------|--------------------------------|---------|-----------------|---------|
| $I_{IH}$  | Input High Current                      | CLK1            | $V_{DD} = V_{IN} = 3.465V$     |         | 150             | $\mu A$ |
|           |   | nCLK1           | $V_{DD} = V_{IN} = 3.465V$     |         | 5               | $\mu A$ |
| $I_{IL}$  | Input Low Current                       | CLK1            | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5      |                 | $\mu A$ |
|           |   | nCLK1           | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150    |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage              |                 | 0.15                           |         | 1.3             | V       |
| $V_{CMR}$ | Common Mode Input Voltage;<br>NOTE 1, 2 |                 | GND + 0.5                      |         | $V_{DD} - 0.85$ | V       |

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for CLK1, nCLK1 is  $V_{DD} + 0.3V$ .

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol        | Parameter                                 | Test Conditions                                       | Minimum   | Typical | Maximum | Units |    |
|---------------|---|---|---|---------|---------|-------|----|
| $f_{MAX}$     | Output Frequency                          |   | 15.625  |         | 250     | MHz   |    |
| $t_{pLH}$     | Propagation Delay,<br>Low-to-High; NOTE 1 | CLK0  | PLL_SEL = 0V,<br>$f \leq 250MHz, Qx \div 2$         | 5       |         | 7     | ns |
|               |   | CLK1, nCLK1   | PLL_SEL = 0V,<br>$f \leq 250MHz, Qx \div 2$         | 5       |         | 7.3   | ns |
| $t(\theta)$   | Static Phase Offset;<br>NOTE 2, 4         | CLK0  | PLL_SEL = 3.3V,<br>$f_{REF} \leq 200MHz, Qx \div 1$ | -100    | 25      | 150   | ps |
|               |   | CLK1, nCLK1   | PLL_SEL = 3.3V,<br>$f_{REF} \leq 167MHz, Qx \div 1$ | -15     | +135    | 285   | ps |
|               |   |   | PLL_SEL = 3.3V,<br>$f_{REF} = 200MHz, Qx \div 1$    | -50     | +100    | 250   | ps |
|               |   | CLK0  | PLL_SEL = 3.3V,<br>$f_{REF} = 66MHz, Qx * 2$        | -150    | -25     | 100   | ps |
|               |   | CLK1, nCLK1   | PLL_SEL = 3.3V,<br>$f_{REF} = 66MHz, Qx * 2$        | 0       | 150     | 300   | ps |
| $t_{sk(o)}$   | Output Skew;<br>NOTE 3, 4                 | CLK0  | PLL_SEL = 0V  |         |         | 65    | ps |
|               |   | CLK1, nCLK1   | PLL_SEL = 0V  |         |         | 55    | ps |
| $t_{jit(cc)}$ | Cycle-to-Cycle Jitter; NOTE 4             | $f_{OUT} > 40MHz$                                     |   |         | 45      | ps    |    |
| $t_L$         | PLL Lock Time                             |   |   |         | 1       | mS    |    |
| $t_R / t_F$   | Output Rise/Fall Time                     |   | 400   |         | 950     | ps    |    |
| odc           | Output Duty Cycle                         |   | 43  |         | 57      | %     |    |
|               |   | PLL x 4 mode, $f_{in} = 45MHz,$<br>$f_{OUT} = 180MHz$ | 47  |         | 53      | %     |    |

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at  $V_{DDO}/2$ .

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



**TABLE 4D. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDA}$ | Analog Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$  | Power Supply Current  |                 |         |         | 90      | mA    |
| $I_{DDA}$ | Analog Supply Current |                 |         |         | 15      | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         |         | 20      | mA    |

**TABLE 4E. LVCMOS / LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol   | Parameter                   | Test Conditions                                     | Minimum                        | Typical | Maximum        | Units   |
|----------|-----------------------------|---|--------------------------------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage          | PLL_SEL, CLK_SEL, SEL0, SEL1, SEL2, SEL3, FB_IN, MR | 2                              |         | $V_{DD} + 0.3$ | V       |
|          |                             | CLK0  | 2                              |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage           | PLL_SEL, CLK_SEL, SEL0, SEL1, SEL2, SEL3, FB_IN, MR | -0.3                           |         | 0.8            | V       |
|          |                             | CLK0  | -0.3                           |         | 1.3            | V       |
| $I_{IH}$ | Input High Current          | CLK0, CLK_SEL, MR, FB_IN, SEL0, SEL1, SEL2, SEL3    | $V_{DD} = V_{IN} = 2.625V$     |         | 150            | $\mu A$ |
|          |                             | PLL_SEL   | $V_{DD} = V_{IN} = 2.625V$     |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current           | CLK0, CLK_SEL, MR, FB_IN, SEL0, SEL1, SEL2, SEL3    | $V_{DD} = 2.625V, V_{IN} = 0V$ | -5      |                | $\mu A$ |
|          |                             | PLL_SEL   | $V_{DD} = 2.625V, V_{IN} = 0V$ | -150    |                | $\mu A$ |
| $V_{OH}$ | Output High Voltage; NOTE 1 |   | 1.8                            |         |                | V       |
| $V_{OL}$ | Output Low Voltage; NOTE 1  |   |                                |         | 0.5            | V       |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . In the Parameter Measurement Information section, see "2.5V Output Load Test Circuit" figure.

**TABLE 4F. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter                            | Test Conditions | Minimum                        | Typical | Maximum         | Units   |
|-----------|--------------------------------------|-----------------|--------------------------------|---------|-----------------|---------|
| $I_{IH}$  | Input High Current                   | CLK1            | $V_{DD} = V_{IN} = 2.625V$     |         | 150             | $\mu A$ |
|           |                                      | nCLK1           | $V_{DD} = V_{IN} = 2.625V$     |         | 5               | $\mu A$ |
| $I_{IL}$  | Input Low Current                    | CLK1            | $V_{DD} = 2.625V, V_{IN} = 0V$ | -5      |                 | $\mu A$ |
|           |                                      | nCLK1           | $V_{DD} = 2.625V, V_{IN} = 0V$ | -150    |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage           |                 | 0.15                           |         | 1.3             | V       |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 |                 | GND + 0.5                      |         | $V_{DD} - 0.85$ | V       |

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for CLK1, nCLK1 is  $V_{DD} + 0.3V$ .



**TABLE 5B. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol            | Parameter                                 | Test Conditions  | Minimum   | Typical | Maximum  | Units |    |
|-------------------|---|--|---|---------|----------|-------|----|
| $f_{MAX}$         | Output Frequency                          |  | 15.625  |         | 250      | MHz   |    |
| $t_{pLH}$         | Propagation Delay,<br>Low-to-High; NOTE 1 | CLK0   | PLL_SEL = 0V,<br>$f \leq 250MHz$ , $Q_x \div 2$         | 5       |          | 7     | ns |
|                   |   | CLK1, nCLK1  | PLL_SEL = 0V,<br>$f \leq 250MHz$ , $Q_x \div 2$         | 5       |          | 7.3   | ns |
| $t(\theta)$       | Static Phase Offset;<br>NOTE 2, 4         | CLK0   | PLL_SEL = 2.5V,<br>$f_{REF} \leq 200MHz$ , $Q_x \div 1$ | -250    | 25       | 200   | ps |
|                   |   | CLK1, nCLK1  | PLL_SEL = 2.5V,<br>$f_{REF} = 133MHz$ , $Q_x \div 1$    | -50     | 100      | 250   | ps |
|                   |   |  | PLL_SEL = 2.5V,<br>$f_{REF} = 200MHz$ , $Q_x \div 1$    | -100    | +100     | 300   | ps |
|                   |   | CLK1, nCLK1  | PLL_SEL = 2.5V,<br>$f_{REF} = 66MHz$ , $Q_x * 2$        | 0       | 150      | 300   | ps |
| $t_{sk(o)}$       | Output Skew;<br>NOTE 3, 4                 | CLK0   | PLL_SEL = 0V  |         |          | 65    | ps |
|                   |   | CLK1, nCLK1  | PLL_SEL = 0V  |         |          | 55    | ps |
| $f_{jit(cc)}$     | Cycle-to-Cycle Jitter; NOTE 4             | $f_{OUT} > 40MHz$                                      |   |         | 45       | ps    |    |
| $f_{jit(\theta)}$ | Phase Jitter; NOTE 4, 5                   | PLL_SEL = 2.5V,<br>$f_{REF} = 66MHz$ , $Q_x * 2$       |   |         | $\pm 50$ | ps    |    |
| $t_L$             | PLL Lock Time                             |  |   |         | 1        | mS    |    |
| $t_R / t_F$       | Output Rise/Fall Time                     |  | 400   |         | 950      | ps    |    |
| odc               | Output Duty Cycle                         |  | 43  |         | 57       | %     |    |
|                   |   | PLL x 4 mode, $f_{in} = 45MHz$ ,<br>$f_{OUT} = 180MHz$ | 45  |         | 55       | %     |    |

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at  $V_{DDO}/2$ .

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

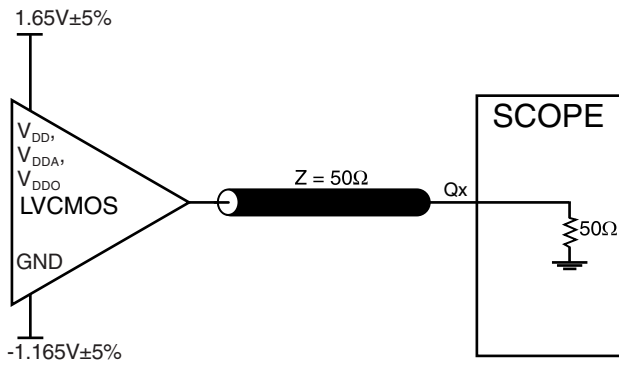
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

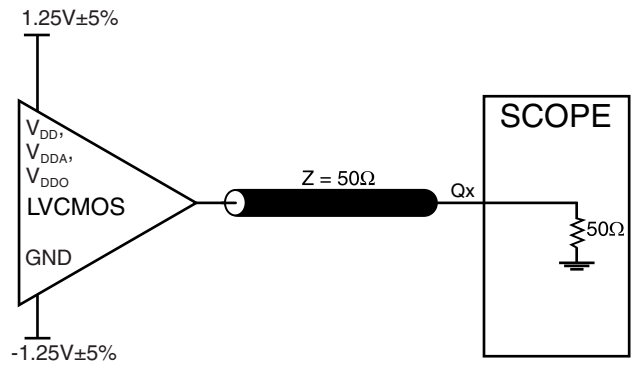
NOTE 5: Phase jitter is dependent on the input source used.



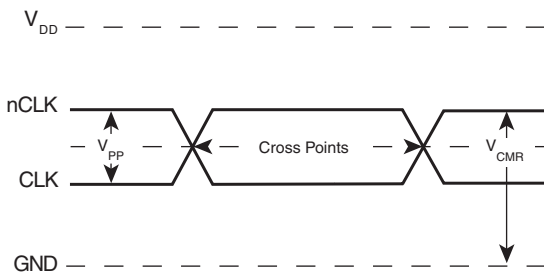
## PARAMETER MEASUREMENT INFORMATION



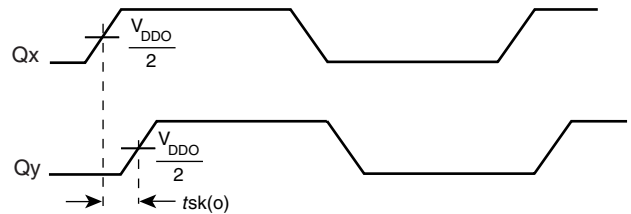
**3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT**



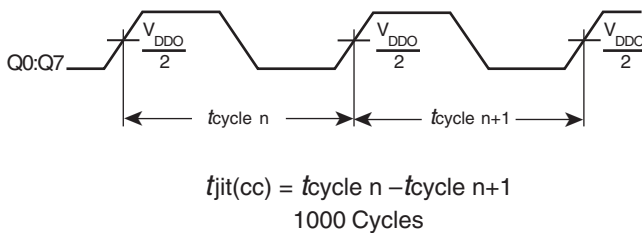
**2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



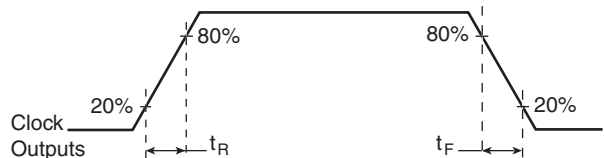
**DIFFERENTIAL INPUT LEVEL**



**OUTPUT SKEW**

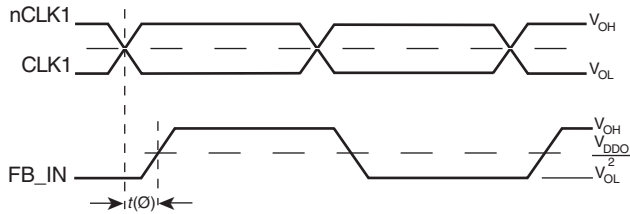


**CYCLE-TO-CYCLE JITTER**



**OUTPUT RISE/FALL TIME**

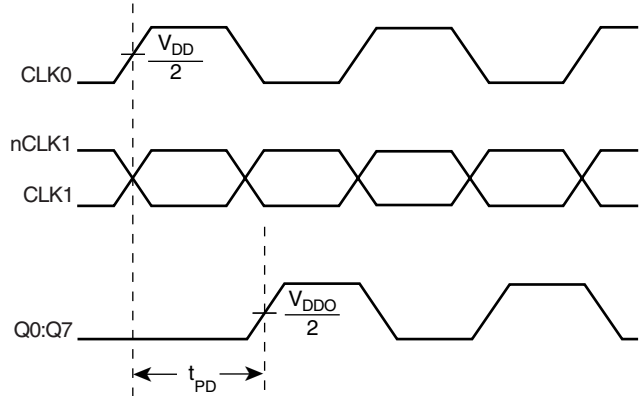




$$f_{jit}(\varnothing) = |t(\varnothing) - t(\varnothing)_{mean}| = \text{Phase Jitter}$$

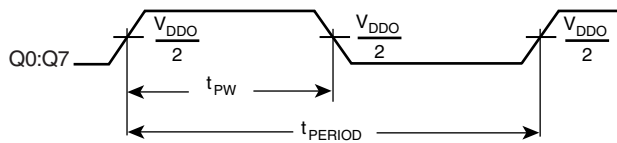
$$t(\varnothing)_{mean} = \text{Static Phase Offset}$$

(where  $t(\varnothing)$  is any random sample, and  $t(\varnothing)_{mean}$  is the average of the sampled cycles measured on controlled edges)



**PHASE JITTER & STATIC PHASE OFFSET**

**PROPAGATION DELAY**



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8705 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ , and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{DDA}$ .

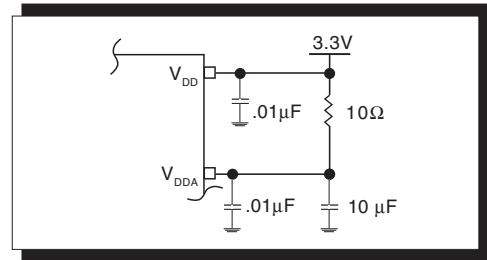


FIGURE 1. POWER SUPPLY FILTERING

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3\text{V}$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

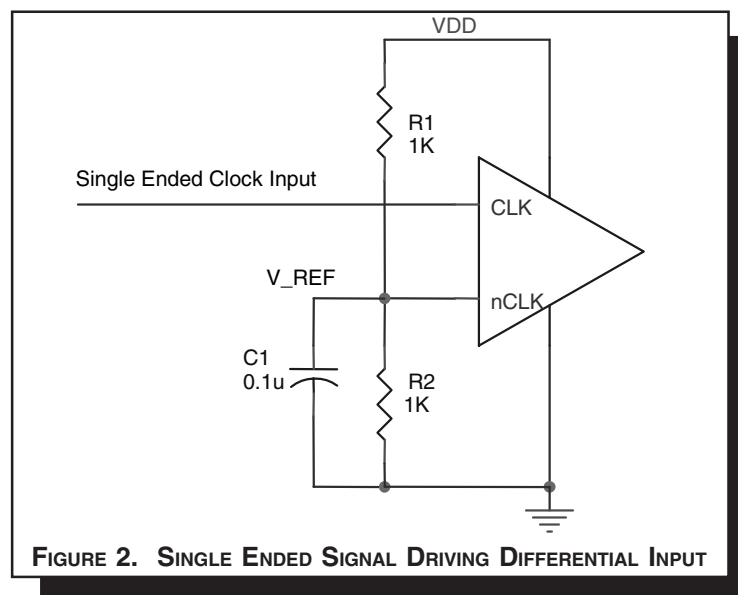


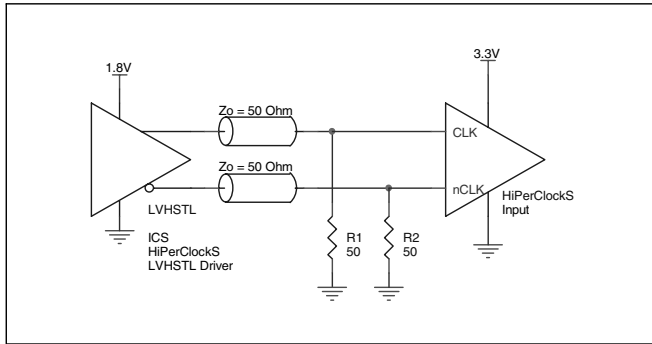
FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT



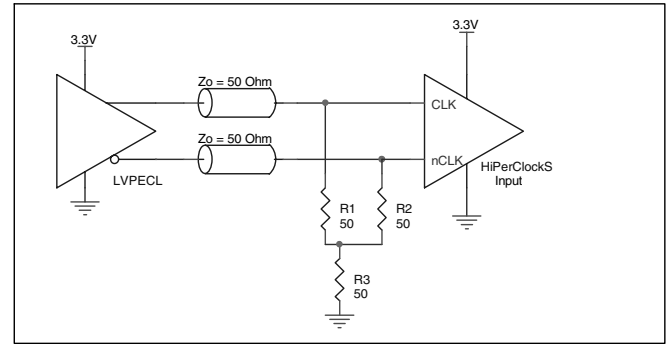
### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

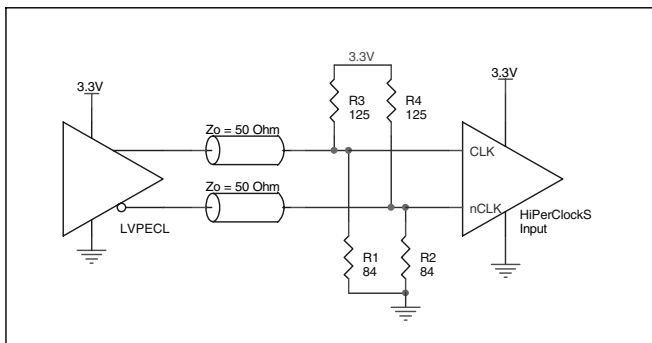
here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



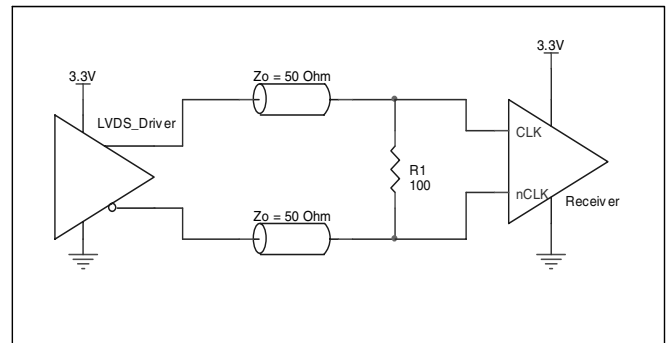
**FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER**



**FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



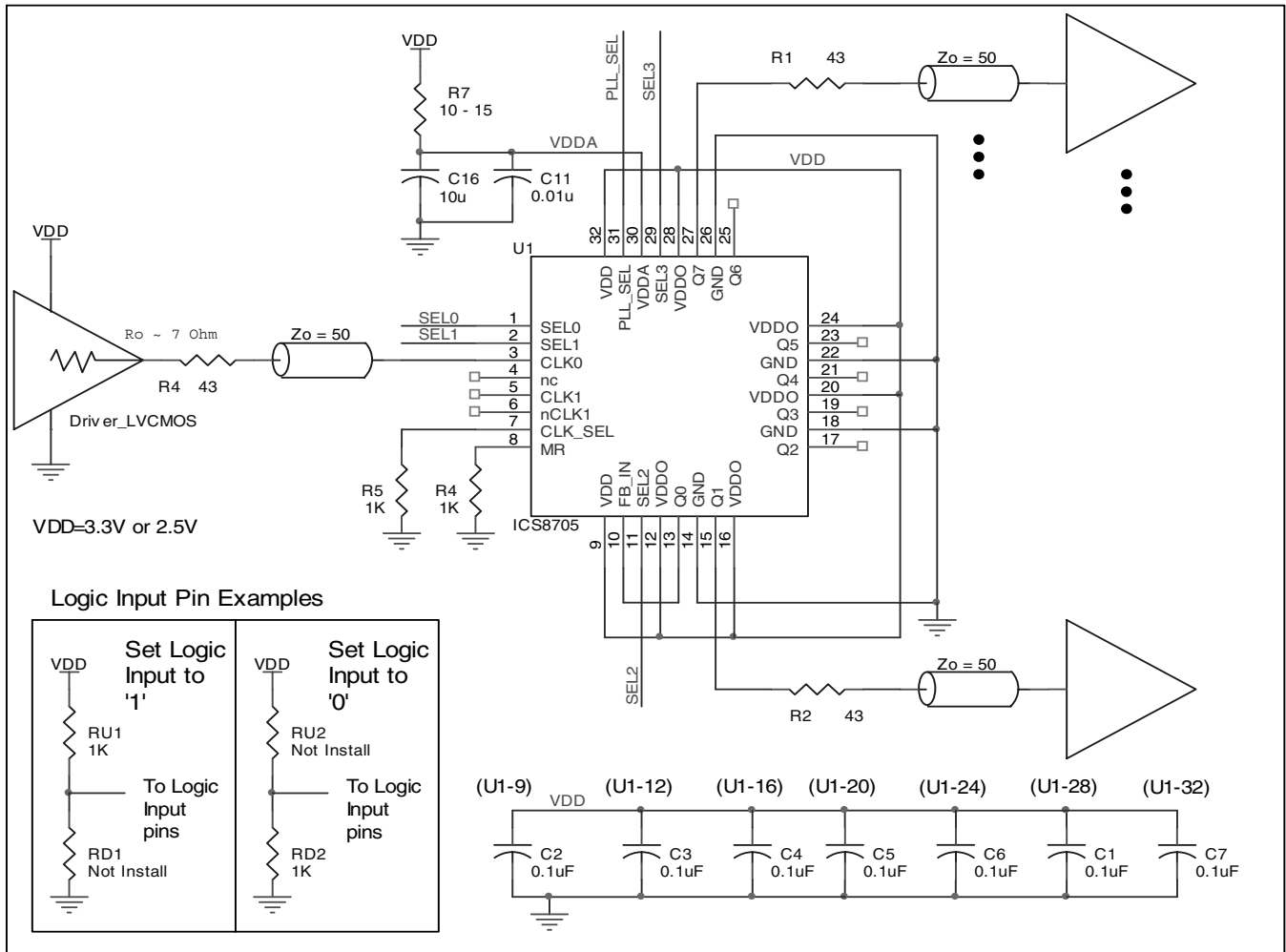
**FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



**LAYOUT GUIDELINE**

The schematic of the ICS8705 layout example is shown in *Figure 4A*. The ICS8705 recommended PCB board layout for this example is shown in *Figure 4B*. This layout example is used as a general guideline. The layout in the actual system will

depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.



**FIGURE 4A. ICS8705 LVC MOS CLOCK GENERATOR SCHEMATIC EXAMPLE**



The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

#### POWER AND GROUNDING

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the  $V_{DDA}$  pin as possible.

#### CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the

trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The series termination resistors should be located as close to the driver pins as possible.

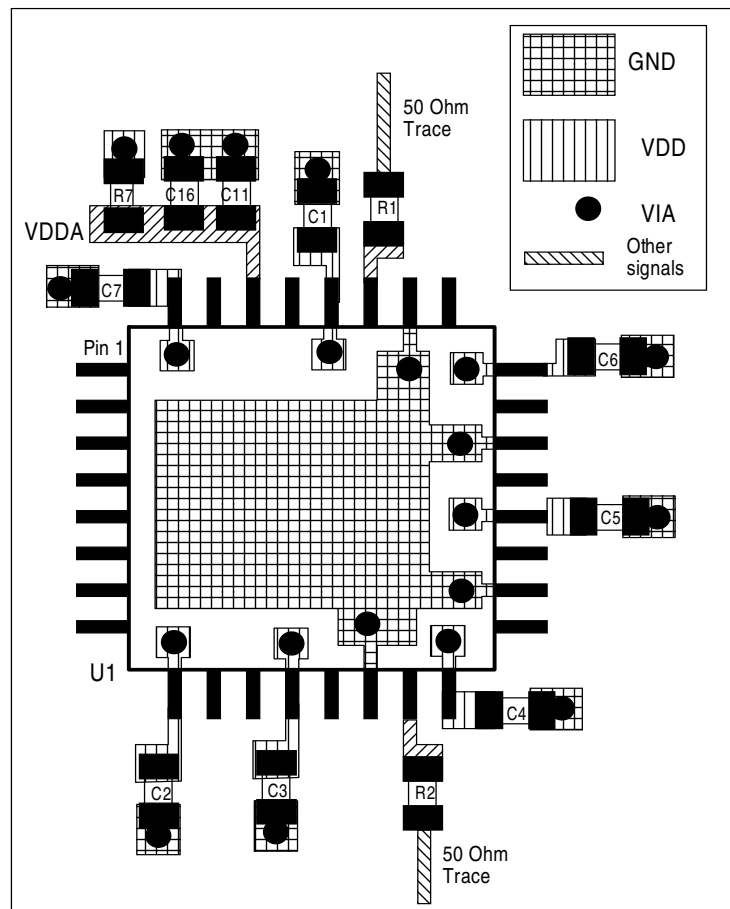


FIGURE 4B. PCB BOARD LAYOUT FOR ICS8705



## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 32 LEAD LQFP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |          |          |          |
|--|----------|----------|----------|
|  | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards       | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 47.9°C/W | 42.1°C/W | 39.4°C/W |

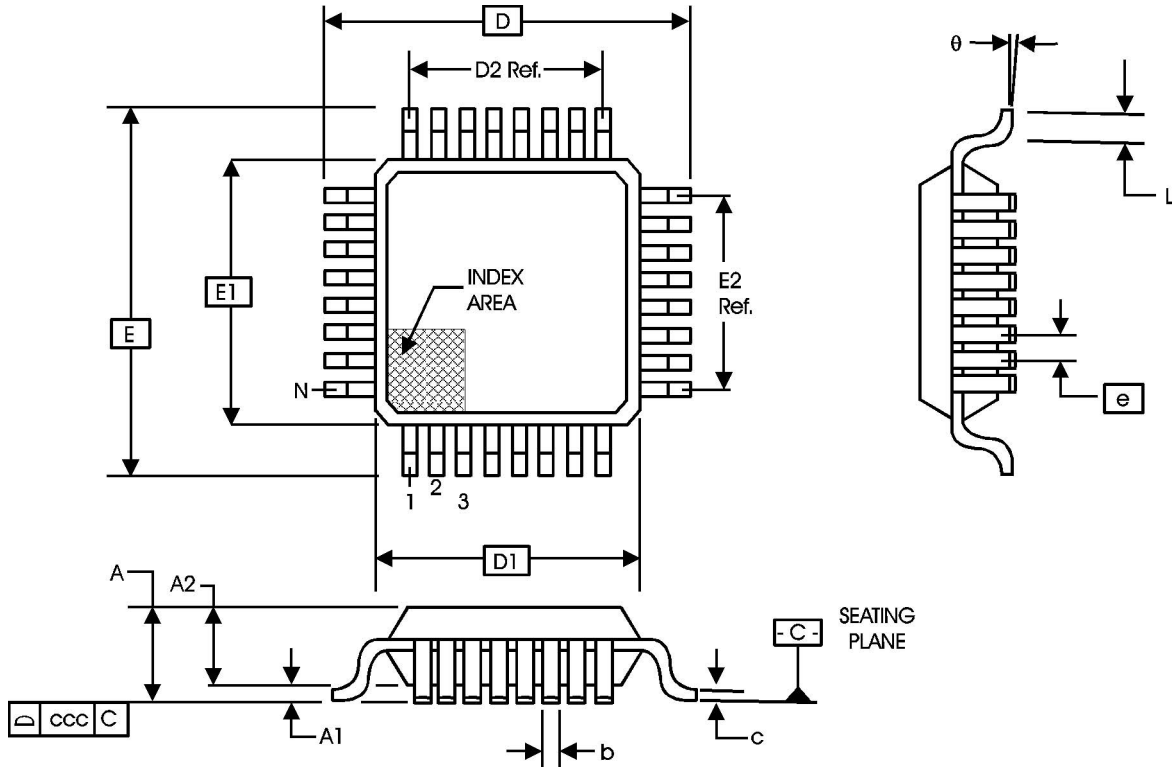
**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8705 is: 3126



**PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP**



**TABLE 7. PACKAGE DIMENSIONS**

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |            |         |         |
|--|------------|---------|---------|
| SYMBOL   | BBA        |         |         |
|  | MINIMUM    | NOMINAL | MAXIMUM |
| N  | 32         |         |         |
| A  | --         | --      | 1.60    |
| A1   | 0.05       | --      | 0.15    |
| A2   | 1.35       | 1.40    | 1.45    |
| b  | 0.30       | 0.37    | 0.45    |
| c  | 0.09       | --      | 0.20    |
| D  | 9.00 BASIC |         |         |
| D1   | 7.00 BASIC |         |         |
| D2   | 5.60 Ref.  |         |         |
| E  | 9.00 BASIC |         |         |
| E1   | 7.00 BASIC |         |         |
| E2   | 5.60 Ref.  |         |         |
| e  | 0.80 BASIC |         |         |
| L  | 0.45       | 0.60    | 0.75    |
| θ  | 0°         | --      | 7°      |
| ccc  | --         | --      | 0.10    |

Reference Document: JEDEC Publication 95, MS-026



Integrated  
Circuit  
Systems, Inc.

# ICS8705

## ZERO DELAY, DIFFERENTIAL-TO-LVCMOS/LVTTL

### CLOCK GENERATOR

**TABLE 8. ORDERING INFORMATION**

| Part/Order Number | Marking     | Package                                   | Count        | Temperature |
|-------------------|-------------|---|--------------|-------------|
| ICS8705BY         | ICS8705BY   | 32 Lead LQFP                              | 250 per tray | 0°C to 70°C |
| ICS8705BYT        | ICS8705BY   | 32 Lead LQFP on Tape and Reel             | 1000         | 0°C to 70°C |
| ICS8705BYLF       | ICS8705BYLF | 32 Lead "Lead Free" LQFP                  | 250 per tray | 0°C to 70°C |
| ICS8705BYLFT      | ICS8705BYLF | 32 Lead "Lead Free" LQFP on Tape and Reel | 1000         | 0°C to 70°C |

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| REVISION HISTORY SHEET |                          |         |  |          |
|------------------------|--------------------------|---------|--|----------|
| Rev                    | Table                    | Page    | Description of Change  | Date     |
| A                      |                          | 1       | Updated Block Diagram  | 1/25/02  |
| B                      | T3A                      | 3       | PLL Enable Function Table - revised the Reference Frequency Range column   | 3/14/02  |
|                        | T5A                      | 5       | 3.3V AC Characteristics Table - updated the Output Frequency row from 350MHz Max. to 275MHz Max.   |          |
|                        | T4D:T4F; T5B             | 6, 7    | Added 2.5V tables.   |          |
| C                      | T3A                      | 3       | PLL Enable Function Table - revised the Reference Frequency Range column   | 4/4/02   |
|                        | T5A                      | 5       | 3.3V AC Characteristics Table - updated the Output Frequency row from 275MHz Max. to 250MHz Max.   |          |
|                        | T5B                      | 7       | 2.5V AC Characteristics Table - updated the Output Frequency row from 275MHz Max. to 250MHz Max.   |          |
| C                      | T1                       | 2       | Pin Description Table - revised power pin descriptions.  | 4/10/02  |
| C                      | T2                       | 2       | Pin Characteristics Table - add 23pF (typical) in C <sub>PD</sub> row.   | 7/15/02  |
| C                      | T1                       | 2       | Pin Description Table - Pin# 10 from description, replaced "Connect to pin 10." with "Connect to one of the outputs."  | 8/1/02   |
| C                      | T1                       | 2       | Revised CLK0 description and MR description.   | 8/21/02  |
|                        |                          | 8       | Revised Output Rise/Fall Time Diagram.   |          |
| D                      | T1, T4A, T4D<br>T5A, T5B | 2, 4, 6 | Revised description for V <sub>DD</sub> to read Core supply from Positive supply.  | 11/22/02 |
|                        |                          | 5, 7    | AC Characteristics, added another row to "odc" with different test conditions and values.<br>Updated format.   |          |
| E                      | 1                        | 2       | Pin Description table - revised MR description.  | 1/22/03  |
|                        | T5A & T5B                | 5 & 7   | AC tables - Changed the Static Phase Offset limits for CLK1, nCLK1.  |          |
| F                      | T5A & T5B                | 5 & 7   | AC tables - added Static Phase Offset with "fREF = 66MHz, Qx * 2".   | 2/13/03  |
|                        |                          |         | 3.3V AC table - corrected typo in SPO parameter to read NOTE 4 from NOTE 7.<br>Throughout datasheet revised title to read "...Differential-to-LVCMOS/LVTTL..." |          |
| G                      | T5B                      | 7       | 2.5V AC Characteristics Table - added Phase Jitter spec, and Note 5.   | 3/14/03  |
|                        |                          | 9       | Replaced Static Phase Offset Diagram with Phase Jitter & SPO Diagram.  |          |
| G                      | T2                       | 2       | Pin Characteristics Table - changed C <sub>IN</sub> from 4pF max. to 4pF typical.  | 5/15/03  |
|                        |                          | 11      | Added Differential Clock Input Interface section.  |          |
| G                      |                          | 12 & 13 | Added Layout Guideline   | 6/6/03   |
| G                      | T6                       | 14      | Ordering Information Table - added "Lead-Free" part number   | 6/16/04  |