Low Skew, 1-to-6, Dual Crystal/LVCMOS-to-3.3V, 2.5V LVPECL Fanout Buffer

ICS8536-02

DATA SHEET

General Description

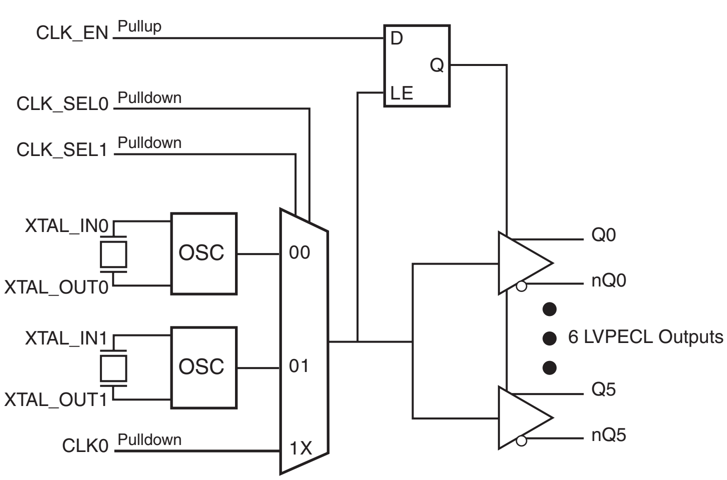
The ICS8536-02 is a low skew, high performance 1-to-6, Dual Crystal or LVCMOS Input-to-3.3V, 2.5V LVPECL Fanout Buffer. The ICS8536-02 has selectable crystal or single ended clock input. The single ended clock input accepts LVCMOS or LVTTL input levels and translates them to LVPECL levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8536-02 ideal for those applications demanding well defined performance and repeatability.

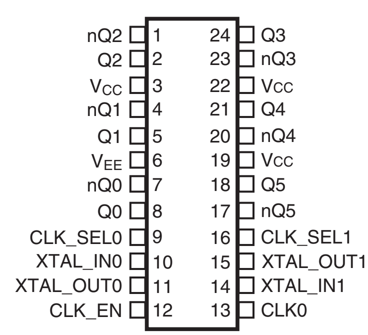
Features

- Six 3.3V, 2.5V differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Maximum output frequency: 266MHz
- Crystal frequency range: 14MHz – 40MHz
- Output skew: 55ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 1.85ns (maximum), 3.3V
- Additive phase jitter, RMS: 0.149ps (typical)
- Full 3.3V or 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8536-02

24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
3, 19, 22	V_{CC}	Power		Power supply pins.
4, 5	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
6	V_{EE}	Power		Negative supply pin.
7, 8	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.
9, 16	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select pins. LVCMOS/LVTTL interface levels. See Table 3B.
10, 11	XTAL_IN0, XTAL_OUT0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
12	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, the outputs are disabled. LVCMOS / LVTTL interface levels. See Table 3A.
13	CLK0	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
14, 15	XTAL_IN1, XTAL_OUT1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
17, 18	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
20, 21	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

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Function Tables

Table 3. Control Input Function Table

Inputs				Outputs	
CLK_EN	**CLK_SEL1**	**CLK_SEL0**	**Selected Source**	**Q[0:5]**	**nQ[0:5]**
0	0	0	XTAL0	Disabled	Disabled
0	0	1	XTAL1	Disabled	Disabled
0	1	X	CLK0	Disabled	Disabled
1	0	0	XTAL0	Enabled	Enabled
1	0	1	XTAL1	Enabled	Enabled
1	1	X	CLK0	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show in Figure 1. In the active mode, the state of the outputs are a function of the selected clock input.

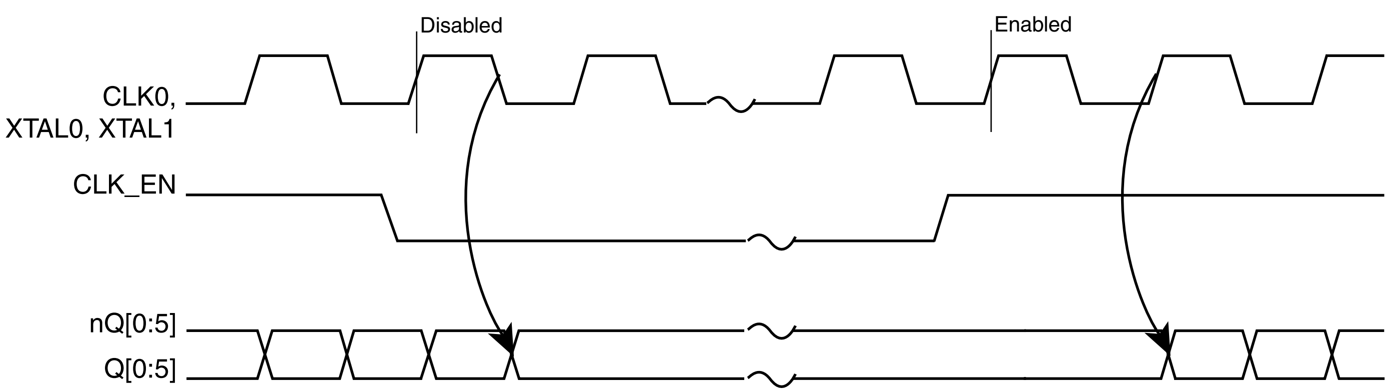

Figure 1. CLK_EN Timing Diagram

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I XTAL_IN Other Input	 0V to V_{CC} -0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	87.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				89	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				84	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK_SEL[0:1]	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
		CLK_EN	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK0, CLK_SEL[0:1]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		CLK_EN	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

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Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4E. LVPECL DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		14		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

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AC Electrical Characteristics

Table 6A. AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1		1.35		1.85	ns
*t*jit	Buffer Additive Phase Jitter, RMS; NOTE 2	155.52MHz, Integration Range: 12kHz – 20MHz		0.149		ps
*t*sk(o)	Output skew; NOTE 3, 4				55	ps
*t*sk(pp)	Part-to-Part skew; NOTE 4, 5				500	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		47		53	%
$MUX_{\_ISOLATION}$	MUX Isolation; NOTE 6	*f* = 150MHz		48		dB
		f = 250MHz		45		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at f_{OUT} unless noted otherwise.
NOTE 1: Measured from $V_{CC}/2$ of the input crossing point to the differential output crossing point.
NOTE 2: Driving CLK0 input.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 6: Measured on either XTAL0 or XTAL1 when single-ended CLK0 switching at 150MHz or 250MHz.

Table 6B. AC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1		1.4		1.9	ns
*t*jit	Buffer Additive Phase Jitter, RMS; NOTE 2	155.52MHz, Integration Range: 12kHz – 20MHz		0.149		ps
*t*sk(o)	Output skew; NOTE 3, 4				55	ps
*t*sk(pp)	Part-to-Part skew; NOTE 4, 5				500	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		47		53	%
$MUX_{\_ISOLATION}$	MUX Isolation; NOTE 6	*f* = 150MHz		40		dB
		f = 250MHz		40		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at f_{OUT} unless noted otherwise.
NOTE 1: Measured from $V_{CC}/2$ of the input crossing point to the differential output crossing point.
NOTE 2: Driving CLK0 input.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 6: Measured on either XTAL0 or XTAL1 when single-ended CLK0 switching at 150MHz or 250MHz.

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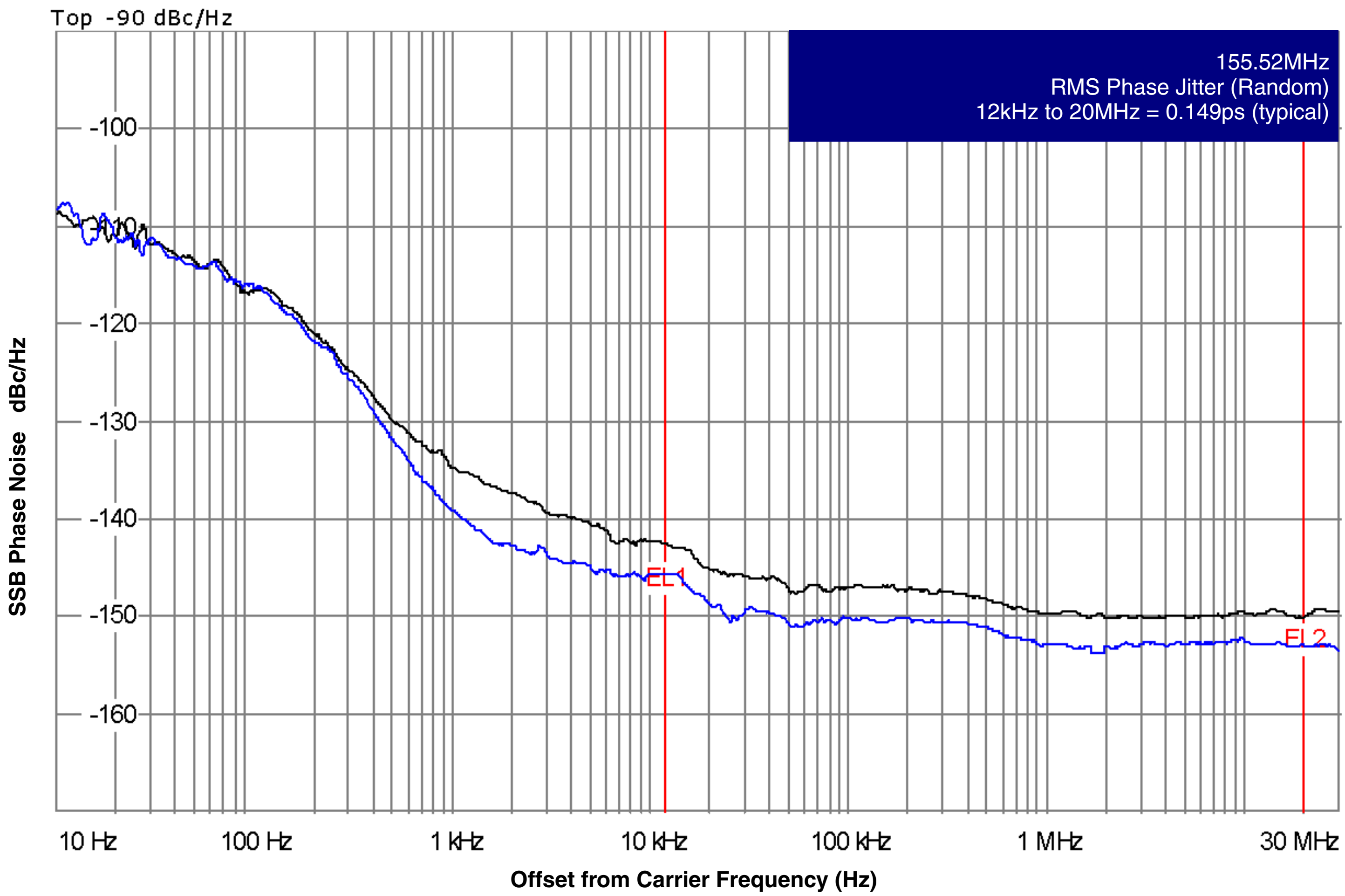
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "SMA 100 Generator 9kHz – 6GHz as external input to an Agilent 8133A 3HGz Pulse Generator".

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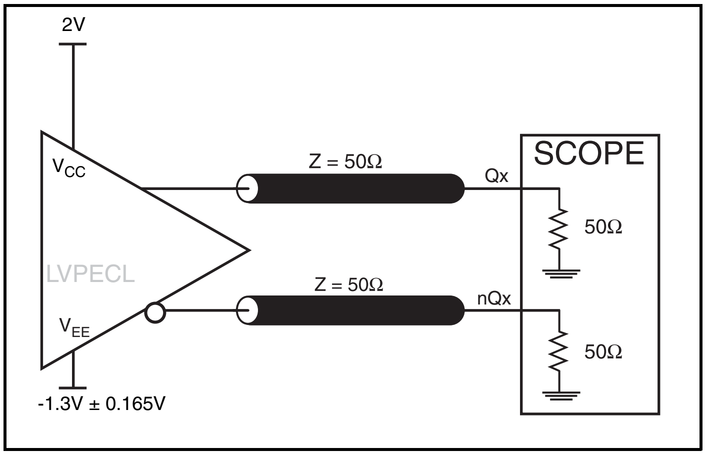
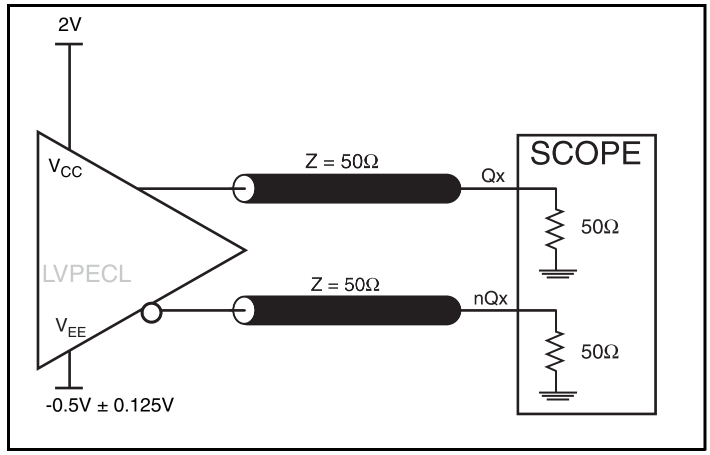
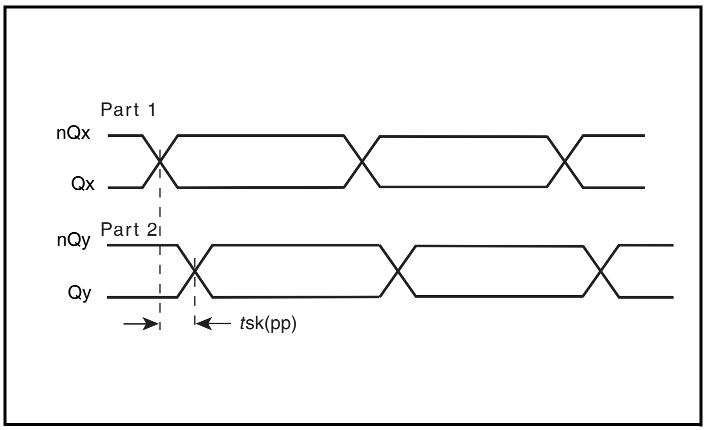
Parameter Measurement Information



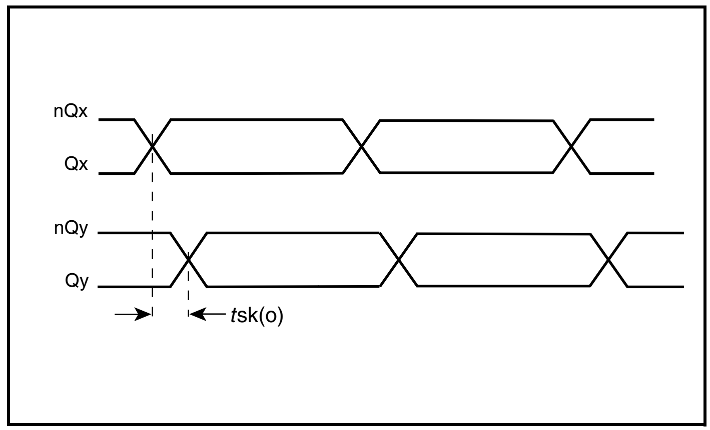
3.3V LVPECL Output Load AC Test Circuit



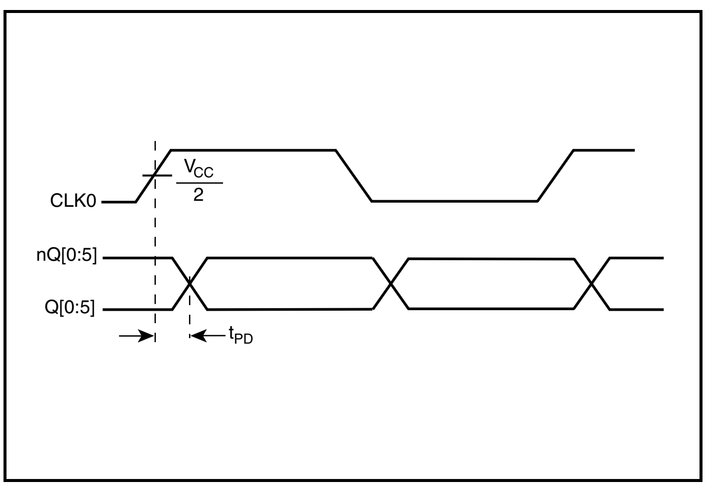
2.5V LVPECL Output Load AC Test Circuit



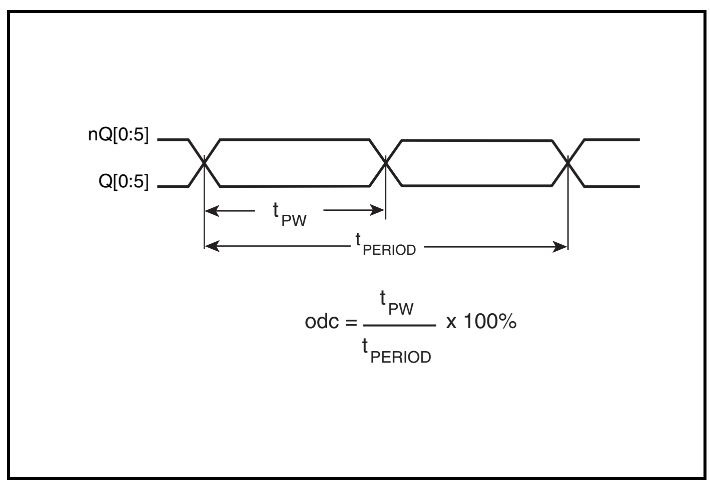
Part-to-Part Skew



Output Skew



Propagation Delay



Output Duty Cycle/Pulse Width/Period

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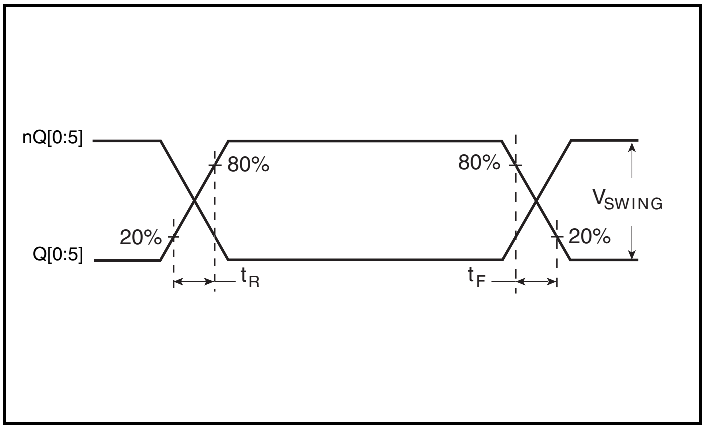
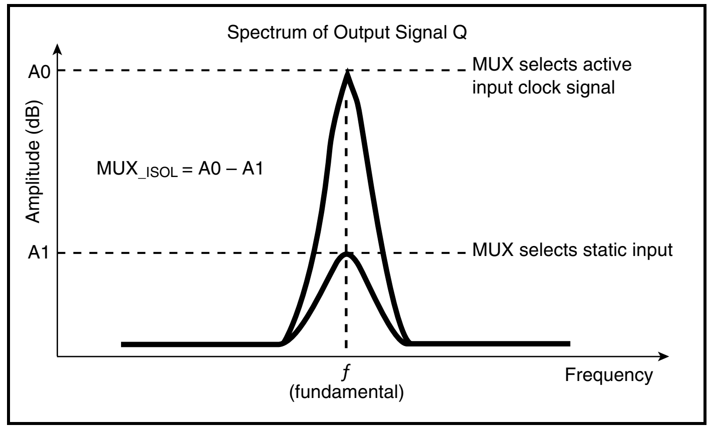
Parameter Measurement Information, continued



Output Rise/Fall Time



MUX_ISOLATION

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK0 Input

For applications not requiring the use of the clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK0 input to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

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Crystal Input Interface

The ICS8536-02 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

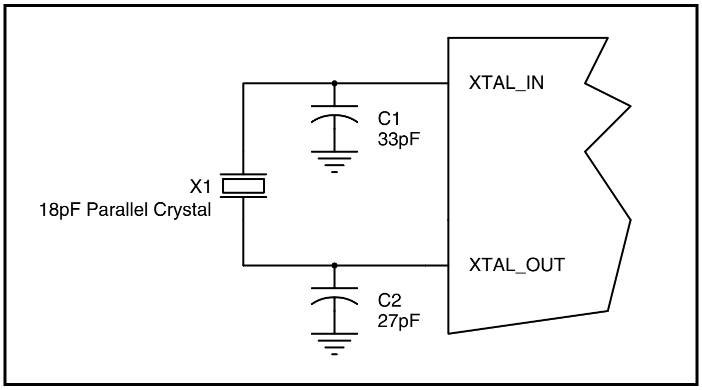

Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

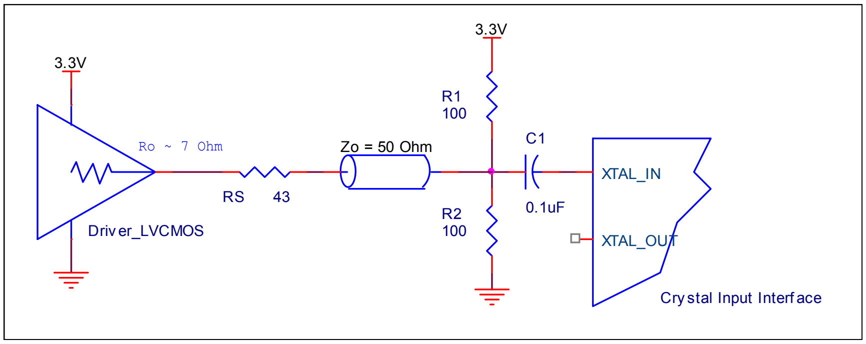

Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

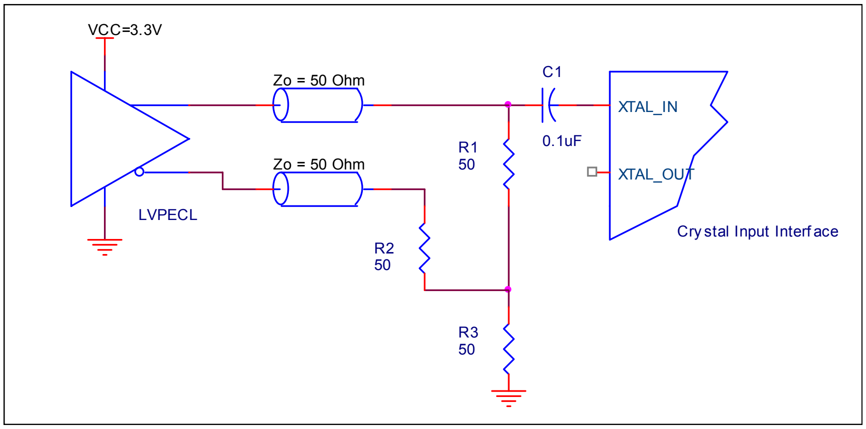

Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

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Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

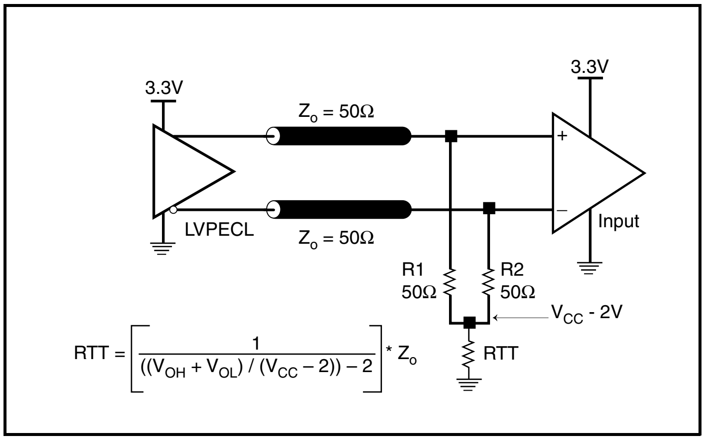

Figure 4A. 3.3V LVPECL Output Termination

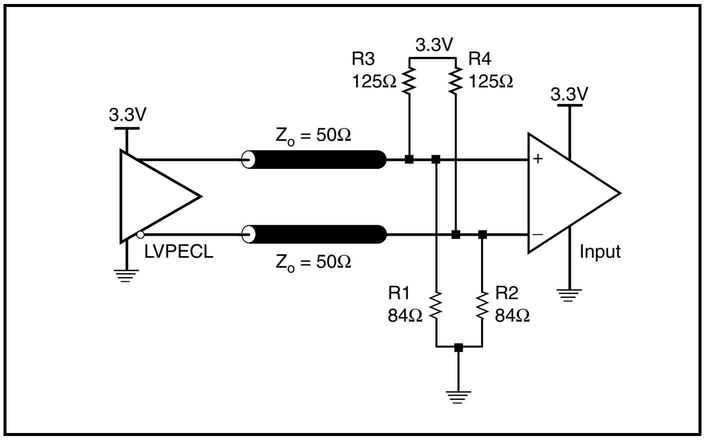

Figure 4B. 3.3V LVPECL Output Termination

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Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

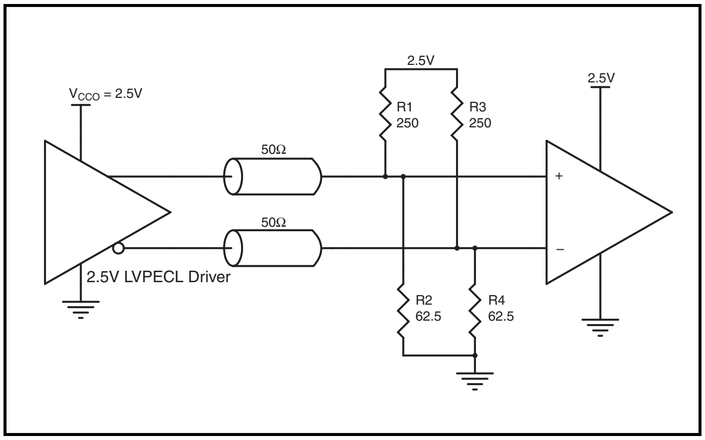

Figure 5A. 2.5V LVPECL Driver Termination Example

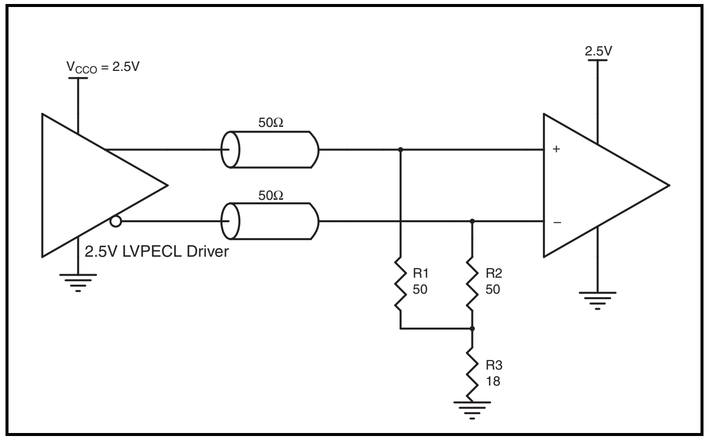

Figure 5B. 2.5V LVPECL Driver Termination Example

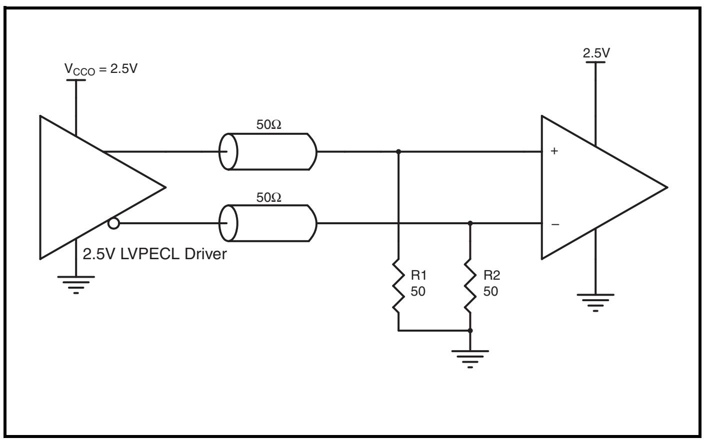

Figure 5C. 2.5V LVPECL Driver Termination Example

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8536-02.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8536-02 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 89mA = **308.385mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 30mW = **180mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 308.385mW + 180mW = **488.385mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 87.8°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.488W * 87.8°C/W = 112.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resitance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.8°C/W	83.5°C/W	81.3°C/W

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3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6.*

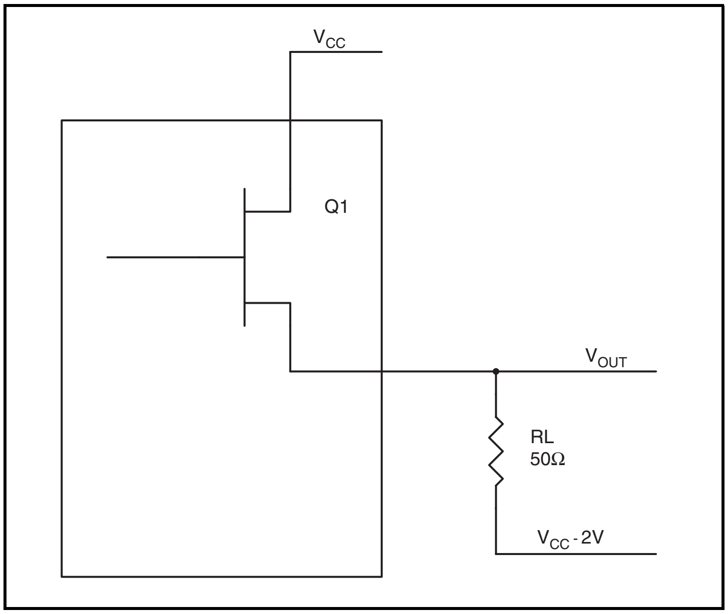

Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V = $ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V = $ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

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Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.8°C/W	83.5°C/W	81.3°C/W

Transistor Count

The transistor count for ICS8536-02 is: 467

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

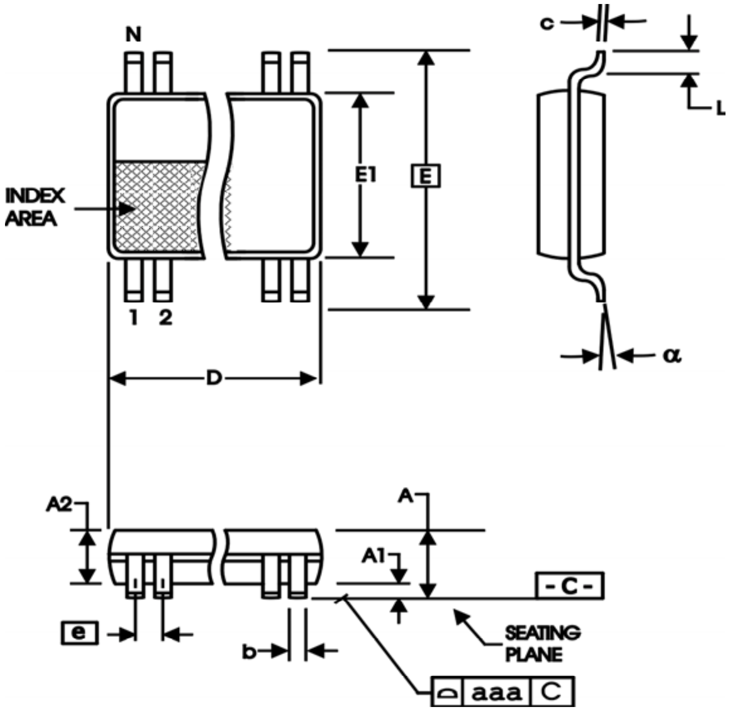

Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

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Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8536AG-02	ICS8536AG-02	24 Lead TSSOP	Tube	0°C to 70°C
8536AG-02T	ICS8536AG-02	24 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
8536AG-02LF	ICS8536AG-02L	“Lead-Free” 24 Lead TSSOP	Tube	0°C to 70°C
8536AG-02LFT	ICS8536AG-02L	“Lead-Free” 24 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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