/V//XI/V/

Four Digit Display Decoder/Drivers

ICM7211/7212

General Description

The Maxim ICM7211 (LCD) and ICM7212 (LED) four digit, seven segment display drivers include input data latches, BCD to segment decoders, and all level translation and timing circuits needed to drive non-multiplexed displays.

Both the ICM7211 and ICM7212 are available in two data input configurations: a multiplexed BCD interface version and a microprocessor interface version. The multiplexed BCD interface version has four BCD data inputs and four separate digit strobes. The micro-processor interface versions, designated by an "M" suffix, have four BCD data inputs, two digit address lines, and two chip selects or WRITE inputs.
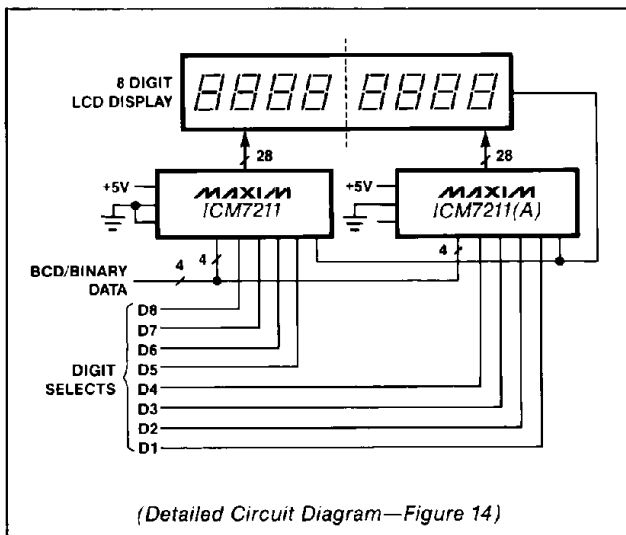
The ICM7211 and ICM7212 decode the BCD data via an onboard character font ROM. There are two different character fonts available, hexadecimal and Code B.

Applications

The low power consumption of the ICM7211 LCD driver makes it ideal for battery powered and portable applications. The ICM7212 LED display driver reduces system cost by eliminating external level translators, external segment drivers, and segment current limiting resistors.

Digital Panel Displays
Intelligent Instruments
Remote Display Units
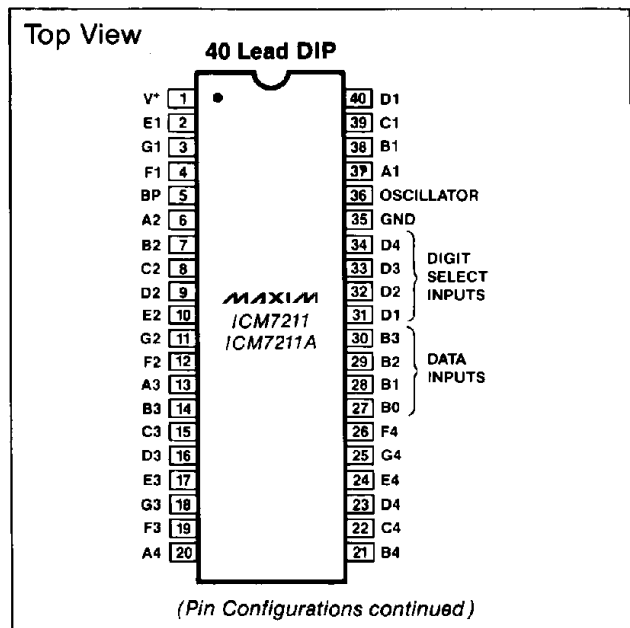Microprocessor-to-Visual Communication

Features

Improved 2nd Source! (See 3rd page for "Maxim Advantage™").

♦ Directly drives Four Digit, 7 Segment Displays
ICM7211 - Non-multiplexed Liquid Crystal Display (LCD)
ICM7212 - Non-multiplexed Common Anode LED

Multiplexed BCD Interface and µP Interface Versions

♦ No external components needed

♦ Low Power CMOS - 25µW typ. (display blanked)

Ordering Information

DEVICE TYPE	OUTPUT CODE	INPUT CONFIGURATION
ICM7211 (LCD)	Hexadecimal	Multiplexed 4-Bit
ICM7211A (LCD)	Code B	
ICM7211M (LCD)	Hexadecimal	µP Interface
ICM7211AM (LCD)	Code B	
ICM7212 (LED)	Hexadecimal	Multiplexed 4-Bit
ICM 7212A (LED)	Code B	
ICM7212M (LED)	Hexadecimal	µP Interface
ICM7212AM (LED)	Code B	

Pin Configurations

Top View   40 Lead DIP

V⁺ 1	40 D1
E1 2	39 C1
G1 3	38 B1
F1 4	37 A1
BP 5	36 OSCILLATOR
A2 6	35 GND
B2 7	34 D4 ⎫
C2 8	33 D3 ⎬ DIGIT SELECT INPUTS
D2 9	32 D2
E2 10	31 D1 ⎭
G2 11	30 B3 ⎫
F2 12	29 B2 ⎬ DATA INPUTS
A3 13	28 B1
B3 14	27 B0 ⎭
C3 15	26 F4
D3 16	25 G4
E3 17	24 E4
G3 18	23 D4
F3 19	22 C4
A4 20	21 B4

/V//XI/V/ ICM7211 ICM7211A

(Pin Configurations continued)

Typical Operating Circuit

(Detailed Circuit Diagram—Figure 14)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Four Digit Display Decoder/Drivers

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ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) .... 0.5 W@ 70°C
Supply Voltage 6.5V
Input Voltage (Any
Terminal) (Note 2) .... V$^+$ +0.3V, GROUND -0.3V
Operating Temperature Range .... -20°C to +85°C
Storage Temperature Range .... -55°C to +125°C
(Lead Temperature (Soldering 10 sec.) .... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V$^+$ = 5V; T$_A$ = 25°C, Test circuit unless noted)

ICM7211 CHARACTERISTICS (LCD)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V$_{SUPP}$		3	5	6	V
Operating Current	I$_{OP}$	Test circuit, Display blank		10	50	μA
Oscillator Input Current	I$_{OSCI}$	Pin 36		±2	±10	
Segment Rise/Fall Time	t$_{RFS}$	C$_L$ = 200pF		0.5		
Backplane Rise/Fall Time	t$_{RFB}$	C$_L$ = 5000pF		1.5		μs
Oscillator Frequency	f$_{OSC}$	Pin 36 Floating		16		kHz
Backplane Frequency	f$_{BP}$	Pin 36 Floating		125		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V$_{SUPP}$		4	5	6	V
Operating Current Display Off	I$_{OP}$	Pin 5 (Brightness), Pin 27-34 - GROUND		10	50	μA
Operating Current	I$_{OP}$	Pin 5 at V$^+$, Display all 8's		200		mA
Segment Leakage Current	I$_{SLK}$	Segment Off		±0.01	±1	μA
Segment On Current	I$_{SEG}$	Segment On, V$_O$ = +3V	5	8		mA

INPUT CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" input voltage	V$_{IH}$		3			V
Logical "0" input voltage	V$_{IL}$				1	
Input leakage current	I$_{ILK}$	Pins 27-34		±.01	±1	μA
Input capacitance	C$_{IN}$	Pins 27-34		5		pF
BP/Brightness input leakage	I$_{BPLK}$	Measured at Pin 5 with Pin 36 at GND		±.01	±1	μA
BP/Brightness input capacitance	C$_{BPI}$	All Devices		200		pF

AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Digit Select Active Pulse Width	t$_{SA}$	Refer to Timing Diagrams	•1			μs
Data Setup Time	t$_{DS}$		500			ns
Data Hold Time	t$_{DH}$		200			
Inter-Digit Select Time	t$_{IDS}$		2			μs

AC CHARACTERISTICS - MICROPROCESSOR INTERFACE

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Chip Select Active Pulse Width	t$_{CSA}$	other chip select either held active, or both driven together	200			ns
Data Setup Time	t$_{DS}$		100			
Data Hold Time	t$_{DH}$		10	0		
Inter-Chip Select Time	t$_{ICS}$		2			μs

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V$^+$ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

MAXIM

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Four Digit Display Decoder/Drivers

♦ **Key Parameters Guaranteed Over Temperature**

♦ **Increased Segment-On Current**

♦ **Low Power (Typically 25µW)**

♦ **Maxim Quality and Reliability**

♦ **Improved ESD Protection (Note 3)**

ABSOLUTE MAXIMUM RATINGS This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V; T_A = 25°C, Test circuit unless noted.)

ICM7211 CHARACTERISTICS (LCD)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{OP}	**Test circuit, Display blank**		**5**	**25**	µA
Oscillator Input Current	I_{OSCI}	Pin 36, V_{OSC} = 2.5V		±2	±10	µA
Segment Rise/Fall Time	t_{RFS}	C_L = 200pF		0.5		µs
Backplane Rise/Fall Time	t_{RFB}	C_L = 5000pF		1.5		
Oscillator Frequency	f_{OSC}	Pin 36 Floating		19		kHz
Backplane Frequency	f_{BP}	Pin 36 Floating		150		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pin 27-34 - GROUND		5	50	µA
Operating Current	I_{OP}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SLK}	Segment Off		±0.01	±1	µA
Segment On Current	I_{SEG}	**Segment On, V_O = +3V; T_A = 25°C** **0°C ≤ T_A ≤ +70°C**	6 5	9		mA

INPUT CHARACTERISTICS (ICM7211 AND ICM7212)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" input voltage	V_{IH}	**Pins 27-34, -20°C to +85°C**	3			**V**
Logical "0" input voltage	V_{IL}	**Pins 27-34, -20°C to +85°C**			1	
Input leakage current	I_{ILK}	Pins 27-34		±.01	±1	µA
Input capacitance	C_{IN}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		±.01	±1	µA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{SA}	Refer to Timing Diagrams	1			µs
Data Setup Time	t_{DS}		-100			ns
Data Hold Time	t_{DH}		200			
Inter-Digit Select Time	t_{IDS}		2			µs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{CSA}	Other chip select either held active, or both driven together		200		ns
Data Setup Time	t_{DS}		100			
Data Hold Time	t_{DH}		10	0		
Inter-Chip Select Time	t_{ICS}		2			µs

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

Note 3: All pins except pin 29 are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil STD 883B Method 3015.1 Test Circuit). Due to the special test functions associated with pin 29, this pin is designed to withstand up to 1500V (same test circuit).
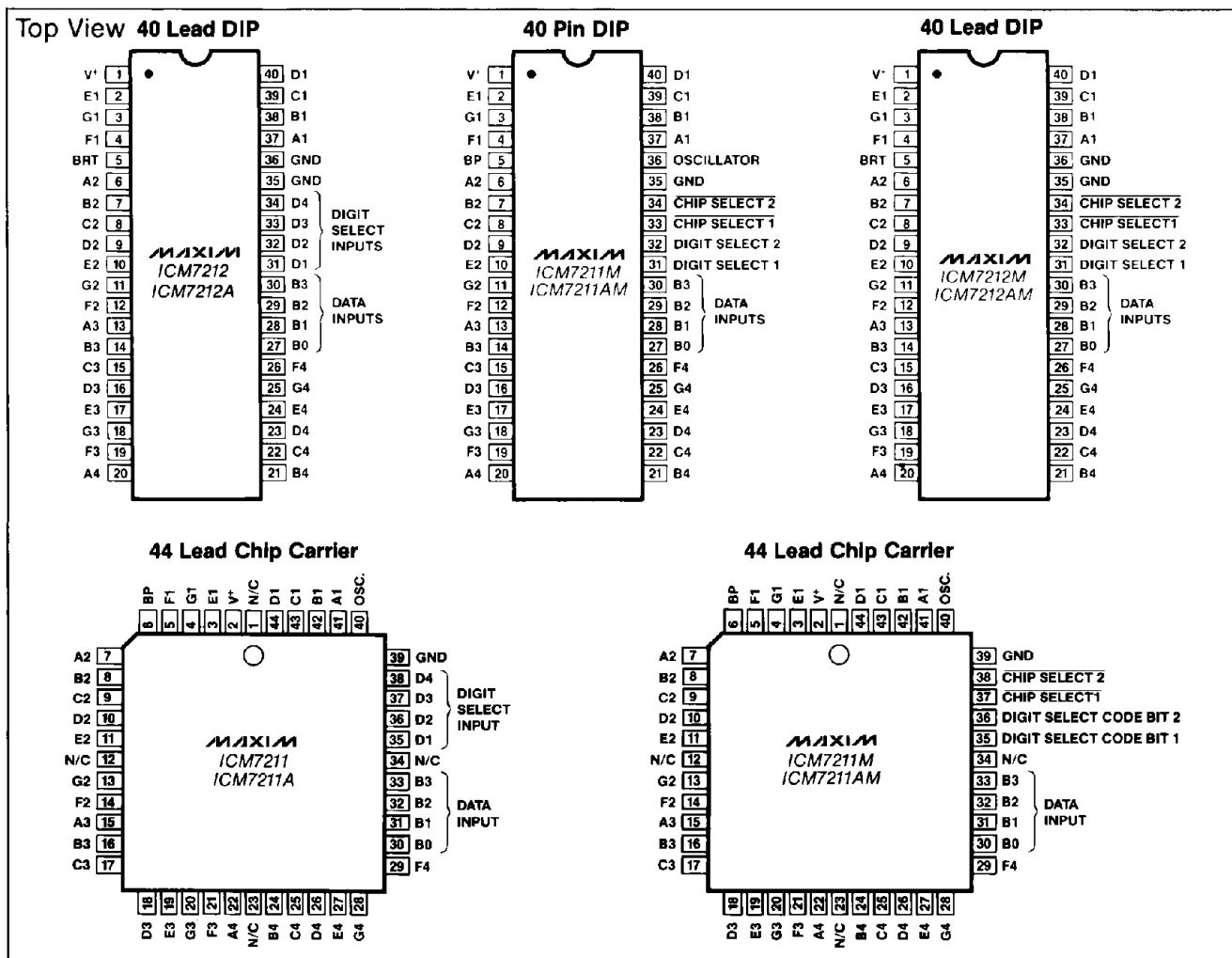
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Four Digit Display Decoder/Drivers

ICM7211/7212

PART	TEMP. RANGE	PACKAGE
ICM7211IQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7211AIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7211MIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7211AMIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212IQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212AIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212MIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212AMIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier

PART	TEMP. RANGE	PACKAGE
ICM7211IPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7211AIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7211MIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7211AMIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212IPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212AIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212MIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212AMIPL	-20°C to +85°C	40 Lead Plastic DIP

Each device type listed is available in dice form;
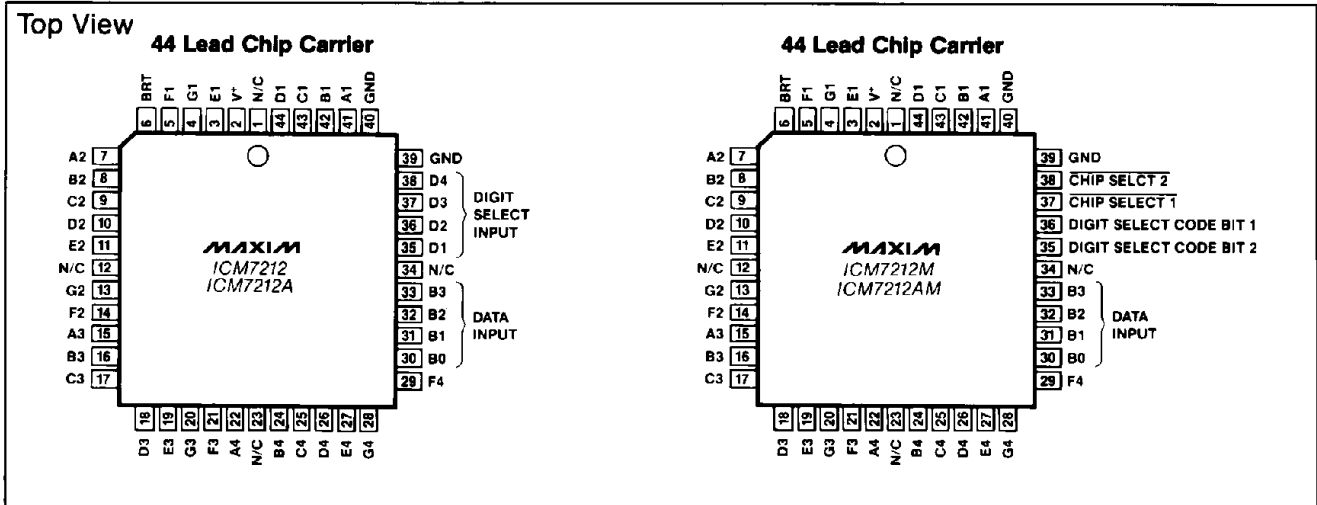Order basic part number followed by C/D;
(i.e. ICM7211C/D).

Top View 40 Lead DIP — MAXIM ICM7212 / ICM7212A

Left		Right	
V+	1	40	D1
E1	2	39	C1
G1	3	38	B1
F1	4	37	A1
BRT	5	36	GND
A2	6	35	GND
B2	7	34	D4
C2	8	33	D3
D2	9	32	D2
E2	10	31	D1
G2	11	30	B3
F2	12	29	B2
A3	13	28	B1
B3	14	27	B0
C3	15	26	F4
D3	16	25	G4
E3	17	24	E4
G3	18	23	D4
F3	19	22	C4
A4	20	21	B4

Pins 34–31: DIGIT SELECT INPUTS; Pins 30–27: DATA INPUTS

40 Pin DIP — MAXIM ICM7211M / ICM7211AM

Left		Right	
V+	1	40	D1
E1	2	39	C1
G1	3	38	B1
F1	4	37	A1
BP	5	36	OSCILLATOR
A2	6	35	GND
B2	7	34	CHIP SELECT 2
C2	8	33	CHIP SELECT 1
D2	9	32	DIGIT SELECT 2
E2	10	31	DIGIT SELECT 1
G2	11	30	B3
F2	12	29	B2
A3	13	28	B1
B3	14	27	B0
C3	15	26	F4
D3	16	25	G4
E3	17	24	E4
G3	18	23	D4
F3	19	22	C4
A4	20	21	B4

Pins 30–27: DATA INPUTS

40 Lead DIP — MAXIM ICM7212M / ICM7212AM

Left		Right	
V+	1	40	D1
E1	2	39	C1
G1	3	38	B1
F1	4	37	A1
BRT	5	36	GND
A2	6	35	GND
B2	7	34	CHIP SELECT 2
C2	8	33	CHIP SELECT 1
D2	9	32	DIGIT SELECT 2
E2	10	31	DIGIT SELECT 1
G2	11	30	B3
F2	12	29	B2
A3	13	28	B1
B3	14	27	B0
C3	15	26	F4
D3	16	25	G4
E3	17	24	E4
G3	18	23	D4
F3	19	22	C4
A4	20	21	B4

Pins 30–27: DATA INPUTS

44 Lead Chip Carrier — MAXIM ICM7211 / ICM7211A

Top pins (6,5,4,3,2,1,44,43,42,41,40): BP, F1, G1, E1, V+, N/C, D1, C1, B1, A1, OSC.

Left		Right	
A2	7	39	GND
B2	8	38	D4
C2	9	37	D3
D2	10	36	D2
E2	11	35	D1
N/C	12	34	N/C
G2	13	33	B3
F2	14	32	B2
A3	15	31	B1
B3	16	30	B0
C3	17	29	F4

Pins 38–35: DIGIT SELECT INPUT; Pins 33–30: DATA INPUT

Bottom pins (18,19,20,21,22,23,24,25,26,27,28): D3, E3, G3, F3, A4, N/C, B4, C4, D4, E4, G4

44 Lead Chip Carrier — MAXIM ICM7211M / ICM7211AM

Top pins (6,5,4,3,2,1,44,43,42,41,40): BP, F1, G1, E1, V+, N/C, D1, C1, B1, A1, OSC.

Left		Right	
A2	7	39	GND
B2	8	38	CHIP SELECT 2
C2	9	37	CHIP SELECT 1
D2	10	36	DIGIT SELECT CODE BIT 2
E2	11	35	DIGIT SELECT CODE BIT 1
N/C	12	34	N/C
G2	13	33	B3
F2	14	32	B2
A3	15	31	B1
B3	16	30	B0
C3	17	29	F4

Pins 33–30: DATA INPUT

Bottom pins (18,19,20,21,22,23,24,25,26,27,28): D3, E3, G3, F3, A4, N/C, B4, C4, D4, E4, G4

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Four Digit Display Decoder/Drivers

Pin Configurations (Cont.)

Top View

44 Lead Chip Carrier

44 Lead Chip Carrier

ICM7212
ICM7212A

Pin	Signal	
39	GND	
38	D4	
37	D3	DIGIT SELECT INPUT
36	D2	
35	D1	
34	N/C	
33	B3	
32	B2	DATA INPUT
31	B1	
30	B0	
29	F4	

Left pins: A2 [7], B2 [8], C2 [9], D2 [10], E2 [11], N/C [12], G2 [13], F2 [14], A3 [15], B3 [16], C3 [17]

Top pins: BRT [6], F1 [5], G1 [4], E1 [3], V+ [2], N/C [1], D1 [44], C1 [43], B1 [42], A1 [41], GND [40]

Bottom pins: D3 [18], E3 [19], G3 [20], F3 [21], A4 [22], N/C [23], B4 [24], C4 [25], D4 [26], E4 [27], G4 [28]

ICM7212M
ICM7212AM

Pin	Signal	
39	GND	
38	CHIP SELCT 2	
37	CHIP SELECT 1	
36	DIGIT SELECT CODE BIT 1	
35	DIGIT SELECT CODE BIT 2	
34	N/C	
33	B3	
32	B2	DATA INPUT
31	B1	
30	B0	
29	F4	

Typical Operating Characteristics

ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

DISPLAY BLANK
PIN 36 OPEN
$T_A = -20°C$
$T_A = 25°C$
$T_A = 70°C$

ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

$T_A = 25°C$
$C_{OSC} = 0$ (PIN 36 OPEN)
$C_{OSC} = 22pF$
$C_{OSC} = 220pF$
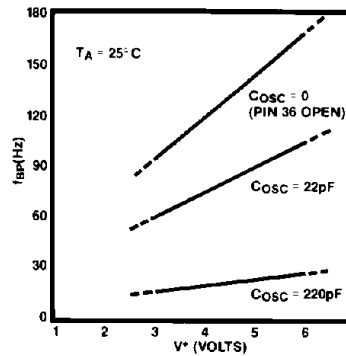
ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

PIN 5 AT V+
$T_A = 25°C$
$V^+ = 6V$
$V^+ = 5V$
$V^+ = 4V$
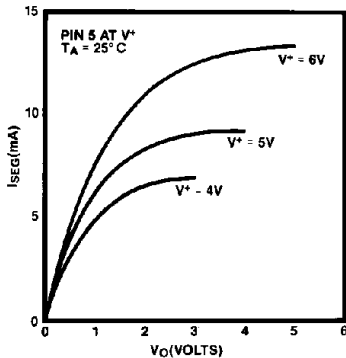
ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE

SEGMENT OUTPUT AT +3V
$T_A = 25°C$
$V^+ = 5V$
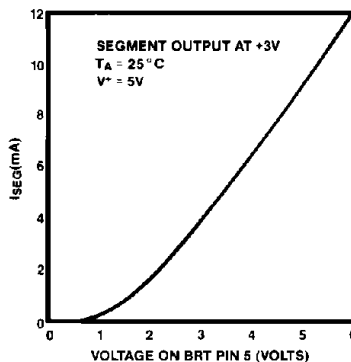
ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE

DISPLAY ALL EIGHTS
LED FORWARD VOLTAGE DROP
$V_{FLED} = 1.7V$
PIN 5 AT V+
$T_A = 25°C$
25°C LIMIT
70°C LIMIT

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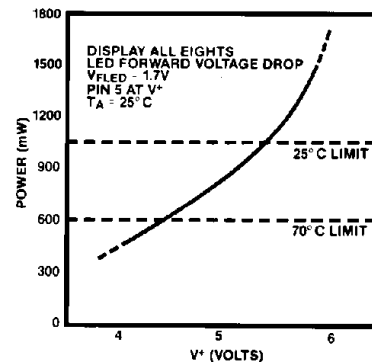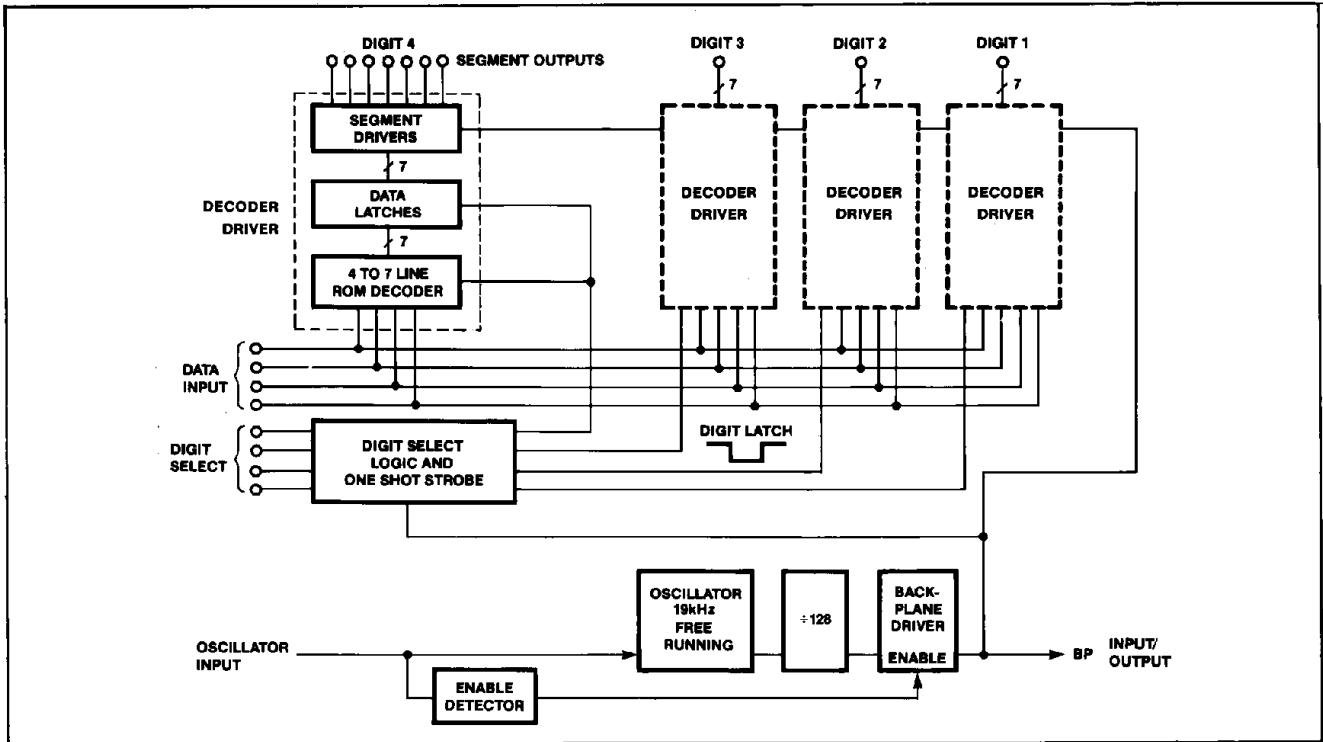
ICM7211/7212

Figure 1. Block diagram of ICM7211 and ICM7211A.
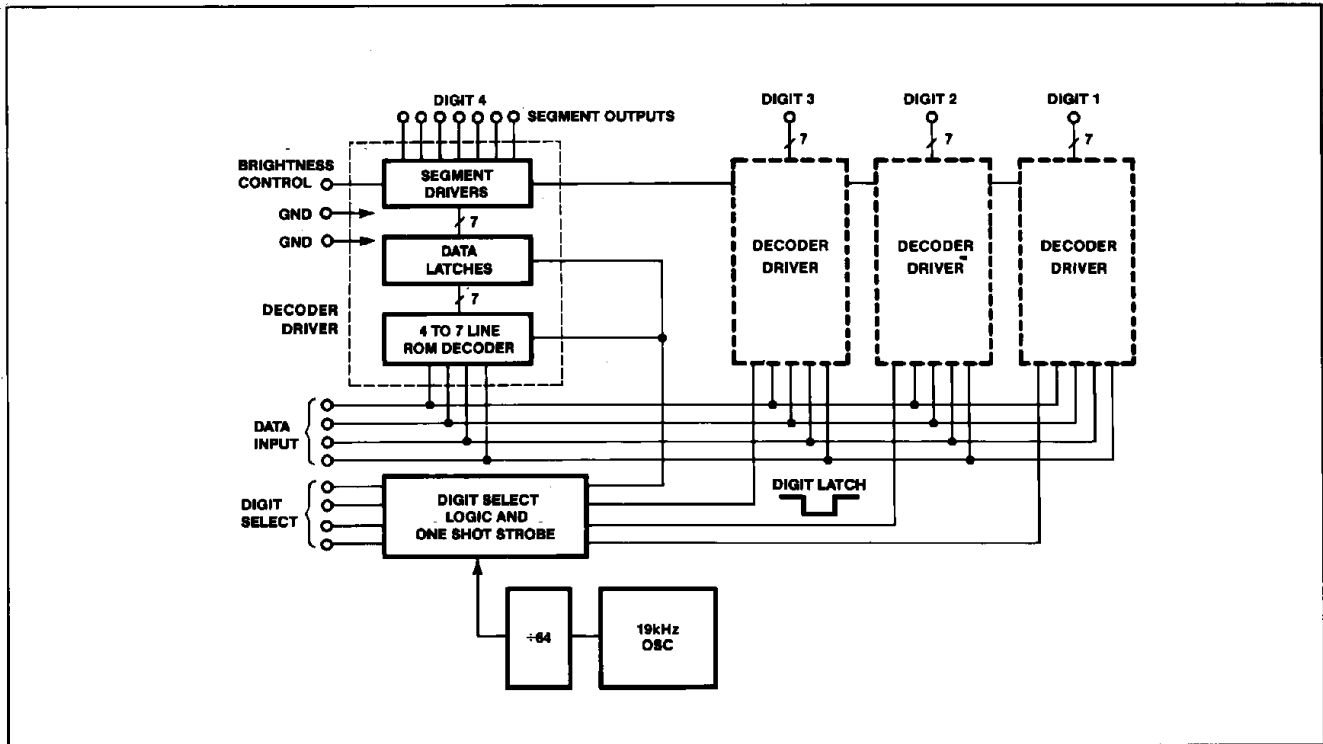
Figure 2. Block diagram of ICM7212 and ICM7212A.

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Figure 3. Block diagram of ICM7211M and ICM7211AM.

Figure 4. Block diagram of ICM7212M and ICM7212AM.

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Four Digit Display Decoder/Drivers

Detailed Description

Display Interface

The ICM7211 and ICM7212 differ only in the type of display interface. The ICM7211 is designed to drive non-multiplexed liquid crystal displays (LCDs), while the ICM7212 is designed to drive non-multiplexed, common anode LED displays.

ICM7211 LCD Display Driver

The display driver section of the ICM7211 includes an oscillator, a 7 stage binary divider, a backplane driver, backplane slaving detector and logic, and 28 segment drivers.

The RC oscillator has a nominal oscillation frequency of 19kHz with no external components. Ordinarily this frequency is suitable and no external oscillator components are needed, but if desired, the frequency may be lowered by connecting a capacitor between pin 36 (Oscillator) and either ground or V$^+$. A graph showing the relationship between capacitor value and oscillator frequency is shown in the Typical Character-istics section. The oscillator may also be overdriven by an external clock source with a frequency of 128 times the desired backplane frequency. The external clock source should swing from approximately 1.5V to 5V when V$^+$ is 5V. The external clock signal must not go below 1V for more than one microsecond, or the backplane disable circuitry may be activated (see below). Figure 7 shows an external clock drive circuit that meets the above requirements.

The 19kHz nominal output of the onboard oscillator is divided by a 7 stage binary divider (÷128) to generate the backplane frequency of 150Hz.

The backplane drive is simply an inverter whose input is the output of the last divider. The backplane output swings from ground to V$^+$ with a 50% duty cycle. The backplane has a low (200 ohm typical) output resistance so that it can drive the capacitance of large displays.

The backplane output driver can be disabled by tying pin 36 (Oscillator) to ground. The Backplane Input/Output (pin 5) then becomes an input which can be driven by the backplane output of another ICM7211 (see Figures 14, 16 and 17). Each backplane is a load of about 200 pF when driven, and no more than 4 ICM7211's (16 digits total) should be slaved together using one "master" ICM7211 as the backplane source, since power dissipation and the DC offset increase when the ICM7211 backplane output drives very large capacitive loads. For more than 16 digits on a common backplane, a separate, external driver with a low impedance should be used to drive all ICM7211s.

The segment drivers are CMOS inverters that swing between ground and V$^+$ with an output resistance of about 2 kΩ. The input to the inverter is switched between two signals, so that the segment driver output is the same as the backplane when LCD segment is to be turned OFF, and is BACKPLANE when the LCD segment is to be turned ON. The segment and

backplane drivers are designed to have equal rise and fall times, so that the average DC component across the LCD is less than 25 millivolts.
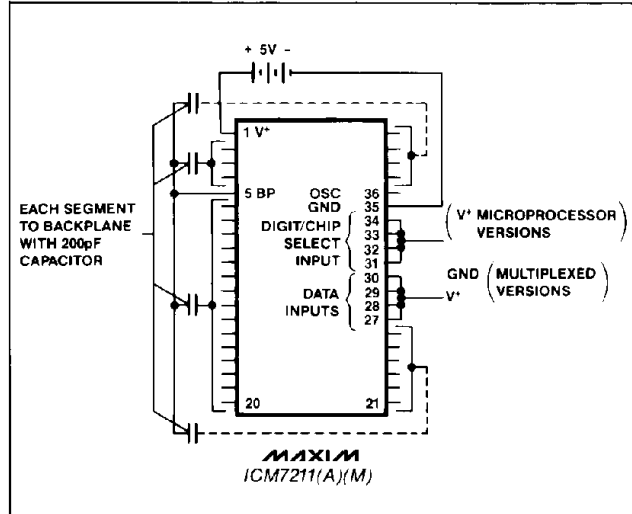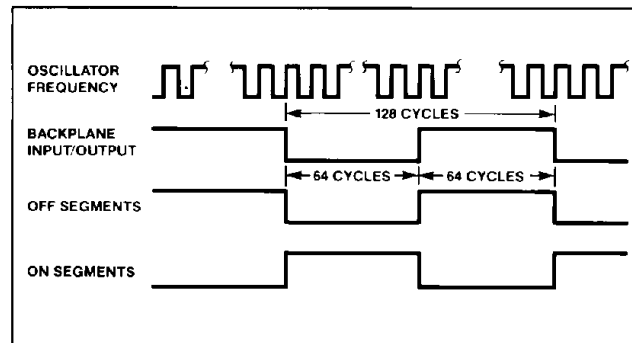

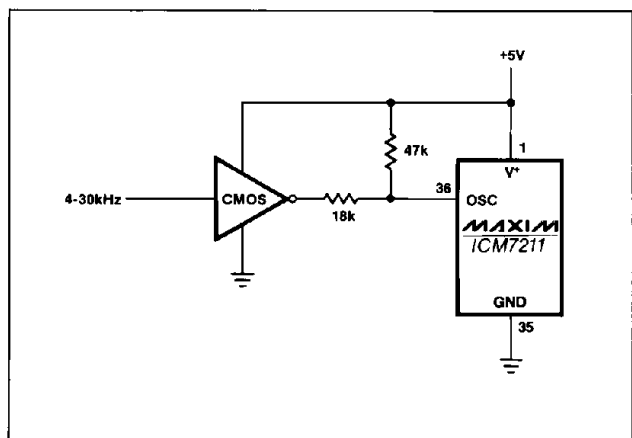Figure 5. ICM7211 Test Circuit (all versions).

Figure 6. Display Waveforms.

Figure 7. External Clock Drive.

MAXIM

ICM7212 LED Drivers

The ICM7212 has 28 open drain constant current n-channel outputs, which eliminate the need for external segment resistors. The LED current vs. output voltage of a typical segment driver is shown in the Typical Characteristics section. The Brightness input (pin 5) supplies the segment driver gate voltage, and it can be used to either control the brightness of the LED display or to completely blank the display. Two methods of controlling display brightness are shown in Figure 8. The first method simply controls the voltage on the brightness pin by means of a potentiometer. The Brightness input draws negligible current and the potentiometer is normally in the range of 100 kilohms to 1 megohm. By replacing the potentiometer with a resistor and a photoresistor, the display brightness can be automatically adjusted in response to changes in the ambient lighting. A second method of display brightness control is to duty-cycle modulate the Brightness input between "full on" and "blanked" states. As with the simple potentiometer method, the display brightness can be automatically adjusted for ambient lighting conditions by replacing one of the timing resistors with a photoresistor.

The ICM7212 has two ground pins to support the high total display current that flows into the segment outputs and then is returned to ground through the ICM7212 ground pins.

Since the ICM7212 will drive the LED display at high total display current, care must be taken not to exceed the absolute maximum power dissipation limit of the ICM7212 at high ambient temperatures. For example, at 70°C, the absolute maximum power dissipation specification is 500 mW. If all 28 segments are turned on (a display of 8888), and each segment is drawing 8 mA, the total power dissipation in the ICM7212 would be

$$Pd = 28 \text{ segments.}(8mA).(V_{seg})$$
$$\text{Where } V_{seg} = V^+ - V_{led} = 5V - 1.6V = 3.4V$$
$$\text{Therefore } Pd = 28.(8).(3.4) = 760 \text{ mW; greater}$$
than the absolute maximum limit.

There are two ways to keep the power dissipation below the ICM7212 power dissipation limits: reduce the LED current, or reduce the voltage across the ICM7212 segment drivers. The LED current can be reduced by the display brightness control circuits shown in figure 8. The other alternative, reducing the voltage across the segment drivers can be accomplished by either reducing the V^+ supply to the entire system, or by reducing the V^+ supply to just the LED display by placing diodes in series with the LED display (see Figure 9). Two silicon diodes in series with the anode of the LED display will reduce the voltage across the segment drivers from 3.4V to 2.2V, resulting in a power reduction of approximately 35%, while only slightly reducing the LED current and brightness. A third diode in series with the LED display would further reduce the power dissipation, but the segment current would also be reduced since there would be only about 1.6V across the n-channel segment driver.

Digital Interface

There are two different types of digital interfaces available for the ICM7211 and ICM7212, a multiplexed BCD interface and a microprocessor interface.

Multiplexed BCD Data Interface

On the multiplexed BCD data entry versions of ICM7211 and ICM7212 there are 8 lines used for entering data: 4 BCD data lines and 4 digit strobes. The multiplexed BCD input timing and truth table is shown in Figure 10. When one of the four digit strobes is taken high, a short internal pulse is generated which latches the decoded segment data in the 7 bit latch associated with that digit. If the digit strobe is continuously held high, each transition of the backplane will cause another internal latch pulse to be generated, latching new segment data if the BCD data has changed. When the digit strobe goes low the data in the latch is held constant with no further updates until the digit strobe is again taken high. As shown in the electrical specifications table, the data setup time is is a negative 100ns, which means that the digit strobe can be taken high as much as 100ns before the BCD data is valid.
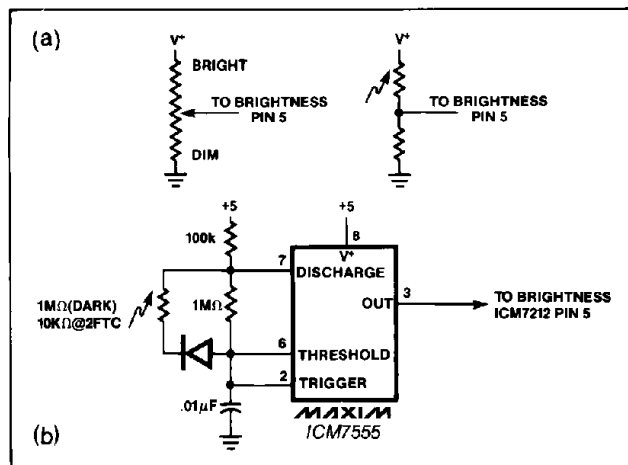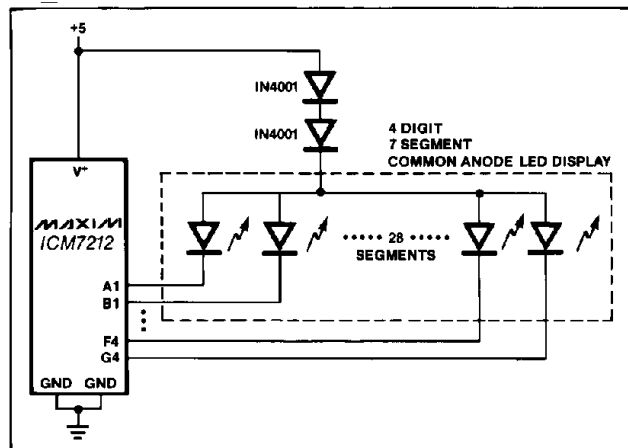

Figure 8A & 8B. Brightness Control

Figure 9. Reducing ICM7212 Power Dissipation.

Four Digit Display Decoder/Drivers

Character Fonts

Table 1 shows the two different output codes or fonts available. Both versions have the same display for 0-9 and differ only in the display of the last 6 input codes. The Code B versions have the suffix "A" in their part number.

Table 1: Output Codes

BINARY				HEXADECIMAL ICM7211(M) ICM7212(M)	CODE B ICM7211A(M) ICM7212A(M)
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	—
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(Blank)

Microprocessor or Data Interface

The microprocessor data interface versions of the ICM7211 and ICM7212 are denoted by an "M" suffix in their part number. The microprocessor data interface also uses 8 lines for the data interface: 4 BCD data lines, 2 digit address lines, and 2 active low chip select lines. A typical data write cycle and the truth table are shown in Figure 11. Data is entered into the input latches whenever both CS (chip select) lines are low. When either CS line goes high an internal one shot is activated, transferring the decoded 7-segment data to the appropriate digit latch. One CS line is ordinarily driven by an address decoder and the other CS line is driven by the microprocessor WR (write) line (see Figure 15). In this type of application, the ICM7211/12 is accessed as 4 "write only" memory locations.

Application Notes

Backplane Frequency

The ICM7211 onboard oscillator generates a backplane frequency of approximately 150Hz with no external components. This is suitable for most displays, but
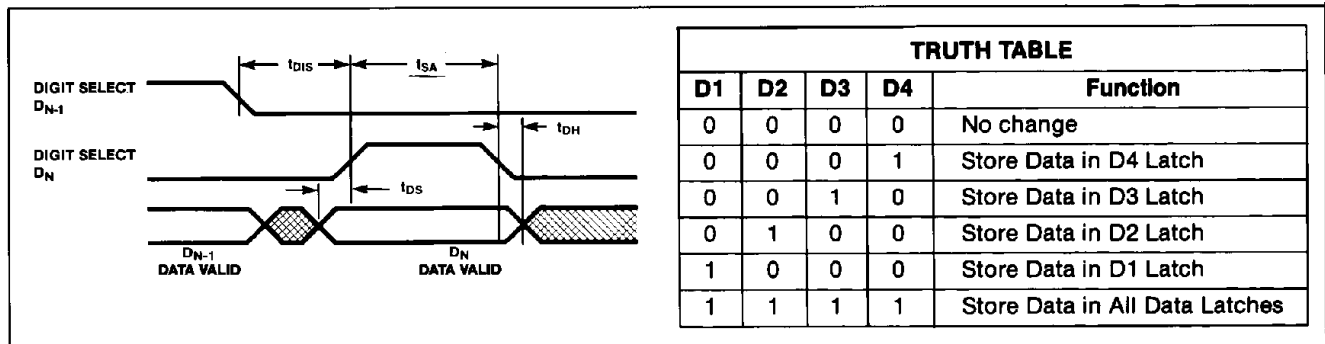

TRUTH TABLE				
D1	D2	D3	D4	Function
0	0	0	0	No change
0	0	0	1	Store Data in D4 Latch
0	0	1	0	Store Data in D3 Latch
0	1	0	0	Store Data in D2 Latch
1	0	0	0	Store Data in D1 Latch
1	1	1	1	Store Data in All Data Latches

Figure 10. Multiplexed input timing diagram and truth table.

TRUTH TABLE				
DS2	DS1	C̄S̄2	C̄S̄1	Function
X	X	X	1	No change
X	X	1	X	
0	0	0	↑	Store D4 Data
0	0	↑	0	
0	1	0	↑	Store D3 Data
0	0	↑	0	
1	0	0	↑	Store D2 Data
1	0	↑	0	
1	1	0	↑	Store D1 Data
1	1	↑	0	
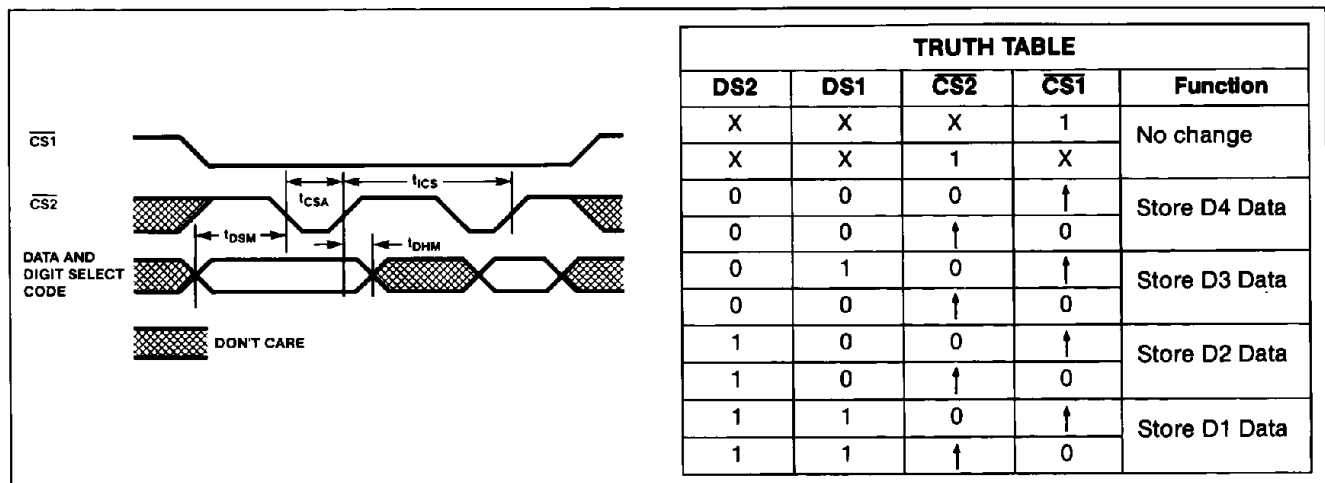
Figure 11. Microprocessor Interface input timing diagram and truth table.

/VI/IXI/VI

150Hz is too high a frequency when driving very large displays or low threshold displays with high segment trace resistance. When driving very large displays (>1" height), the very large capacitance of the display will significantly slow the rise and fall times of the backplane and segment drivers. These drivers are designed to have matching rise and fall times, but any residual mismatch will result in a DC offset across the LCD. This DC offset is directly proportional to the backplane frequency, so the lowest acceptable backplane frequency (usually 30Hz) should be used when driving very large LCDs. A simple way of lowering the backplane frequency is to connect an external capacitor from the OSCillator (pin 36) to either ground or V$^+$. The graph in the Typical Characteristics curves shows the relationship between the value of this external capacitor and the backplane frequency. The backplane frequency can also be controlled by externally driving the OSCillator pin. Figure 12 shows a method of setting the backplane frequency to precisely 32Hz.

If the indium traces on the LCD glass itself are very long and they have high sheet resistance, the resistance of the trace will form an RC delay with the capacitance of the LCD. The phase shift caused by this RC delay causes a small voltage to appear across the LCD segments that are supposed to be in the off state. This may cause "ghosting" or a slight turn-on of segments that are supposed to be off. Reducing the backplane frequency or using LCDs that have a higher threshold will eliminate this problem.

Annunciators or Flags

Many LCD displays have annunciators or flags in addition to the 7 segment digits. Figure 13 shows several different methods of driving LCD segments used as annunciators or flags. Output A of Figure 13 is driven by a CMOS exclusive OR (XOR) gate. The XOR's output is either the same as the backplane or the complement of the backplane, depending on the logic level on the input. With a "1" at the logic input the XOR output is the complement of the backplane and the LCD segment is turned on. Output B is connected to the backplane through a 1 MΩ resistor. When the analog switch is open, output B will be the backplane signal and the segment will be off. When the analog switch is closed, output B will be the complement of the backplane signal and the segment will be on. Output C is simply the complement of the backplane signal, and any segment (such as a decimal point) connected to output C will always be turned on. Output D is another way of turning on a decimal point, but since the voltage at D is simply the average DC voltage of the backplane signal, the total applied voltage across a segment connected to D is only 5 Vpk-pk (assuming 5V V$^+$) rather than the 10Vpk-pk drive received by a segment connected to output C. The resistor-capacitor drive method of output D should be used only with low threshold LCDs. Unused LCD segments should be tied to the backplane, NOT allowed to float. A floating segment, while usually remaining off, may be driven by leakage currents or

capacitive coupling with other segments and become a "ghost" or slightly turned on.

If one or more of the ICM7211 digits are not used, they can be used to drive annunciator segments without using any external logic. If only two annunciator segments need to be driven, connect the annunciators to segments B and D of the unused digit. That digit is then loaded with the data A2, A1 11, where A1 and A2 are the data for the two annunciators.

Three annunciators can be driven from one unused digit, but the input data to select all 8 possible combinations of annunciator states must be obtained from a look-up table. Two possible arrangements are shown in Table 2.

Driving an 8 Digit LCD with Common Backplane

In order to drive 8 LCD digits that have a common backplane, the backplanes of two ICM7211s must be synchronized. In figure 14 the left hand ICM7211's Backplane pin is turned into an input by grounding its oscillator pin. The right hand ICM7211 then drives both the LCD backplane and the Backplane pin of the left hand ICM7211.

Memory Mapped 8048 Microprocessor Interface

In figure 15 the digit select lines DS1 and DS2 are driven by the address latched from the 8048's multiplexed data and address bus. The data is then written into the selected digit by the $\overline{WR}$ line. The 74LS138 is used to decode eight blocks, each four bytes long, starting at address 32 (decimal). The ICM7211s are addressed by MOVX instructions to these external ram locations. The extra decoded outputs of the 74LS138 can be used as chip selects for other I/O devices.

Microprocessor Interface via I/O Port

Figure 16 shows one 8 bit I/O port driving two ICM7211s or ICM7212s. The data and digit selects are controlled by the lower 6 bits, while the upper two bits control which display driver receives the data.

Remote Display via UART

The serial input stream is assembled into an 8 bit parallel output by the UART, then the UART brings the DR (data ready) line high (See Figure 17). The schmitt trigger and RC delay drive both the $\overline{CS}$ inputs of the ICM7211s and the $\overline{DRR}$ (data ready reset) pin of the UART. When the schmitt trigger drives the $\overline{DRR}$ low, the DR pin goes low, and after a short delay, the output of the schmitt trigger output goes back high. This low-going pulse on the schmitt trigger output latches the data into the ICM7211s.

Display Interface for ICL7135 A/D

Figure 18 shows an ICM7212 interfaced to the 4½ digit A/D, ICL7135. The polarity and ½ digit segments are driven by D flip-flops that latch polarity and ½ digit data at the end of each measurement. The ICL7135
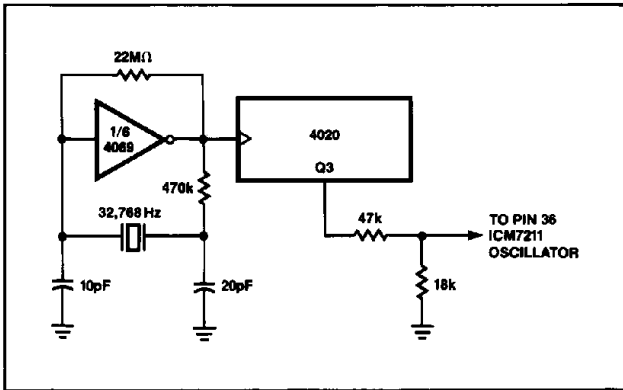
Figure 12. Crystal Controlled Backplane Frequency.

Overrange output drives the ICM7212 Brightness input, blanking the four least significant digits when the input voltage is greater than full-scale.

Similar to the LED display system, Figure 19 uses Maxim's ICM7211 LCD display driver to drive 4 digits of LCD display. The backplane signal of the ICM7211 and the CMOS exclusive OR gates are used to drive the 1/2 digit and the polarity sign. The 4 AND gates combine the ICM7135's digit outputs with its Strobe output to generate the digit select signals that latch data into the ICL7211. Since the Strobe occurs in the middle of each digit's data there is more than enough data setup and hold time to ensure that valid data is latched. The OR gates will force the BCD data to all ones when overrange goes high. The ICM7211A will blank the display when all ones (hex F) is loaded.
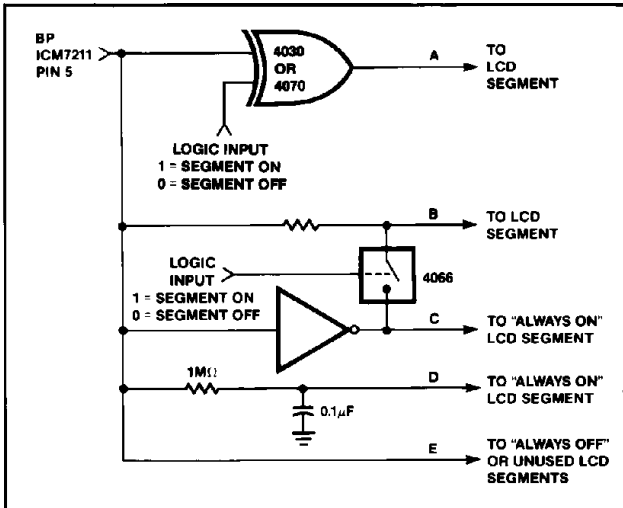

Figure 13. Driving Annunciators, Flags and Decimal Points.

SEGMENT			INPUT DATA FOR ICM7211			
F	E	A	B3	B2	B1	B0
0	0	0	0	0	0	1
0	0	1	0	0	1	1
0	1	0	1	1	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	1	0	1	1
1	1	1	0	0	0	0

0 = OFF
1 = ON

Table 2A: Using Segments to Drive Annunciators, ICM7211
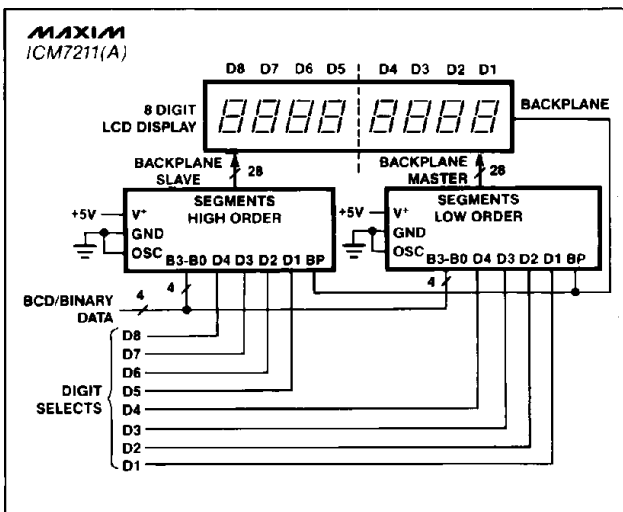
Figure 14. Two ICM7211's Driving 8-Digit LCD Display.

SEGMENT			INPUT DATA FOR ICM7211			
F	E	A	B3	B2	B1	B0
0	0	0	1	1	1	1
0	0	1	0	1	0	1
0	1	0	0	0	0	1
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	0	1	0	1	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	0

0 = OFF
1 = ON

Table 2B: Using Segments to Drive Annunciators, ICM7211A

 MAXIM

Figure 15. 8048 Memory Mapped Interface

Figure 16. uP Interface via I/O Port

Figure 17. Remote Display via UART

Figure 18. LED Display Interface for ICL7135 A/D

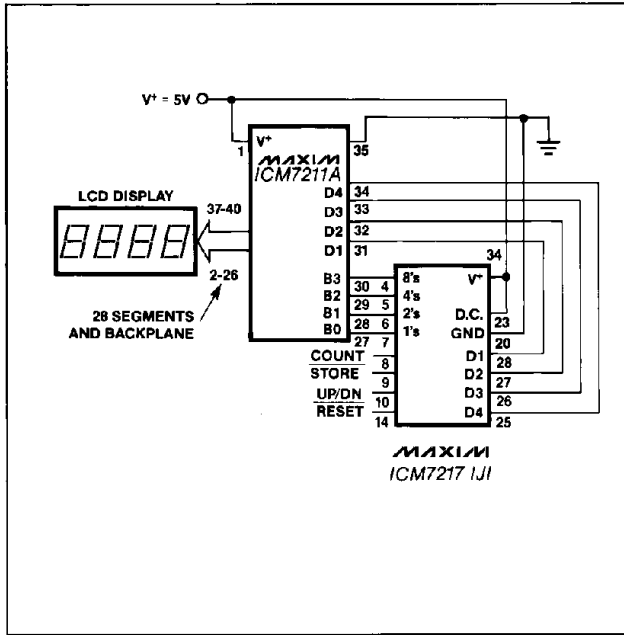Figure 19. LCD Display for ICL7135 A/D

ICM7211/7212

/V/AXI/V/ _____ 13

ICM7211/7212

Figure 20. ICM7217 to LCD Interface.
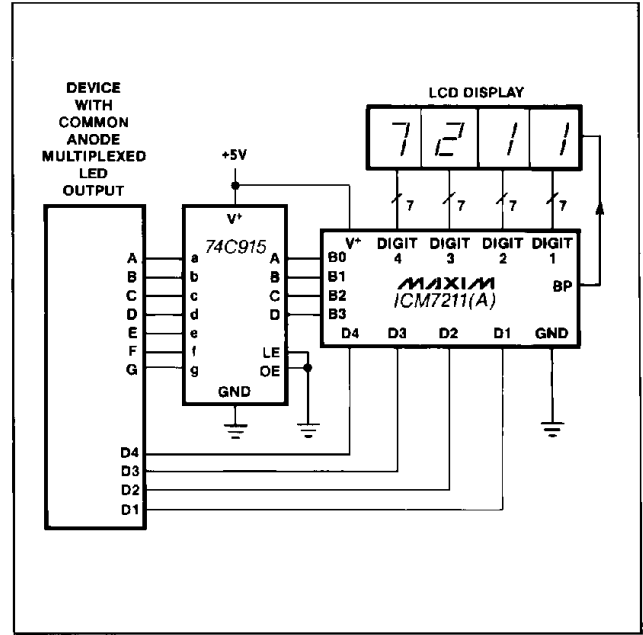
Figure 21. Multiplexed LED Driver to LCD Interface.

/VI/IXI/VI

ICM7211, 7211A

ICM7211M, 7211AM

ICM7212, 12A

ICM7212M, 7212AM

Four Digit Display
Decoder/Drivers

40 Lead Plastic (PL)

$\theta_{JA} = 100°C/W$

$\theta_{JC} = 45°C/W$

44 Lead Plastic Chip Carrier (Quad Pack) (Q)
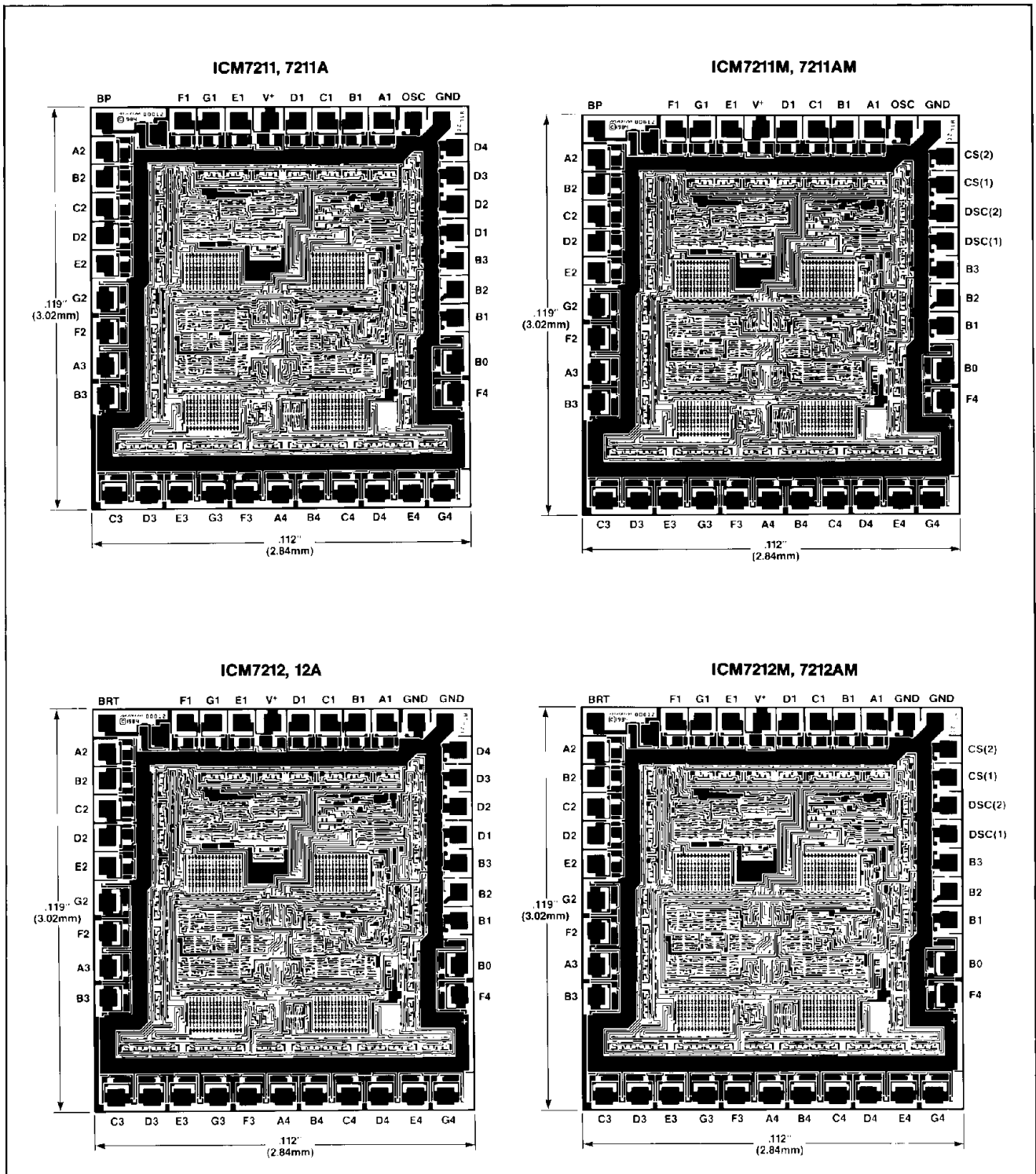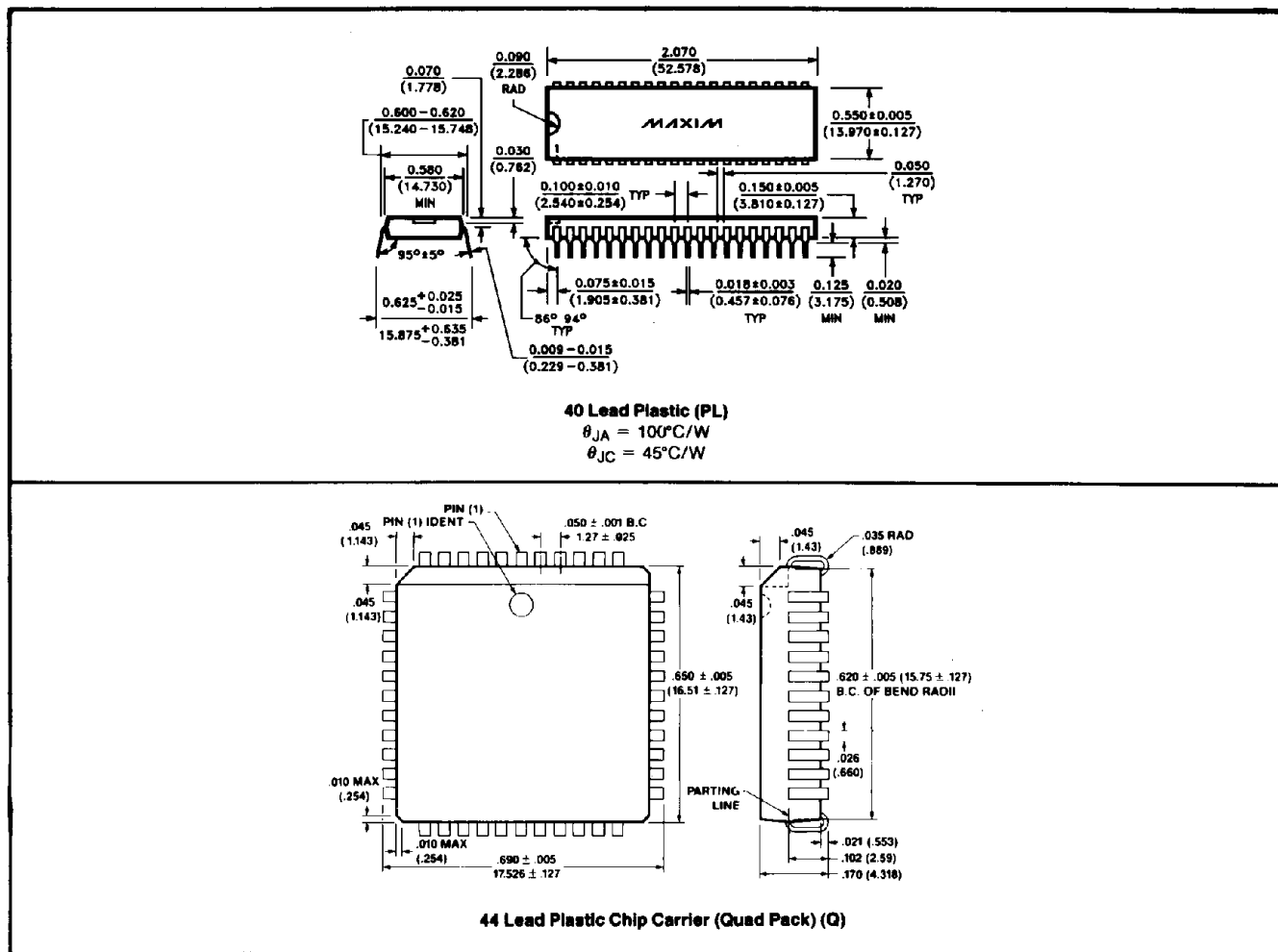
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