International **IOR** Rectifier

# *SELF-OSCILLATING FULL-BRIDGE DRIVER IC*

Features

- ■ Integrated 600V Full-Bridge Gate Driver
- ■ CT, RT programmable oscillator
- ■ 15.6V Zener Clamp on VCC
- ■ Micropower Startup
- ■ Logic Level Latched Shutdown Pin
- ■ Non-latched shutdown on CT pin (1/6th VCC)

- ■ Internal bootstrap FETs
- ■ Excellent Latch Immunity on All Inputs & Outputs
- ■ ESD Protection on All Pins
- ■ 14-lead SOIC or PDIP package
- ■ 1.0 usec (typ.) internal deadtime

Description

The IRS2453D is based on the popular IR2153 self-oscillating half-bridge gate driver IC, and incorporates a high voltage full-bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer. HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. Noise immunity is achieved with low di/dt peak of the gate drivers, and with a undervoltage lockout hysteresis greater than 1.5V. The IRS2453D also includes latched and non-latched shutdown pins.

Package

14 Lead PDIP
IRS2453DPbF

14 Lead SOIC
(Narrow Body)
IRS2453DSPbF
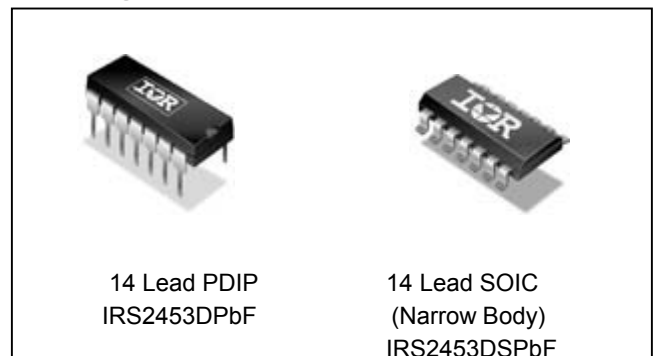
Typical Connection Diagram
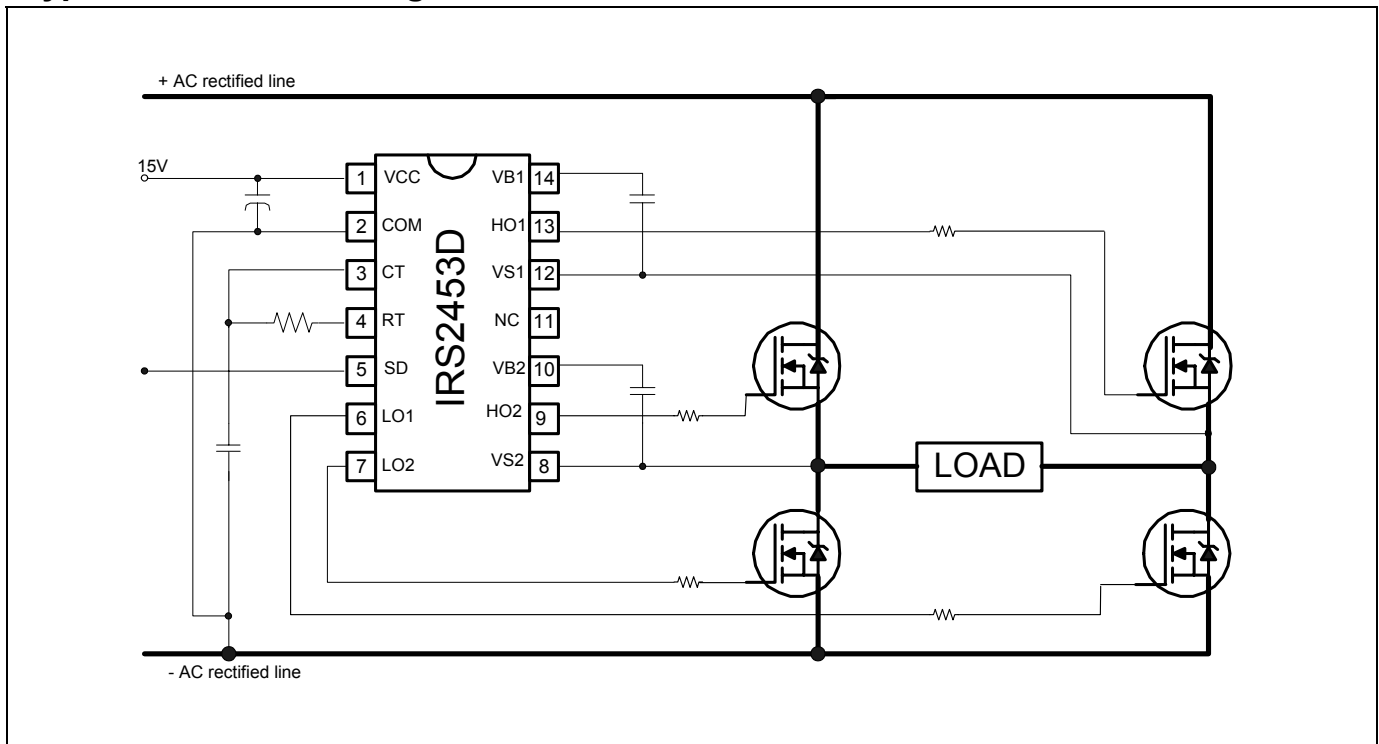
*   *Please note that this datasheet contains advanced information which could change before the product is released to production.*

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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Parameter		Min.	Max.	Units
Symbol	Definition			
V_{B1}, V_{B2}	High Side Floating Supply Voltage	-0.3	625	V
V_{S1}, V_{S2}	High Side Floating Supply Offset Voltage	$V_B - 25$	$V_B + 0.3$	V
V_{HO1}, V_{HO2}	High-Side Floating Output Voltage	$V_S - 0.3$	$V_B + 0.3$	V
V_{LO1}, V_{LO2}	Low-Side Output Voltage	-0.3	$V_{CC} + 0.3$	V
V_{RT}	R_T Pin Voltage	-0.3	$V_{CC} + 0.3$	V
V_{CT}	C_T Pin Voltage	-0.3	$V_{CC} + 0.3$	V
V_{SD}	SD Pin Voltage	-0.3	$V_{CC} + 0.3$	V
I_{RT}	R_T Pin Current	-5	5	mA
I_{CC}	Supply Current (Note 1)	---	25	mA
dV_S/dt	Allowable Offset Voltage Slew Rate	-50	50	V/ns
P_D	Maximum Power Dissipation @ $T_A \le +25ºC$, 8-Pin DIP	---	1.0	W
P_D	Maximum Power Dissipation @ $T_A \le +25ºC$, 8-Pin SOIC	---	0.625	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, 8-Pin DIP	---	125	ºC/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, 8-Pin SOIC	---	200	ºC/W
T_J	Junction Temperature	-55	150	ºC
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	---	300	

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

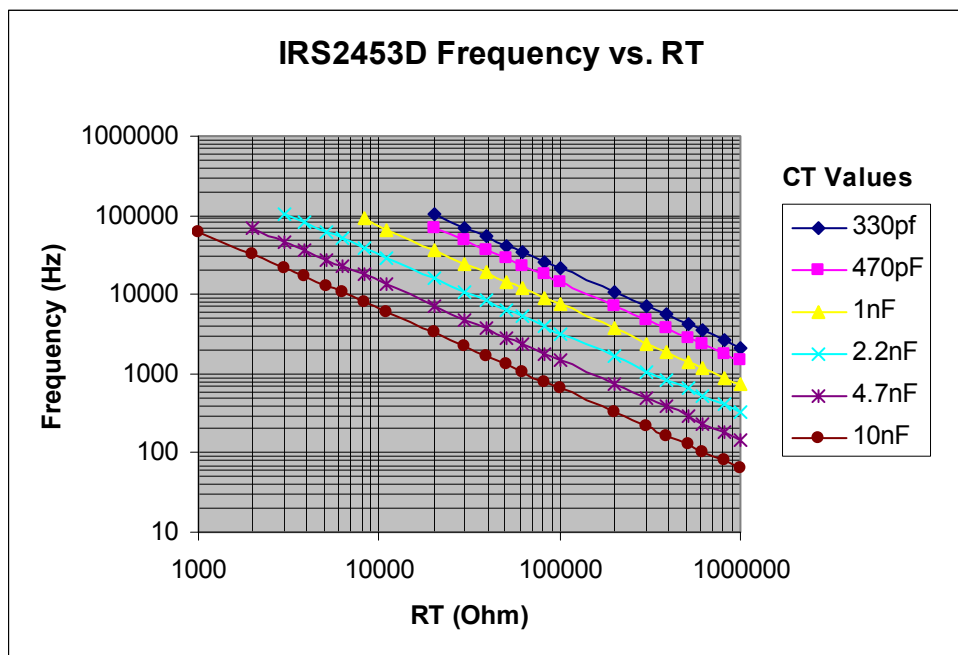| Parameter		Min.	Max.	Units
Symbol	**Definition**			
V_{BS1}, V_{BS2}	High Side Floating Supply Voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_{S1}, V_{S2}	Steady State High Side Floating Supply Offset Voltage	-3.0 (Note 2)	600	V
V_{CC}	Supply Voltage	VCCUV+	V_{CLAMP}	V
I_{CC}	Supply Current	(Note 3)	5	mA
T_J	Junction Temperature	-25	125	ºC

Note 2: Care should be taken to avoid output switching conditions where the V_S node flies inductively below ground by more than 5V.

Note 3: Enough current should be supplied to the V_{CC} pin of the IC to keep the internal 15.6V zener diode clamping the voltage at this pin.

Recommended Component Values

Parameter		Min.	Max.	Units
Symbol	**Component**			
R_T	Timing Resistor Value	1	---	kΩ
C_T	C_T Pin Capacitor Value	330	---	pF

VBIAS (VCC, VBS) = 14V, VS=0V and TA = 25°C, CLO1=CLO2 = CHO1=CHO2 = 1nF.

IRS2453D Frequency vs. RT

CT Values
- 330pf
- 470pF
- 1nF
- 2.2nF
- 4.7nF
- 10nF

Electrical Characteristics

VBIAS (VCC, VBS) = 14V, CT = 1 nF and TA = 25°C unless otherwise specified. The VO and IO parameters are referenced to COM and are applicable to the respective output leads: HO or LO. CLO1=CLO2=CHO1=CHO2=1nF.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Voltage Supply Characteristics						
V_{CCUV+}	Rising V_{CC} Undervoltage Lockout Threshold	10.0	11.0	12.0	V	
V_{CCUV-}	Falling V_{CC} Undervoltage Lockout Threshold	8.0	9.0	10.0		
$V_{CCUVHYS}$	V_{CC} Undervoltage Lockout Hysteresis	1.6	2.0	2.4		
I_{QCCUV}	Micropower Startup V_{CC} Supply Current	---	140	200	µA	$V_{CC} \leq V_{CCUV-}$
I_{QCC}	Quiescent VCC Supply Current	---	1.3	2.0	mA	
V_{CLAMP}	V_{CC} Zener Clamp Voltage	14.6	15.6	16.6	V	I_{CC} = 5mA
Floating Supply Characteristics						
I_{QBS1UV}, I_{QBS2UV}	Micropower Startup V_{BS} Supply Current	---	3	10	µA	$V_{CC} \leq V_{CCUV-}$, $V_{CC} = V_{BS}$
I_{QBS1}, I_{QBS2}	Quiescent V_{BS} Supply Current	---	60	100	µA	
V_{BS1UV+}, V_{BS2UV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.0	9.0	10.0	V	
V_{BS1UV-}, V_{BS2UV-},	V_{BS} Supply Undervoltage negative Going Threshold	7.0	8.0	9.0		
I_{LK1}, $ILK2$	Offset Supply Leakage Current	---	---	50	µA	$V_B = V_S$ = 600V
Oscillator I/O Characteristics						
f_{OSC}	Oscillator Frequency	19.6	20.2	20.8	kHz	R_T = 36.5kΩ
		89	95	101		R_T = 7.15kΩ
d	R_T Pin Duty Cycle	48	50	52	%	f_o < 100kHz
I_{CT}	C_T Pin Current	---	0.05	1.0	µA	
I_{CTUV}	UV-Mode C_T Pin Pulldown Current	1	5	---	mA	V_{CC} = 7V
V_{CT+}	Upper C_T Ramp Voltage Threshold	---	9.1	---	V	
V_{CT-}	Lower C_T Ramp Voltage Threshold	---	4.8	---		
V_{RT+}	High-Level R_T Output Voltage, V_{CC} - V_{RT}	---	10	50	mV	I_{RT} = 100µA
		---	100	300	mV	I_{RT} = 1mA
V_{RT-}	Low-Level R_T Output Voltage	---	10	50	mV	I_{RT} = 100µA
		---	100	300	mV	I_{RT} = 1mA
V_{RTUV}	UV-Mode R_T Output Voltage	---	0	100	mV	$V_{CC} \leq V_{CCUV-}$

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Electrical Characteristics

VBIAS (VCC, VBS) = 14V, CT = 1 nF and TA = 25°C unless otherwise specified. The VO and IO parameters are referenced to COM and are applicable to the respective output leads: HO or LO. CLO1=CLO2=CHO1=CHO2=1nF.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Gate Driver Output Characteristics						
V_{OH}	High-Level Output Voltage, V_{BIAS} - V_O	---	VCC	---		I_O = 0A
V_{OL}	Low-Level Output Voltage, V_O	---	COM	---		I_O = 0A
V_{OL_UV}	UV-Mode Output Voltage, V_O	---	COM	---		I_O = 0A, $V_{CC} \leq V_{CCUV-}$
t_r	Output Rise Time	---	120	220	nsec	
t_f	Output Fall Time	---	50	100		
t_{sd}	Shutdown Propagation Delay	---	275	---		
t_d	Output Deadtime (HO or LO)	0.75	1.0	1.50	μsec	
IO+	Output source current	---	180	---	mA	
IO-	Output sink current	---	260	---		
Shutdown						
V_{SD}	Shutdown Threshold at SD pin (latched)	---	2.0	---	V	
V_{CTSD}	C_T Voltage Shutdown Threshold (non latched)	---	2.3	---	V	
V_{RTSD}	SD-Mode R_T Output Voltage, V_{CC} - V_{RT}	---	10	50	mV	I_{RT} = 100μA, V_{CT} = 0V
		---	100	300	mV	I_{RT} = 1mA, V_{CT} = 0V
Bootstrap FET Characteristics						
VB1_ON VB2_ON	VB when the bootstrap FET is on	---	13.7	---	V	
IB1_CAP IB2_CAP	VB source current when FET is on	30	55	---	mA	CBS=0.1uF
IB1_10V IB2_10V	VB source current when FET is on	8	12	---		VB=10V

Lead Assignment
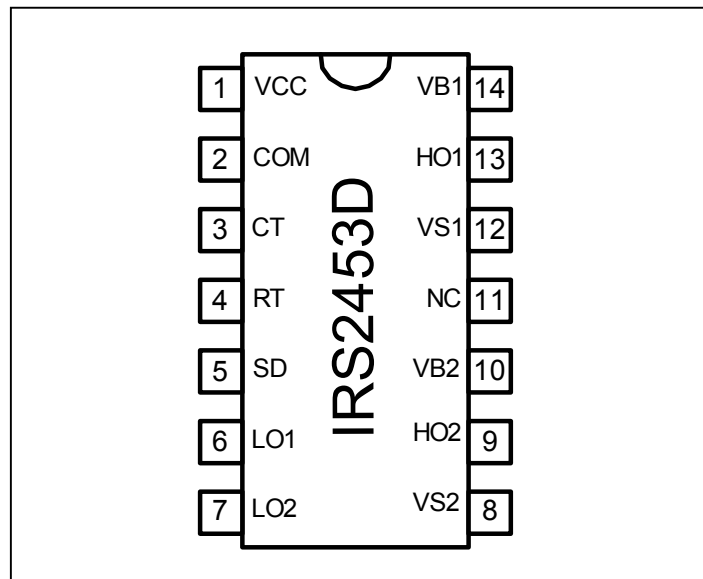
Lead Definitions

Lead		
Pin	**Symbol**	**Description**
1	VCC	Logic and internal gate drive supply voltage
2	COM	IC power and signal ground
3	CT	Oscillator timing capacitor input
4	RT	Oscillator timing resistor input
5	SD	Shutdown input
6	LO1	Low-side gate driver output
7	LO2	Low-side gate driver output
8	VS2	High voltage floating supply return
9	HO2	High-side gate driver output
10	VB1	High side gate driver floating supply
11	NC	No connect
12	VS1	High voltage floating supply return
13	HO1	High-side gate driver output
14	VB1	High side gate driver floating supply

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IRS2453DPbF

Functional Block Diagram
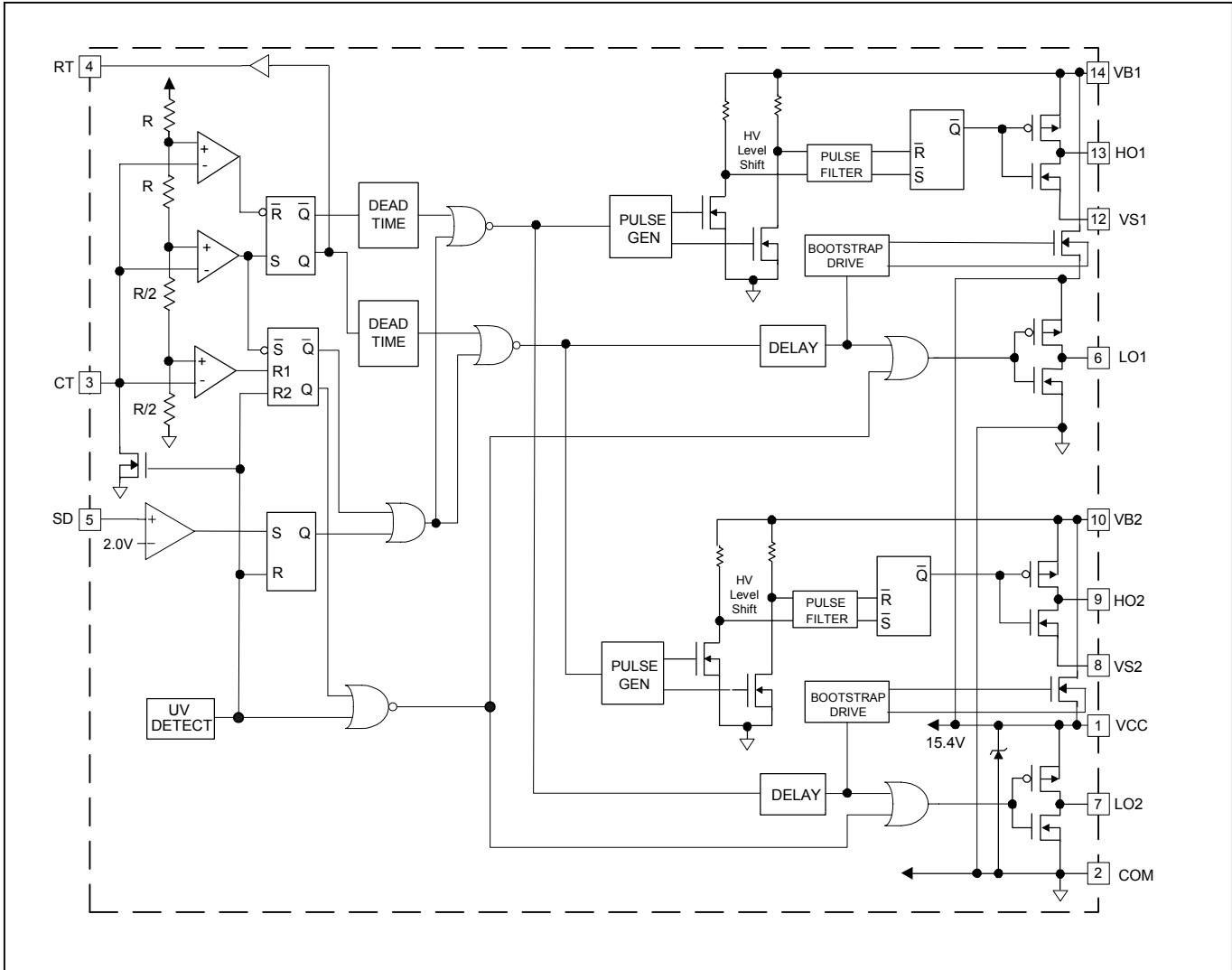
All values are typical.

Timing Diagram

VCC

VCCUV+

Fault mode
VCT<1/6*VCC

2/3 VCC
1/3 VCC
1/6 VCC

LO1   VCC

LO2   VCC   DT

HO1   VCC   DT

HO2   VCC   DT

VRT   VCC

IRT   1mA   -1mA
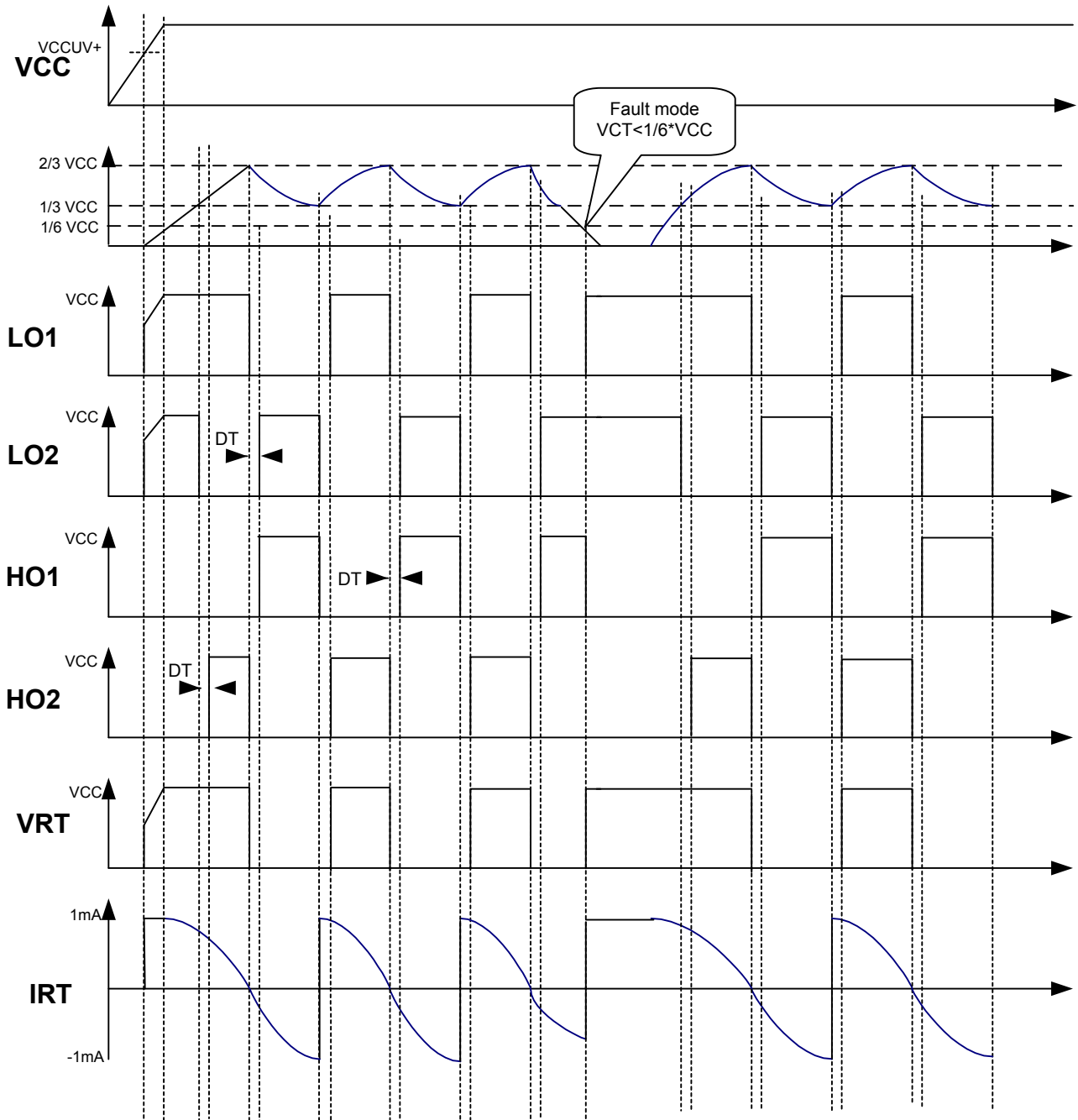
Functional Description

Under-voltage Lock-Out Mode (UVLO)
The under-voltage lockout mode (UVLO) is defined as the state the IC is in when VCC is below the turn-on threshold of the IC. The IRS2453D under voltage lock-out is designed to maintain an ultra low supply current of less than 150uA, and to guarantee the IC is fully functional before the high and low side output drivers are activated. During under voltage lock-out mode, the high and low-side driver outputs LO1, LO2, HO1, HO2 are all low. With VCC above the VCCUV+ threshold, the IC turns on and the output begin to oscillate.

Normal operating mode
Once VCC reaches the start-up threshold VCCUV+, the MOSFET M1 opens, RT increases to approximately VCC (VCC-VRT+) and the external CT capacitor starts charging. Once the CT voltage reaches VCT- (about 1/3 of VCC), established by an internal resistor ladder, LO1 and HO2 turn on with a delay equivalent to the deadtime td. Once the CT voltage reaches VCT+ (approximately 2/3 of VCC), LO1 and HO2 go low, RT goes down to approximately ground (VRT-), the CT capacitor starts discharging and the deadtime circuit is activated. At the end of the deadtime, LO2 and HO1 go high. Once the CT voltage reaches VCT-, LO2 and HO1 go low, RT goes to high again, the deadtime is activated. At the end of the deadtime, LO1 and HO2 go high and the cycle starts over again.

The frequency is best determined by the graph, Frequency vs. RT, Page 3, for different values of CT. A first order approximate of the oscillator frequency can also be calculated by the following formula::

$$f \approx \frac{1}{1.453 \times RT \times CT}$$

This equation can vary slightly from actual measurements due to internal comparator over- and under-shoot delays.
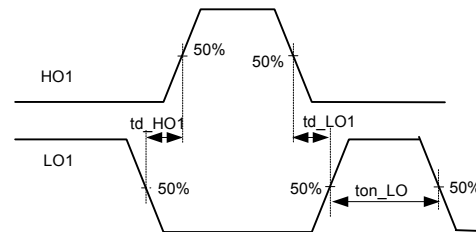
Bootstrap MOSFET
The internal bootstrap FET and supply capacitor (C_{BOOT}) comprise the supply voltage for the high side driver circuitry. The internal boostrap FET only turns on when the corresponding LO is high. To guarantee that the high-side supply is charged up before the first pulse on HO1 and HO2, LO1 and LO2 are both on when CT ramps between zero and 1/3*VCC. LO1 and LO2 are also on when CT is grounded below 1/6*VCC to ensure that the bootstrap capacitor is charged when CT is brought back over 1/3*VCC.

Non-latched Shutdown
If CT is pulled down below V_{CTSD} (approximately 1/6 of VCC) by an external circuit, CT doesn't charge up and oscillation stops. All outputs are held low and the bootstrap FETs are off. Oscillation will resume once CT is able to charge up again to VCT-.
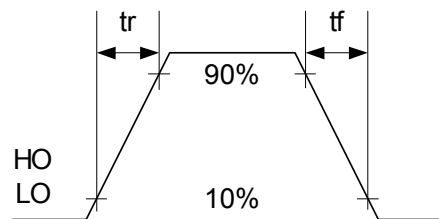
Latched Shutdown
When the SD pin is brought above 2V, the IC goes into fault mode and all outputs are low. VCC has to be recycled below VCCUV- to restart the IC. The SD pin can be used for over-current or over-voltage protection using appropriate external circuitry.
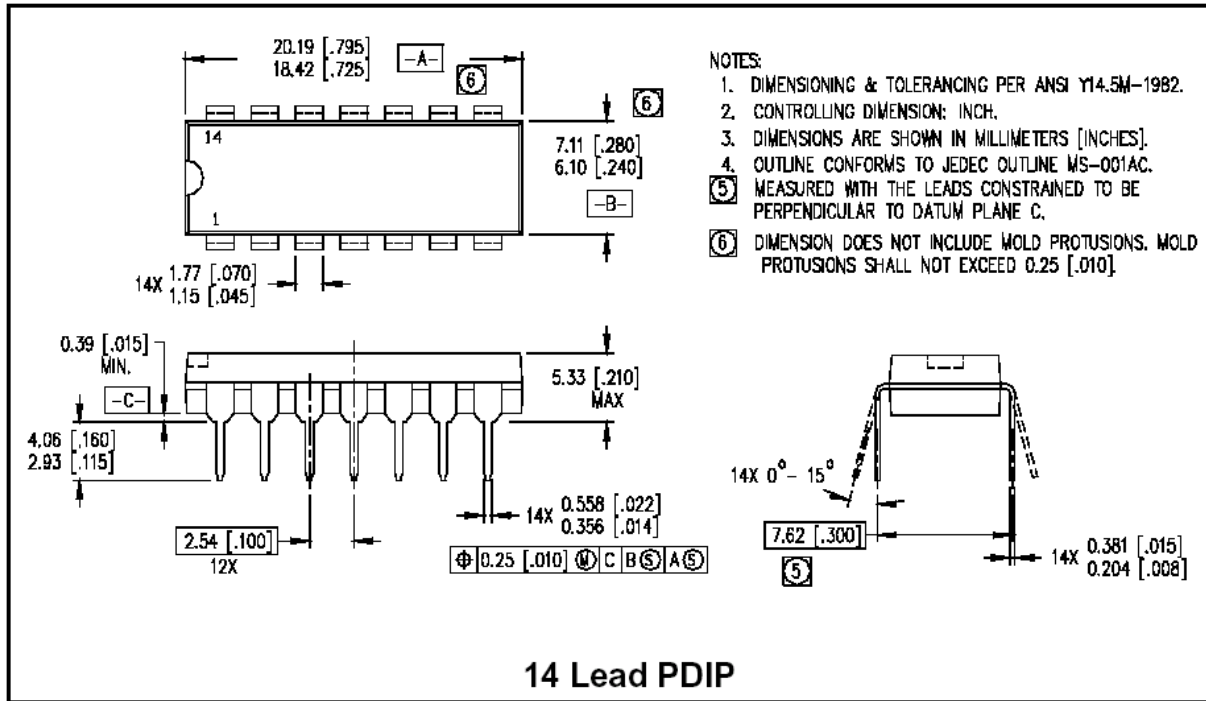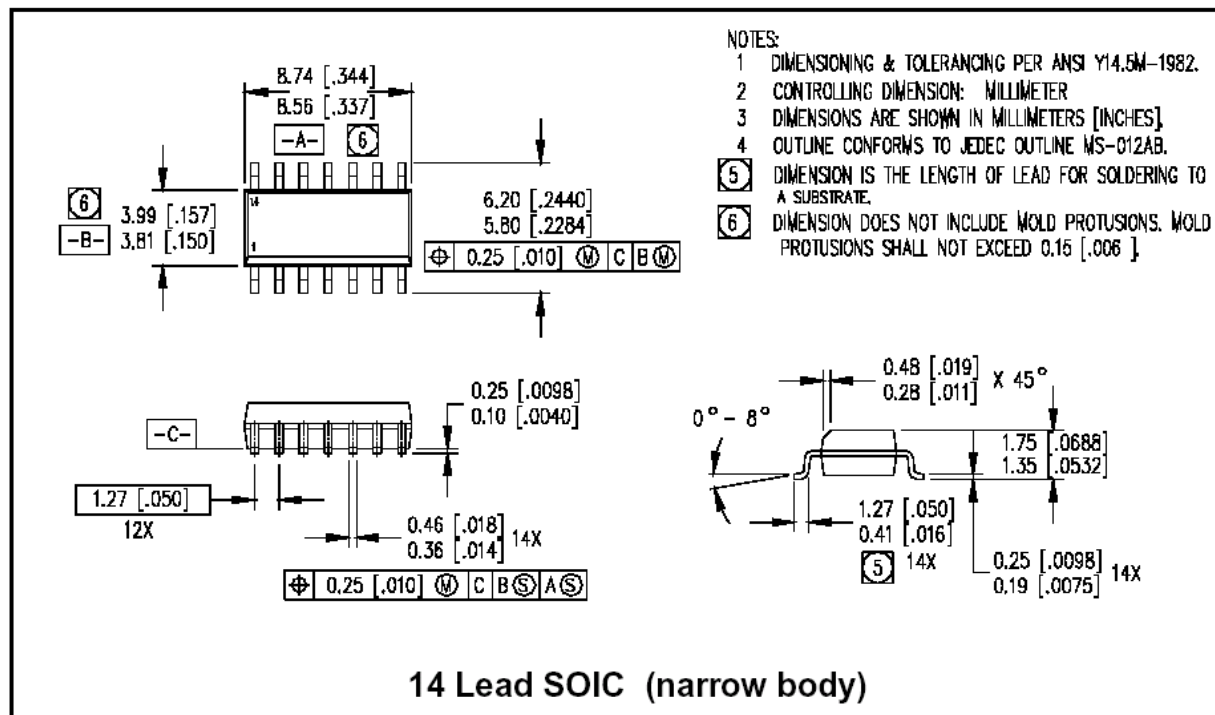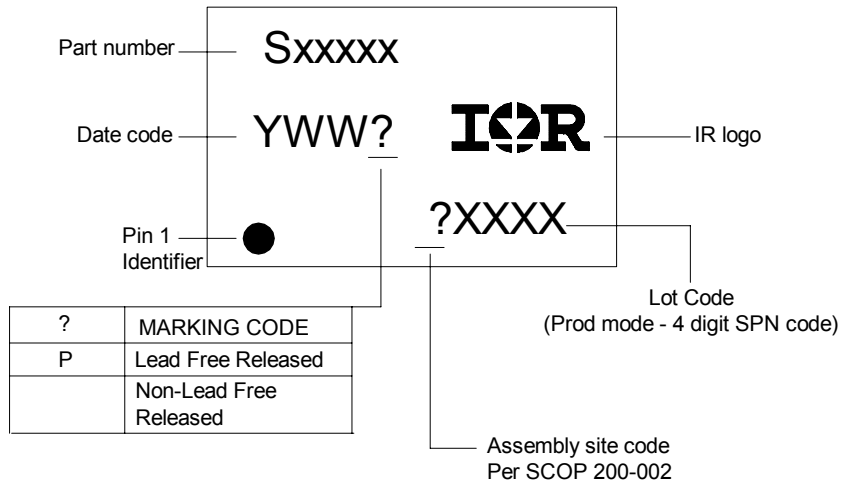

Deadtime Waveform Definitions
Deadtime waveform

Rise and fall time waveform

IRS2453DPbF

IRS2453D

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

14 Lead PDIP

IRS2453DS

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AB.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

14 Lead SOIC (narrow body)

10

Part number — Sxxxxx

Date code — YWW?

Pin 1 Identifier —

IOR — IR logo

?XXXX

Lot Code
(Prod mode - 4 digit SPN code)

?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Assembly site code
Per SCOP 200-002

ORDER INFORMATION

8-lead PDIP: order IRS2453DPbF
8-lead SOICN: order IRS2453DSPbF
8-lead SOICN tape & reel: order IRS2453DSTRPbF