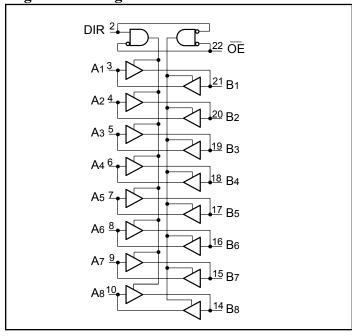


8-Bit Dual Supply Bus Transceiver with Configurable Output Voltage and 3-State Outputs

Product Features

- 2.7V to 3.6V on A-port and 3V to 5.5V on B-port
- Latch-up performance exceeds 200mA Per JESD78
- ESD protection exceeds JESD22
 2000V Human-Body Model (A114-B)
 200V Machine Model (A115-A)
- Industrial Temperature: -40°C to +85°C
- Packages (Pb-free available):
 - 24-pin 173-mil wide plastic TSSOP (L) (Pb-free & Green available)
 - 24-pin 150-mil wide plastic OSOP (O)
 - 24-pin 300-mil wide plastic SOIC (S)

Logic Block Diagram



Truth Table⁽¹⁾

Inputs		Outputs
ŌE	DIR	
L	L	Bus B Data to Bus A
L	Н	Bus A Data to Bus B
Н	X	Z (Isolation)

Note:

- H = High Signal Level
 X = Don't Care or Irrelevant
- L = Low Signal Level Z = High Impedance

1

Product Description

Pericom Semiconductor's PI74LVC series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed.

The PI74LVCC3245A is a non-inverting 8-bit Bidirectional Transceiver that uses two seperate power supply rails. A-port (V_{CCA}) is set to operate at 3.3V and B-port (V_{CCB}) is set to operate from 3.3V to 5V. This allows for translation from a 3.3V to a 5V environment and vice-versa. This tranceiver is designed for asynchronous two-way communication between data buses. The direction control input pin (DIR) determines the dataflow from the A bus to the B bus or from the B bus to the A bus. The output enable (\overline{OE}) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

Product Pin Configuration

(3.3V) V _{CCA}	1	24 D V	CCB (3.3V to 5V)
DIR [2	23 🗆 N	IC
A1 [3	22 D C	DΕ
A2 [4	21 B	1
A3 [5	20 B	2
A4 [6	19 🛭 B	3
A5 [7	18 🛭 B	4
A6 [8	17 🛭 B	5
A7 [9	16 🛭 B	6
A8 [10	15 🛭 B	7
GND [11	14 🕽 B	8
GND [12	13 🛭 G	AND

Product Pin Description

roduct i in Description				
Pin Name	Description			
ŌĒ	3-State Output Enable Inputs (Active LOW)			
DIR	Direction Control Input			
Ax	Side A Inputs or 3-State Outputs			
Bx	Side B Inputs or 3-State Outputs			
NC	NO Internal Connect			
GND	Ground			
V _{CCA} ,V _{CCB}	Power			

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

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Supply voltage range, V _{CCA} and V _{CCB}	-0.5V to +7V
Input voltage range, $V_I^{(2)}$: I/O ports (A-port)	$-0.5V$ to $V_{CCA} + 0.5V$
I/O ports (B-port)	0.5V to V _{CCB} +0.5V
Control Pins	$-0.5V$ to $V_{CCA} + 0.5V$
Input clamp current, I _{IK} (V _I <0)	50mA
Output clamp current, I _{OK} (V _O <0)	50mA
Continous Output Current IO	±50mA
Continous Current through each V _{CC} or GND pin	
Package thermal impedance, $\theta_{JA}^{(3)}$: package L	84°C/W
package Q	
package S	79°C/W
Storage Temperature range, T _{stg}	65°C to 150°C

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

- 2. This value is limited to 7V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

2



Recommended Operating Conditions⁽⁴⁾

Parameter	Description		V _{CCA}	V _{CCB}	Min.	Nom.	Max.	Units
V _{CCA}	Supply Voltage				2.7	3.3	3.6	
V _{CCB}	Supply Voltage				3	5	5.5	
			2.7V	3V	2			
V_{IHA}	High-Level Input Voltage	$V_{OB} \le 0.1 V$ or $V_{OB} \ge V_{CCB} - 0.1 V$	3.0V	3.6V	2			
		OI VOB \(\times\) VCCB \(\times\). I V	3.6V	5.5V	2			
			2.7V	3V	2			
V_{IHB}	High-Level Input Voltage	$V_{OA} \le 0.1V$ or $V_{OA} \ge V_{CCA} - 0.1V$	3.0V	3.6V	2			
		or voa = vcca =0.1 v	3.6V	5.5V	3.85			
			2.7V	3V			0.8	
V_{ILA}	Low-Level Input Voltage	$V_{OB} \le 0.1 V$ or $V_{OB} \ge V_{CCB} - 0.1 V$	3.0V	3.6V			0.8	
		OI VOB = VCCB =0.1 V	3.6V	5.5V			0.8	
			2.7V	3V			0.8	
$V_{\rm ILB}$	Low-Level Input Voltage	$V_{OA} \le 0.1V$ or $V_{OA} \ge V_{CCA} - 0.1V$	3.0V	3.6V			0.8	V
		or voa = vcca o.i v	3.6V	5.5V			1.65	
		$V_{OA} \le 0.1V$	2.7V	3V	2			
V _{IH} High-Level Input Voltage (Control Pins)	or $V_{OA} \ge V_{CCA} - 0.1V$,	3.0V	3.6V	2]	
	(Control Phis)	$ or V_{OB} \le 0.1V $ $ or V_{OB} \ge V_{CCB} -0.1V $	3.6V	5.5V	2			
		$V_{OA} \le 0.1V$ or $V_{OA} \ge V_{CCA} - 0.1V$,	2.7V	3V			0.8	
V_{IL}	Low-Level Input Voltage		3.0V	3.6V			0.8	
	(Control Pins)	$ or V_{OB} \le 0.1V $ $ or V_{OB} \ge V_{CCB} -0.1V $	3.6V	5.5V			0.8	
V _{IA}	Input Voltage				0		V _{CCA}	
V_{IB}	Input Voltage				0		V _{CCB}	
V _{OA}	Output Voltage				0		V _{CCA}	
V _{OB}	Output Voltage				0		V _{CCB}	
I	High-level output Current		2.7V	3V			-12	
I_{OHA}	riigii-ievei output Current		3.3V	3V			-24	
Love	High-level output Current		2.7V	3.3V			-12	
I_{OHB}	riigii-ievei output Current		3.3V	3V			-24	mA
Lov	Low-level output Current		2.7V	3V			12	IIIA
I _{OLA}	Low-level output Current		3.3V	3V			24	
I _{OLB}	Low-level output Current		2.7V	3.3V			12	
	Low-level output Current		3.3V	3V			24	
$\Delta t/\Delta v$	Input transition Rise or Fall Rate						10	ns/v
T _A	Operating Free-Air Temperature				-40		85	°C

Note: 4. All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation.

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DC Electrical Characteristics (Over the Operating Range, $T_A = -40$ °C to +85°C)

Parameters	Description	Test Conditions	V _{CCA}	V _{CCB}	Min.	Typ.	Max.	Units
		$I_{OH} = -100 \mu A$	3V	3V	2.9	3		
$ m V_{OHA}$	Minimum High Level		2.7V	3V	2.2	2.5		1
		$I_{OH} = -12mA$	3V	3V	2.4	2.8		
	Output Voltage (Port A)	. 24	3V	3V	2.2	2.6		1
		$I_{OH} = -24 \text{mA}$	2.7V	4.5V	2	2.4		
		$I_{OH} = -100 \mu A$	3V	3V	2.9	3		1
T 7	Minimum High Level	$I_{OH} = -12mA$	2.7V	3V	2.4	2.8		1
V_{OHB}	Output Voltage (Port B)	. 24	3V	3V	2.2	2.6		1
		$I_{OH} = -24 \text{mA}$	2.7V	4.5V	3.2	4.2		V
		$I_{OL} = 100 \mu A$	3V	3V			0.1	
	Maximum Low Level	$I_{OL} = 12mA$	2.7V	3V		0.1	0.5	
V_{OLA}	Output Voltage (Port A)		3V	3V		0.2	0.5	
		$I_{OL} = 24mA$	2.7V	4.5V		0.2	0.5	1
		$I_{OL} = 100 \mu A$	3V	3V			0.1	
	Maximum Low Level	$I_{OL} = 12mA$	2.7V	3V		0.1	0.5	
V_{OLB}	Output Voltage (Port B)		3V	3V		0.2	0.5	
		$I_{OL} = 24mA$		4.5V		0.2	0.5	
	Maximum Input Leakage	$V_{\rm I} = V_{\rm CCA}$ or GND	3.6V	3.6V			±1	
I_{I}	I _I Current (Control Inputs)		3.0 ,	5.5V			±1	
I _{OZ} ⁽⁵⁾	Maximum 3-State Output Leakage Current (A or B ports)	$\begin{array}{c c} V_{I} = V_{IL} \text{ or } V_{IH}, \\ \overline{OE} = V_{CCA} V_{O} = V_{CCA/B} \\ \text{ or GND} \end{array} \qquad 3.6V \qquad 3.6V$				±5		
-	Quiescent V _{CCA}	A port = V_{CCA} or GND, $I_O = 0$	3.6V	Open			10	μΑ
I_{CCA}	Supply Current	B to A, B-Port = V_{CCB}	3.6V	3.6V			10	1
		or GND, I_O (A port) = 0		5.5V			10	
т	Quiescent V _{CCB}	A to B, A port = V_{CCA}	3.6V	3.6V			10	
I_{CCB}	Supply Current	or GND, $I_O(B \text{ port}) = 0$		5.5V			10	
	I _{CC} per input (A port)	One input $V_I = V_{CCA} - 0.6V$, other inputs = V_{CCA} or GND, $\overrightarrow{OE} = GND$ and DIR = V_{CCA}	3.6V	3.6V			50	
I _{CC} ⁽⁶⁾	I_{CC} per input (\overline{OE}) I_{CC} per input (DIR)	$V_I = V_{CCA} - 0.6V$, other inputs = V_{CCA} or GND, DIR = V_{CCA}	3.6V	3.6V			50	μА
		$V_{I} = V_{CCA} - 0.6V,$ other inputs = V_{CCA} or GND, $\overline{OE} = GND$	3.6V	3.6V			50	
	I _{CC} per input (B Port)	One Input $V_I = V_{CCB} - 2.1V$, other inputs = V_{CCB} or GND, $\overline{OE} = GND$ and DIR = GND	3.6V	5.5V		0.7	1.5	mA

Notes:

6. This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0V or the associated V_{CC} .

^{5.} For I/O ports, the parameter $I_{\mbox{\scriptsize OZ}}$ includes the input leakage current.



Capacitance $(T_A = 25^{\circ}C)$

Parameters	Description	Test Co	Тур.	Units	
C_{IN}	Control Input Capacitance	$V_I = V_{CCA}$ or GND, V_C	2.6		
C _{I/O}	Input/Output Capacitance (A or B port)	$V_{I/O} = V_{CCA/B}$ or GND,	9	pF	
C	Power Dissipation Capaci-	Outputs Enabled	$V_{CCA} = 3.3V$, $V_{CCB} = 5V$	22	
C_{PD}	tance (7)	Outputs Disabled	$C_L = 0pF, f = 10MHz$	2.4	

Notes:

AC Electrical Characteristics (Over Operating Range, $T_A = -40$ °C to +85°C)

Parameters	From	То	V _{CCB} =	.7V to 3.6V, 5V ±0.5V	$V_{CCA} = 2.7V \text{ to } 3.6V,$ $V_{CCB} = 3.3V \pm 0.3V$ $C_L = 50 \text{pF}, R_L = 500 \Omega$		Units
	(Input)	(Output)		$R_{\rm L} = 500\Omega$	-	1	4
			Min.	Max.	Min.	Max.	
$t_{ m PHL}$	A	В	1	5.6	1	7.1	
$t_{\rm PLH}$	A	Б	1	5.3	1	7.2	
$t_{ m PHL}$	В		1	5.0	1	6.4	
$t_{\rm PLH}$	Б	A	1	5.2	1	6.6	
t_{PZL}	ŌĒ	A	1	8.0	1	9.0	
t _{PZH}	OE		1	7.8	1	8.8	
t_{PZL}	ŌĒ	В	1	8.1	1	9.1	ns
t _{PZH}		Б	1	8.4	1	8.8	
$t_{\rm PLZ}$	ŌĒ	A	1	7.1	1	7.3	
$t_{ m PHZ}$	OE	A	1	7.3	1	7.5	
$t_{\rm PLZ}$	ŌĒ	В	1	7	1	7.5	
t_{PHZ}	OE.		1	7	1	7.6	
t _{SK(O)}	Output-t Ske	o-Output w ⁽⁸⁾		1.5		1.5	

Note:

8. Skew between any two outputs of the same device, switching in the same direction. Parameter guaranteed by design.

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C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle, C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) +(I_{CC} static)



Power- Up Considerations

To avoid excessive supply current, bus contention or oscillation during power-up, the following guidelines should be followed:

- 1. Connect ground first before any supply voltage is applied.
- 2. Power up V_{CCA}, which is the control side of the device.
- 3. Ramp \overline{OE} ahead of or with V_{CCA} to help prevent bus contention
- 4. Ramp DIR with V_{CCA} if DIR high is needed (A bus to B bus). Otherwise keep DIR Low.

PARAMETER MEASUREMENT INFORMATION FOR A TO B PORT V_{CCA} =2.7V TO 3.6V and V_{CCB} = 5V ± 0.5V

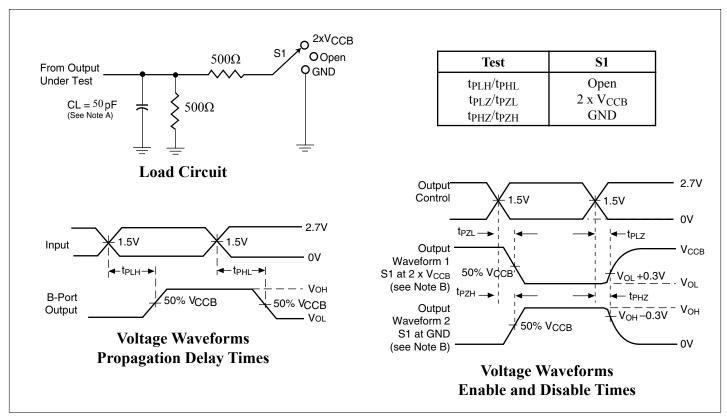


Figure 1. Load Circuit and Voltage Waveforms

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: $PRR \le 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \le 2.5 \text{ns}$, $t_F \le 2.5 \text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.



PARAMETER MEASUREMENT INFORMATION FOR B TO A PORT V_{CCA} =2.7V TO 3.6V and V_{CCB} = 5V ± 0.5V

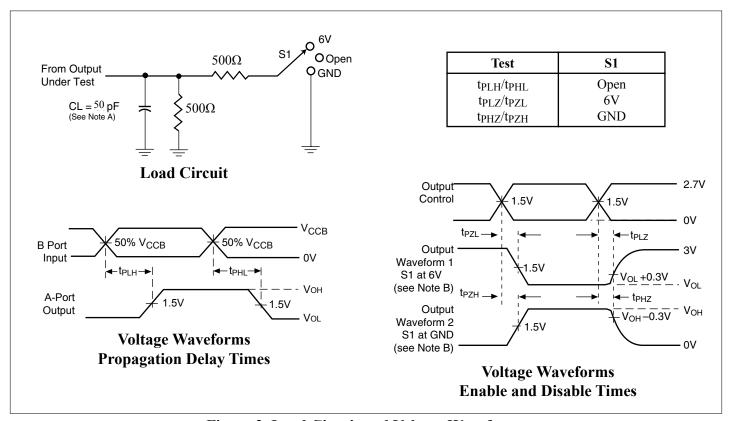


Figure 2. Load Circuit and Voltage Waveforms

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Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: $PRR \le 10 \text{ MHz}$, $Z_O = 50\Omega$, $t_R \le 2.5 \text{ns}$, $t_F \le 2.5 \text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.



PARAMETER MEASUREMENT INFORMATION FOR A TO B AND B TO A V_{CCA} =2.7V TO 3.6V and V_{CCB} = 3.3V ± 0.3V

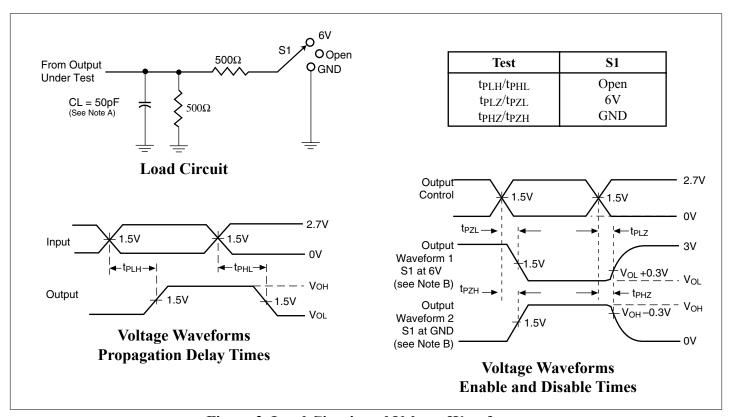


Figure 2. Load Circuit and Voltage Waveforms

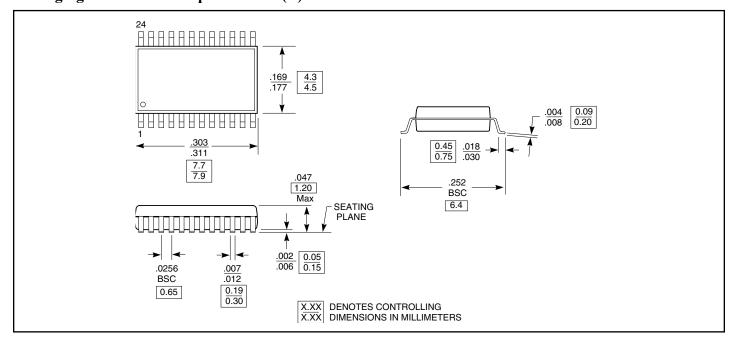
8

Notes:

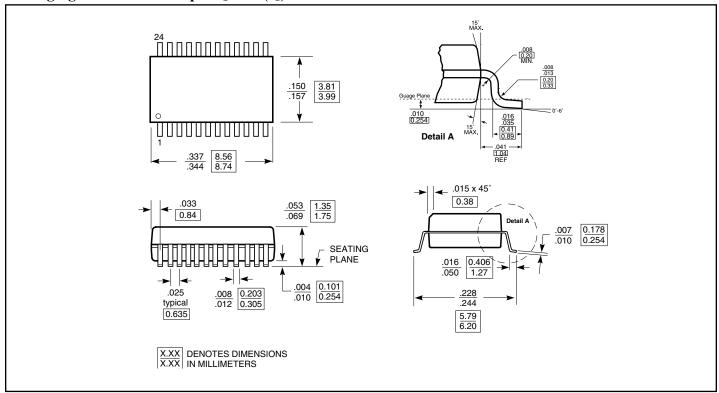
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- D. The outputs are measured one at a time with one transition per measurement.



Packaging Mechanical: 24-pin TSSOP (L)



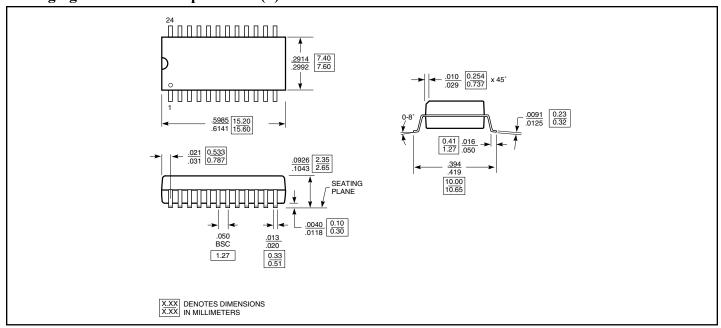
Packaging Mechanical: 24-pin QSOP (Q)



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Packaging Mechanical: 24-pin SOIC (S)



Ordering Information

Ordering Code	Package Code	Package Desription
PI74LVCC3245AL	L	24-pin, 173-mil wide plastic TSSOP
PI74LVCC3245ALE	L	Pb-free, 24-pin, 173-mil wide plastic TSSOP
PI74LVCC3245AQ	Q	24-pin, 150-mil wide plastic QSOP
PI74LVCC3245AS	S	24-pin, 300-mil wide plastic SOIC

Notes:

1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/

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