128K x 8 Static RAM

Features

- **High speed**
  - —t_{AA} = 10 ns
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **Easy memory expansion with CE and OE options**

Functional Description

The CY7C1019 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O$_0$ through I/O$_7$) is then written into the location specified on the address pins (A$_0$ through A$_{16}$).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O$_0$ through I/O$_7$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1019 is available in standard 400-mil-wide SOJs.

Logic Block Diagram

1019–1

Pin Configuration

SOJ Top View

1019–2
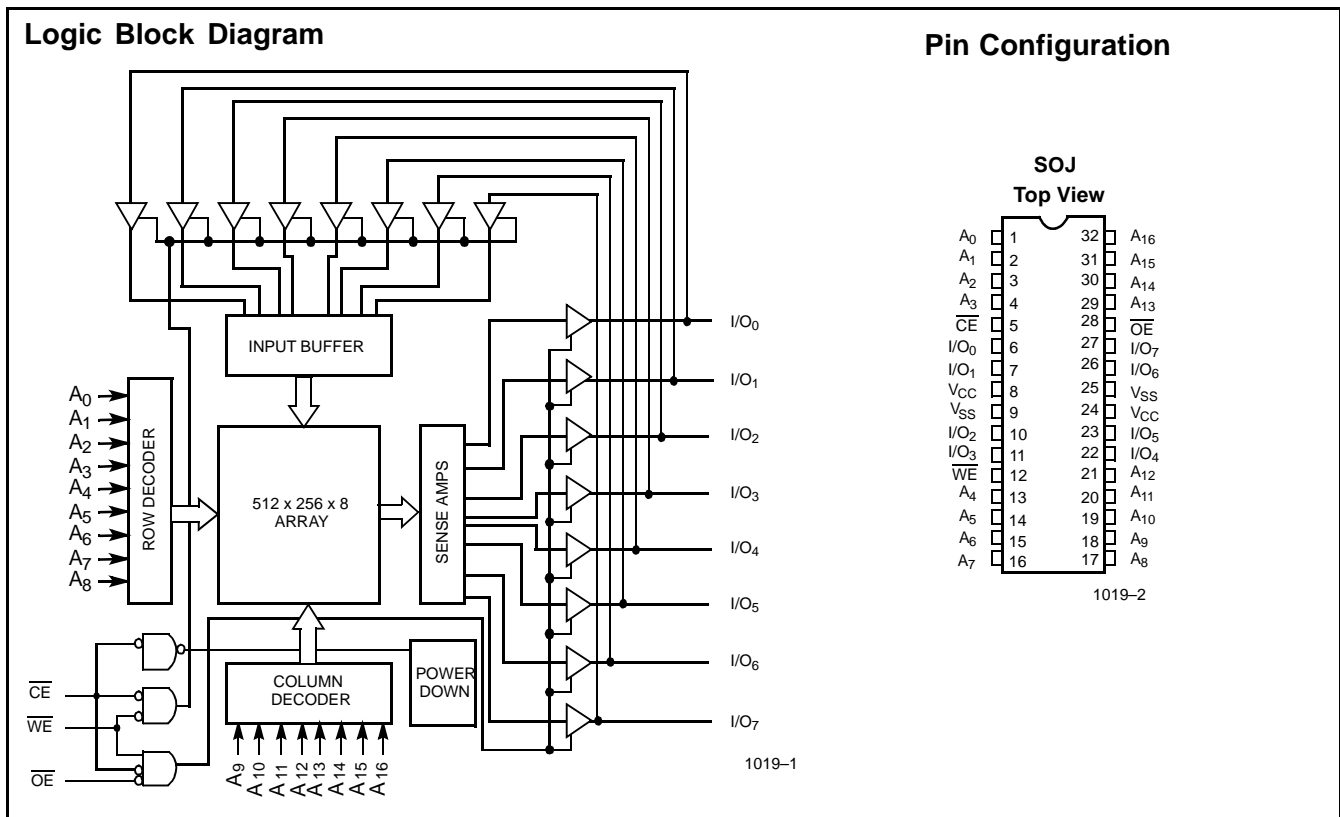
Selection Guide

		7C1019–10	7C1019–12	7C1019–15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)		240	220	200
	L	210	190	175
Maximum Standby Current (mA)		10	10	10
	L	1	1	1

Shaded areas contain advance information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied.. −55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State[1] .... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] .... −0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C1019-10 Min.	7C1019-10 Max.	7C1019-12 Min.	7C1019-12 Max.	7C1019-15 Min.	7C1019-15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{RC}			240		220		200	mA
			L		210		190		175	
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		40		40	mA
			L		20		20		20	
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V, or V_{IN} ≤ 0.3V, f=0			10		10		10	mA
			L		1		1		1	

Shaded areas contain advance information.

Capacitance[3]

| Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes:
1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms
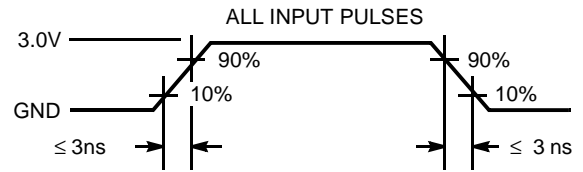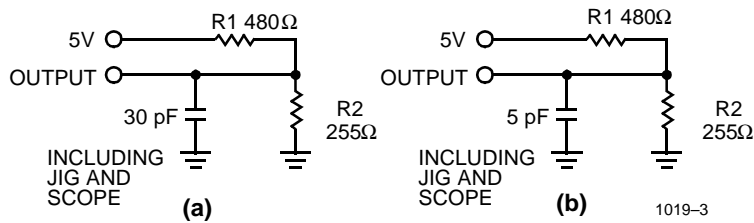
Equivalent to: THÉVENIN EQUIVALENT
OUTPUT ⚬—WW—⚬ 1.73V
        167Ω
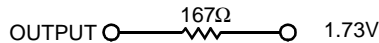
Switching Characteristics[4] Over the Operating Range

| Parameter	Description	7C1019-10 Min.	7C1019-10 Max.	7C1019-12 Min.	7C1019-12 Max.	7C1019-15 Min.	7C1019-15 Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5, 6]		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		5		6		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15	ns
WRITE CYCLE[7,8]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		ns
t_{AW}	Address Set-Up to Write End	7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		10		ns
t_{SD}	Data Set-Up to Write End	5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		5		6		7	ns

Shaded areas contain advance information.

Note:
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

## Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Conditions	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention	No input may exceed V_{CC} + 0.5V	2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 3.0V$, $\overline{CE}_1 \geq V_{CC} - 0.3V$,		300	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
t_R	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform
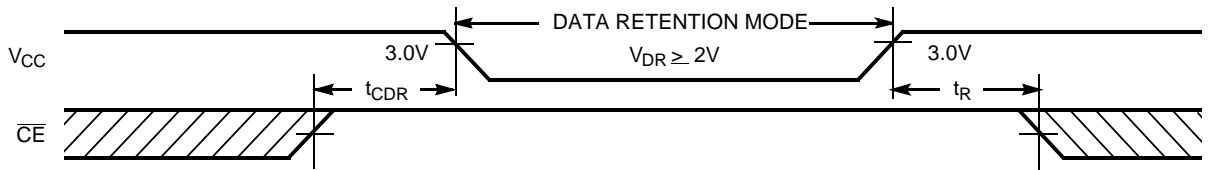
1019–5
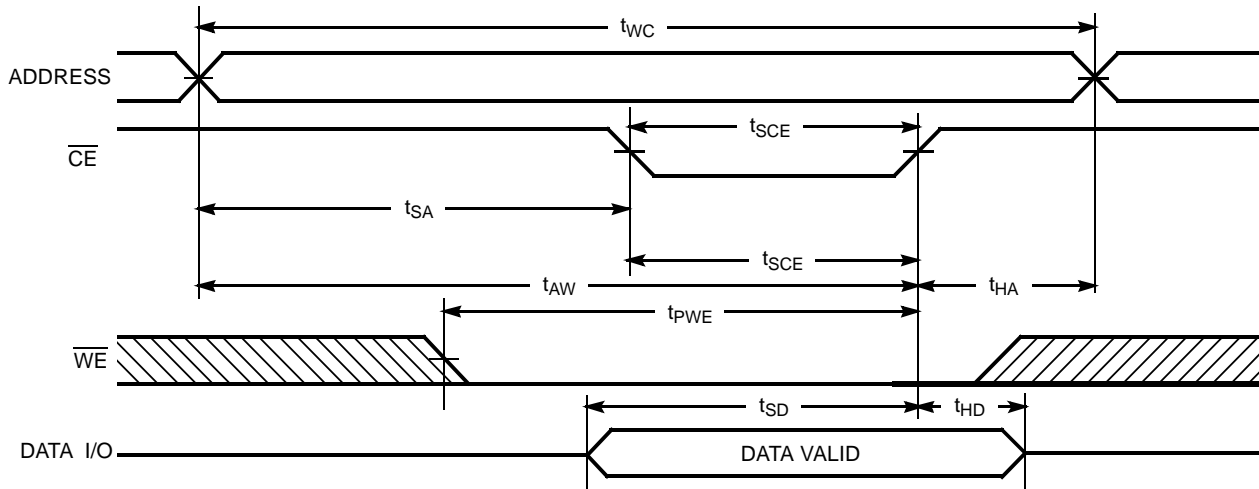
Switching Waveforms

Read Cycle No. 1[9, 10]
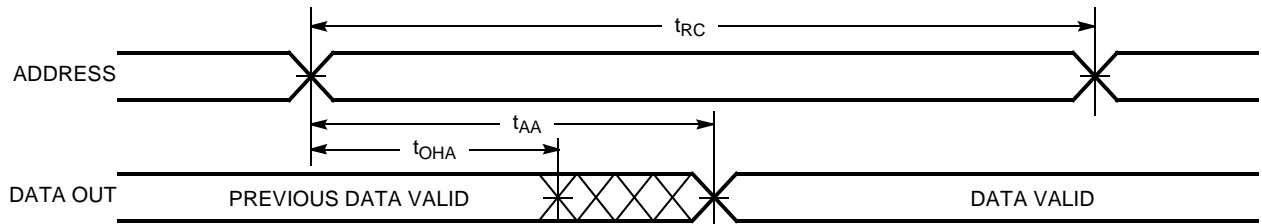
1019–6

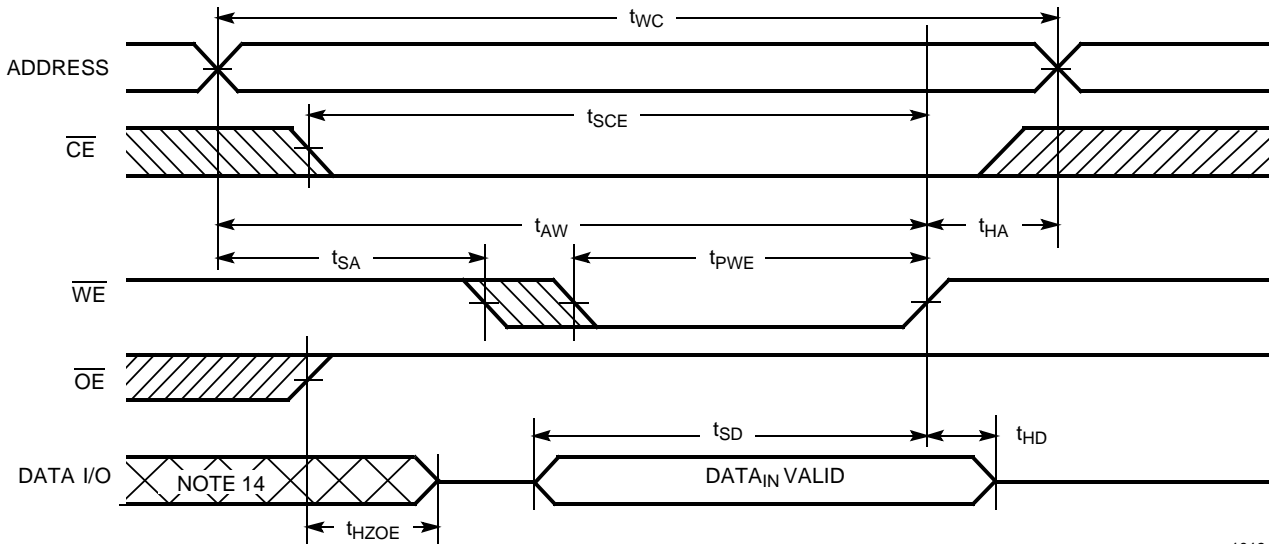**Read Cycle No. 2 ($\overline{OE}$ Controlled)**[10, 11]
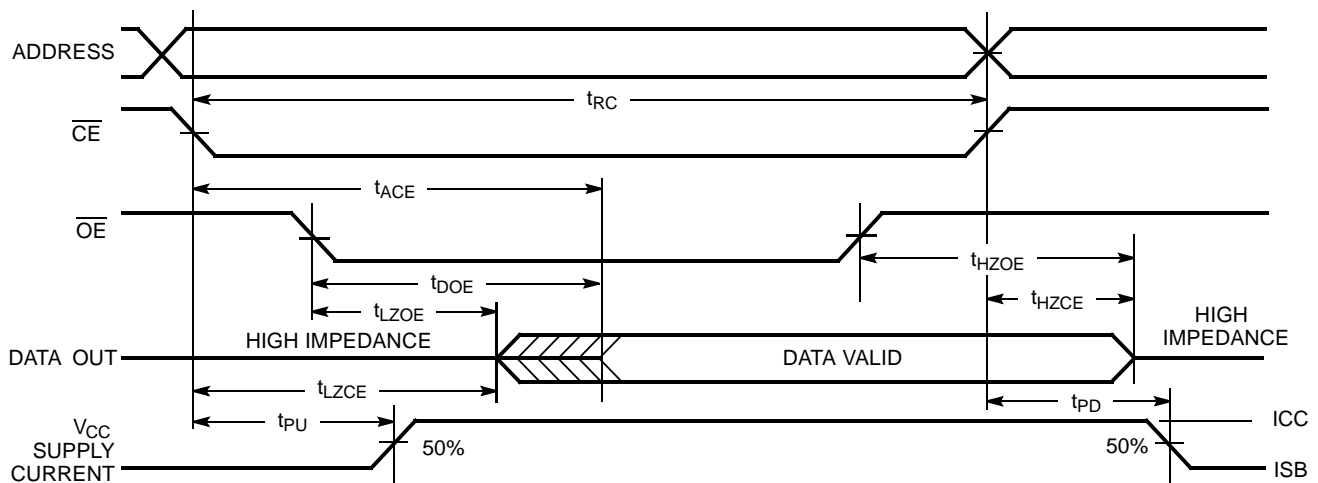
1019–7

Notes:
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

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Switching Waveforms (continued)

**Write Cycle No. 1 ($\overline{CE}$ Controlled)**[12, 13]

1019–8

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[12, 13]

1019–9

Notes:
12. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[13]
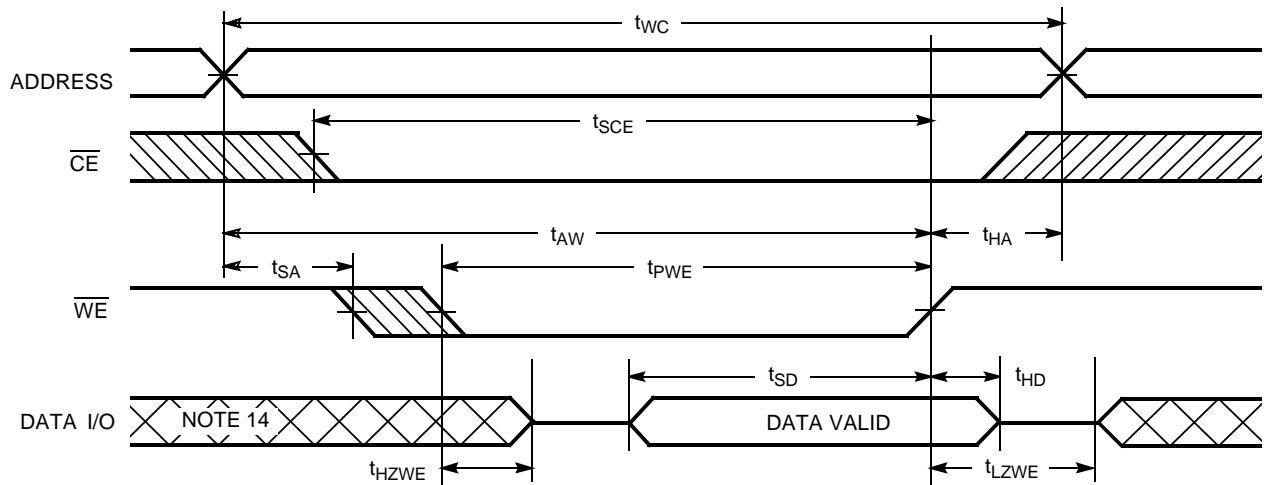
1019–10

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O$_0$–I/O$_7$	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

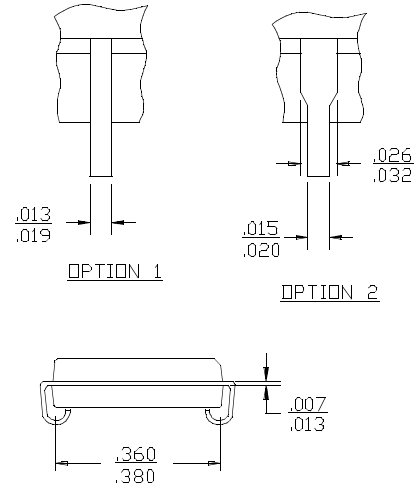| Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1019-10VC	V33	32-Lead 400-Mil Molded SOJ	Commercial
	CY7C1019L-10VC	V33	32-Lead 400-Mil Molded SOJ	
12	CY7C1019-12VC	V33	32-Lead 400-Mil Molded SOJ	Commercial
	CY7C1019L-12VC	V33	32-Lead 400-Mil Molded SOJ	
15	CY7C1019-15VC	V33	32-Lead 400-Mil Molded SOJ	Commercial
	CY7C1019L-15VC	V33	32-Lead 400-Mil Molded SOJ	

Shaded area contains advance information.

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Package Diagram

32-Lead (400-Mil) Molded SOJ V33

DIMENSIONS IN INCHES $\frac{MIN.}{MAX.}$

PIN 1 I.D
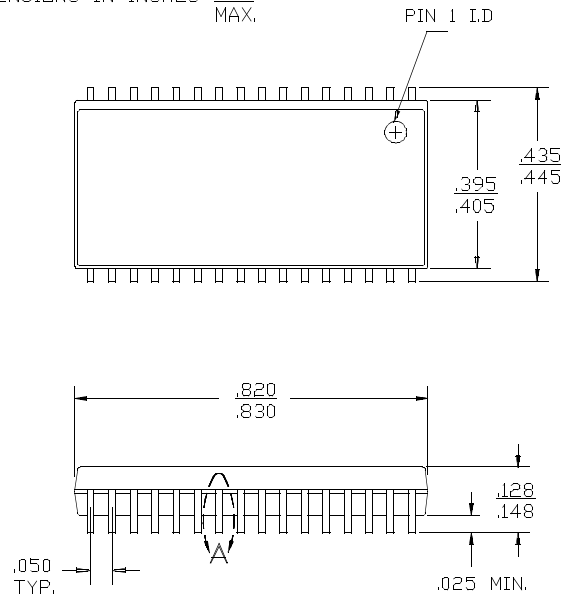
DETAIL A
EXTERNAL LEAD DESIGN

.435
.445

.395
.405

.820
.830

.128
.148

.050
TYP.

.025 MIN.

.013
.019

OPTION 1

.026
.032

.015
.020

OPTION 2

.007
.013

.360
.380

Document Title: 7C1019 128K x 8 Static RAM Document Number: 38-05055				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107246	09/10/01	SZV	Change from Spec number: 38-00440 to 38-05055