

FEATURES

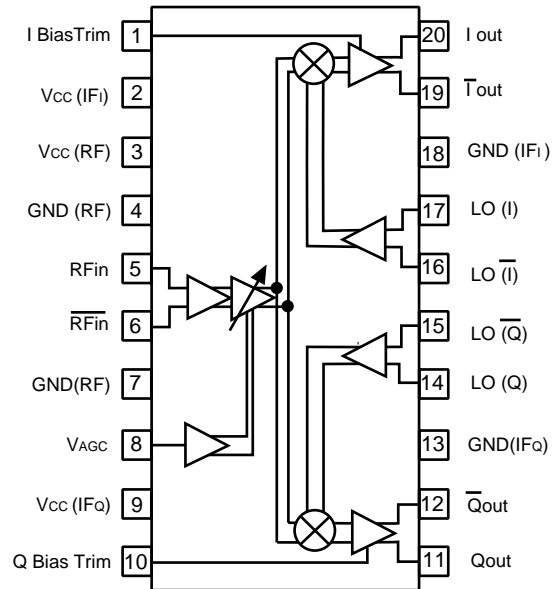
- **BROADBAND OPERATION**
RF & LO DC to 1 GHz
IF (IQ) DC to 100 MHz
- **WIDEBAND IQ PHASE AND AMPLITUDE MATCHING**
Amplitude Matching: ± 0.3 dB Typical
Phase Matching: $\pm 0.3^\circ$ (driven in phase)
- **AGC DYNAMIC RANGE:**
30 dB Typical
- **LOW DISTORTION:**
30 dBc Typical
- **SMALL SSOP 20 PACKAGE**
- **TAPE AND REEL PACKAGING AVAILABLE**

DESCRIPTION

The UPC2766GR Silicon MMIC Wideband IQ Demodulator was manufactured with the NESAT III MMIC process. The NESAT III process produces transistors with f_T approaching 20 GHz. The device was designed specifically for digital video and data receivers. The IC consists of a wide band RF amplifier, Gain Control amplifier, dual balanced mixers, LO buffers, and I & Q output buffer amplifiers.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS¹ ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $Z_L = 50\ \Omega$)

PART NUMBER PACKAGE OUTLINE			UPC2766GR S20 (SSOP 20)		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I _{CC}	Circuit Current (no signal)	mA		60	78
f _{RF}	RF Input Bandwidth ² f _{IF} = 40 MHz, f _{RF} > f _{LO} , 3 dB down	MHz	DC-750	DC-1000	
f _{IF}	IF Output Bandwidth ³ f _{RF} = 480 MHz, f _{RF} > f _{LO} , 3 dB down, V _{AGC} = 0 V	MHz		200	
CG	Conversion Gain	dB	15	20	25
NF	Noise Figure	dB		21	
IM3	3rd Order Intermodulation Distortion f _{RF1} = 480 MHz, f _{RF2} = 490 MHz, f _{LO} = 440 MHz, P _{IN} = -20 dBm, V _{AGC} = 1 V	dBc		30	
$\Delta\Phi$	IQ Phase Balance (LO driven in phase)	deg		± 0.3	± 1.5
ΔG	IQ Amplitude Balance	dB		± 0.3	± 0.5
G _{AGC}	AGC Range, V _{AGC} = 0-5 V	dB	40	45	
LO-RF	LO to RF Isolation	dB		55	
LO-IF	LO to IF Isolation	dB		10	
P _{SAT}	Saturated Output Level	dBm		+2	
V _O	Saturated Output Voltage (Z _L = 250 Ω /2pF)	V _{P-P}	1.2	1.5	

Notes:

1. f_{RF} = 480 MHz, f_{IF} = 40 MHz, P_{LO} = -10 dBm, P_{RF} = -30 dBm, V_{AGC} = 0 V, f_{RF} > f_{LO} unless otherwise specified.
2. RF Bandwidth defined as 3 dB down from response at f_{RF} = 40 MHz.
3. IF Bandwidth defined as 3 dB down from response at f_{IF} = 10 MHz.

ABSOLUTE MAXIMUM RATINGS¹ (TA = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
Vcc	Supply Voltage	V	6
P _D	Power Dissipation ²	mW	430
T _{OP}	Operating Temperature Range	°C	-40 to +85
T _{STG}	Storage Temperature	°C	-55 to +150

Notes:

1. Operation in excess of any one of these parameters may result in permanent damage.
2. Mounted on a 50x50x1.6 mm epoxy glass PWB (TA = 85°C).

RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
Vcc	Supply Voltage	V	4.5	5.0	5.5
T _{OP}	Operating Temperature	°C	-40	+25	+85

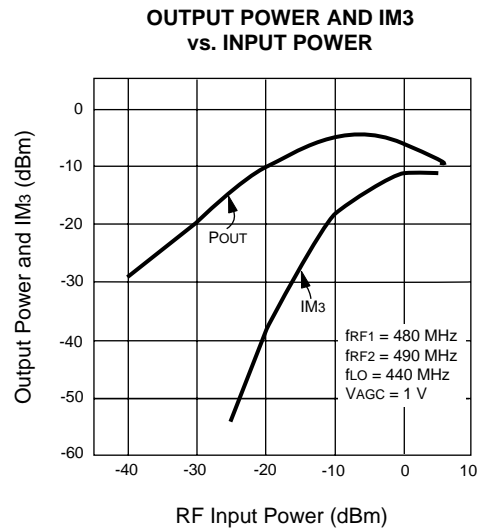
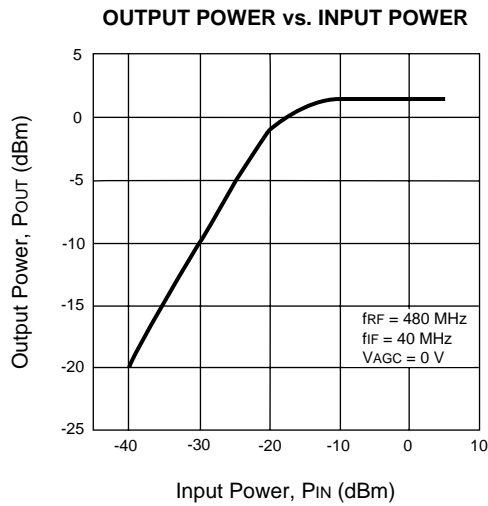
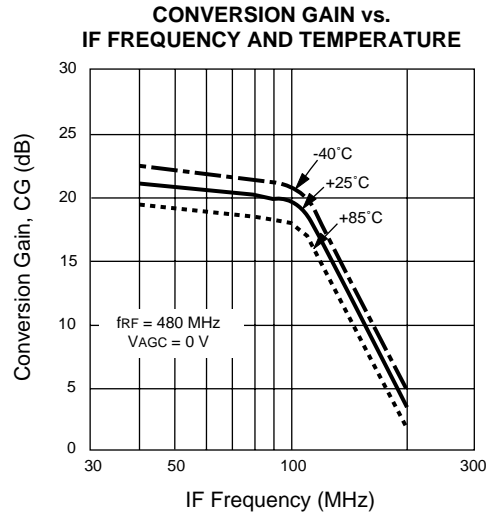
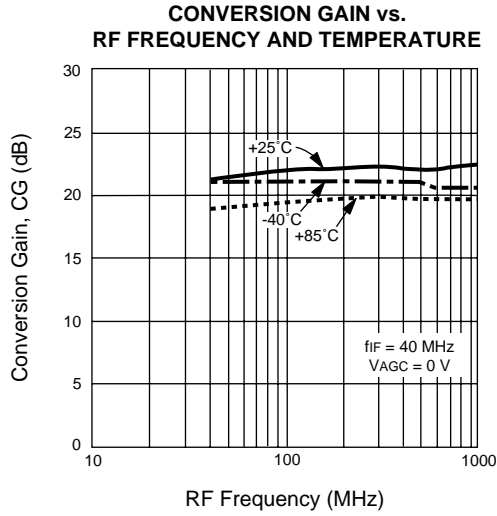
PIN FUNCTIONS

Pin No.	Pin Name	Pin Voltage Typ. (V)	Function and Explanation	Equivalent Circuit
1	I Trim	4.2	Limiter control for I-IF output	
2	Vcc (IFi)	5.0	Power supply pin of I-Mixer.	
3	Vcc (RF)	5.0	Power supply pin of RF and AGC block.	
4	GND (RF)	0.0	Ground pin of RF and AGC block.	
5	RFin	2.6	RF input pin. For single-ended applications, Pin 6 should be bypassed to GND via a capacitor.	
6	RFin	2.6		
7	GND (RF)	0.0	Ground pin of RF and AGC block.	
8	VAGC	0-5	Gain control pin. • VAGC = 0 V: Maximum Gain • VAGC = 5 V: Maximum Attenuation	
9	Vcc (IFq)	5.0	Power supply pin of Q-Mixer	
10	Q Trim	4.2	Limiter control for Q-IF output.	

PIN FUNCTIONS

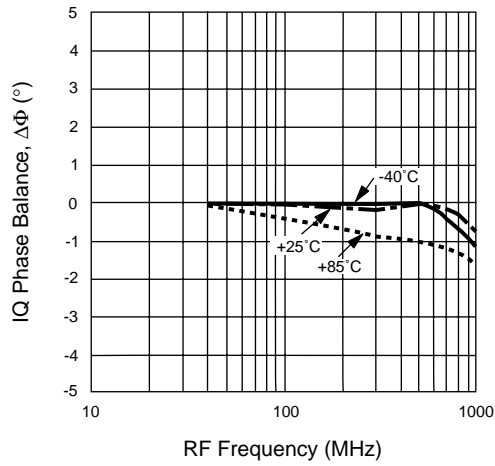
Pin No.	Pin Name	Pin Voltage Typ. (V)	Function and Explanation	Equivalent Circuit
11	Qout	3.3	Q-IF output pin. Output impedance is approximately 55 Ω. Output load should be approximately 250 Ω. Pin 11 and pin 12 are differential outputs. For single-ended applications, terminate unused output with equivalent impedance.	
12	$\overline{\text{Qout}}$	3.3		
13	GND (IF _Q)	0.0	Ground pin of Q-IF block.	
14	LO (α)	2.2	Oscillator input of Q-Mixer. For single-ended applications, pin 15 should be bypassed to GND via a capacitor.	
15	LO ($\overline{\alpha}$)	2.2		
16	LO (\overline{i})	2.2	Oscillator input of I-Mixer. For single-ended applications, pin 16 should be bypassed to GND via a capacitor.	
17	LO (i)	2.2		
18	GND (IF _I)	0.0	Ground pin of I-IF block.	
19	$\overline{\text{lout}}$	3.3	I-IF output pin. Output impedance is approximately 55 Ω. Output load should be approximately 250 Ω. Pin 19 and pin 20 are differential outputs. For single-ended applications, terminate unused output with equivalent impedance.	
20	lout	3.3		

TYPICAL PERFORMANCE CURVES (TA = 25°C unless otherwise specified)

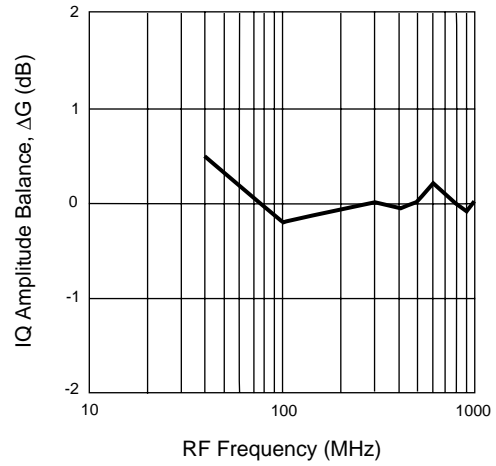


TYPICAL PERFORMANCE CURVES (TA = 25°C, fIF = 40 MHz, unless otherwise specified.)

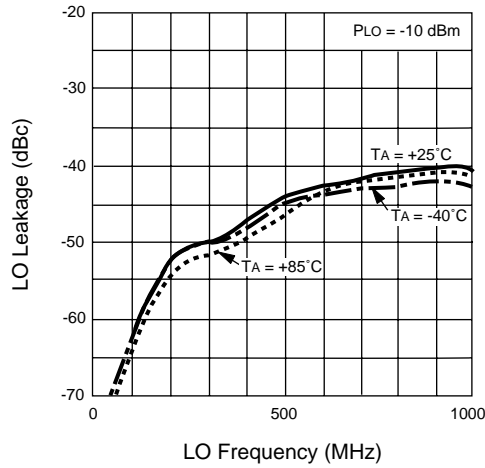
IQ PHASE BALANCE vs. RF FREQUENCY AND TEMPERATURE



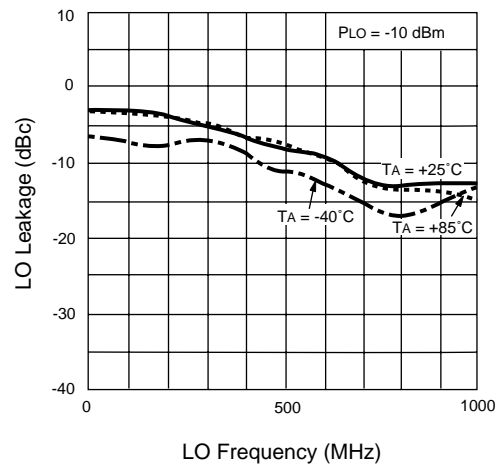
IQ AMPLITUDE BALANCE vs. RF FREQUENCY



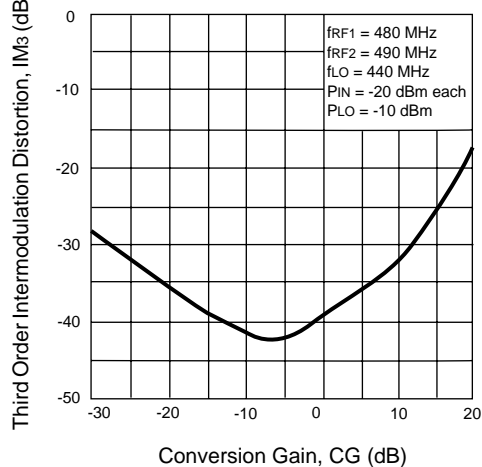
LO LEAKAGE TO RF PORT vs. LO FREQUENCY AND TEMPERATURE



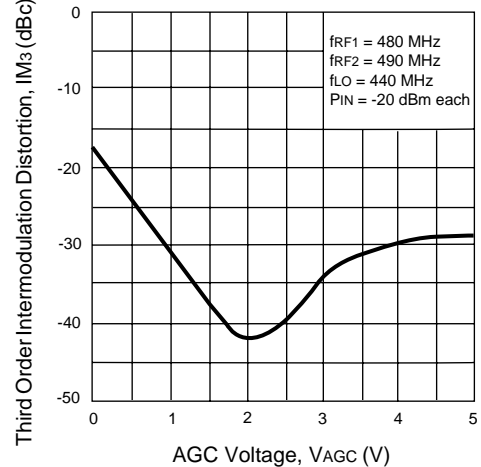
LO LEAKAGE TO IF PORT vs. LO FREQUENCY AND TEMPERATURE



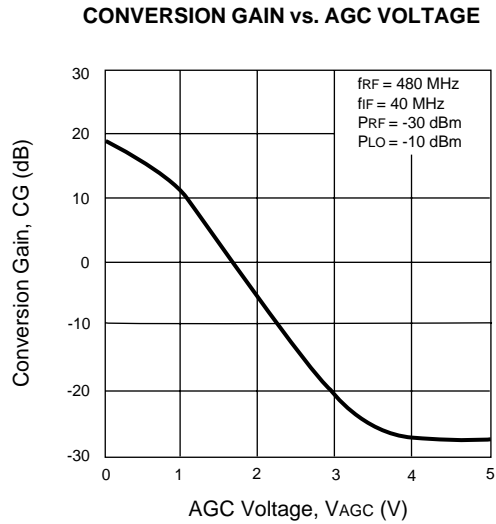
THIRD ORDER INTERMODULATION vs. CONVERSION GAIN



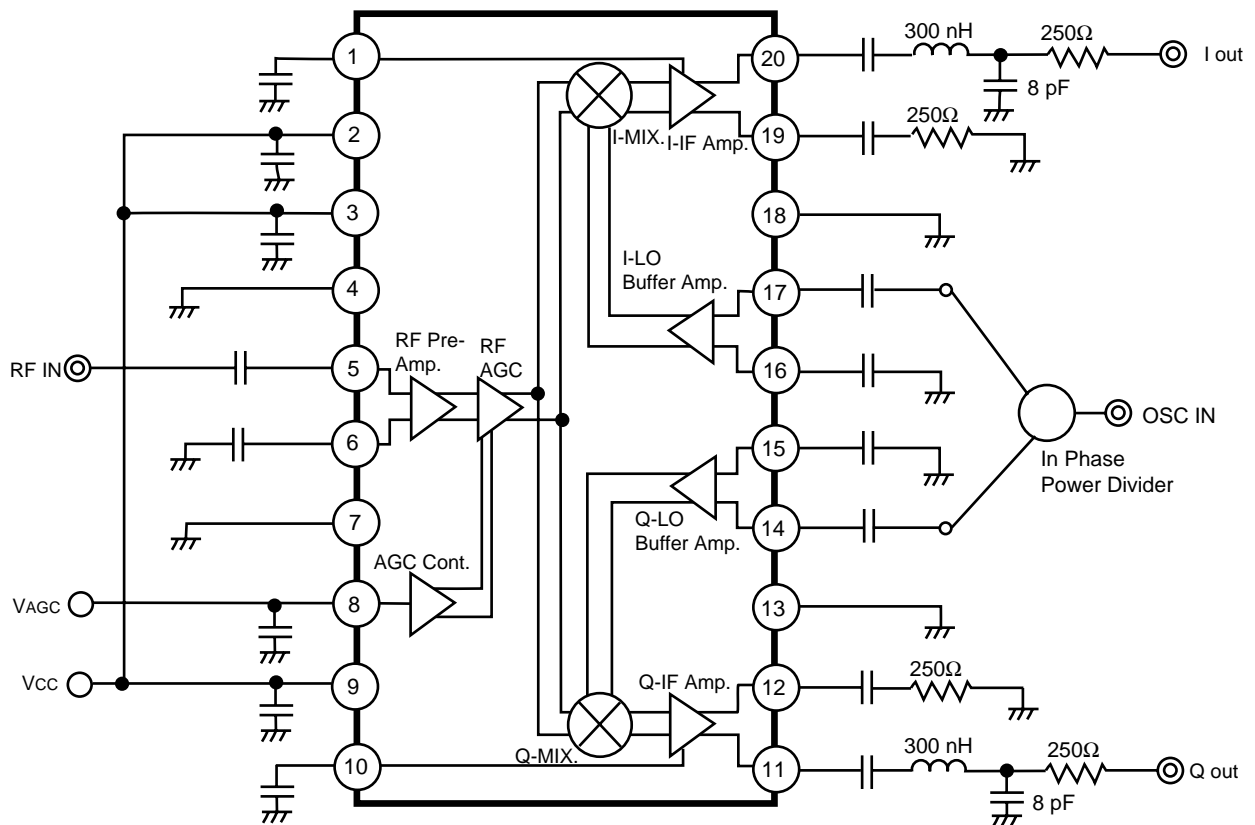
THIRD ORDER INTERMODULATION vs. AGC VOLTAGE



TYPICAL PERFORMANCE CURVES (TA = 25°C)

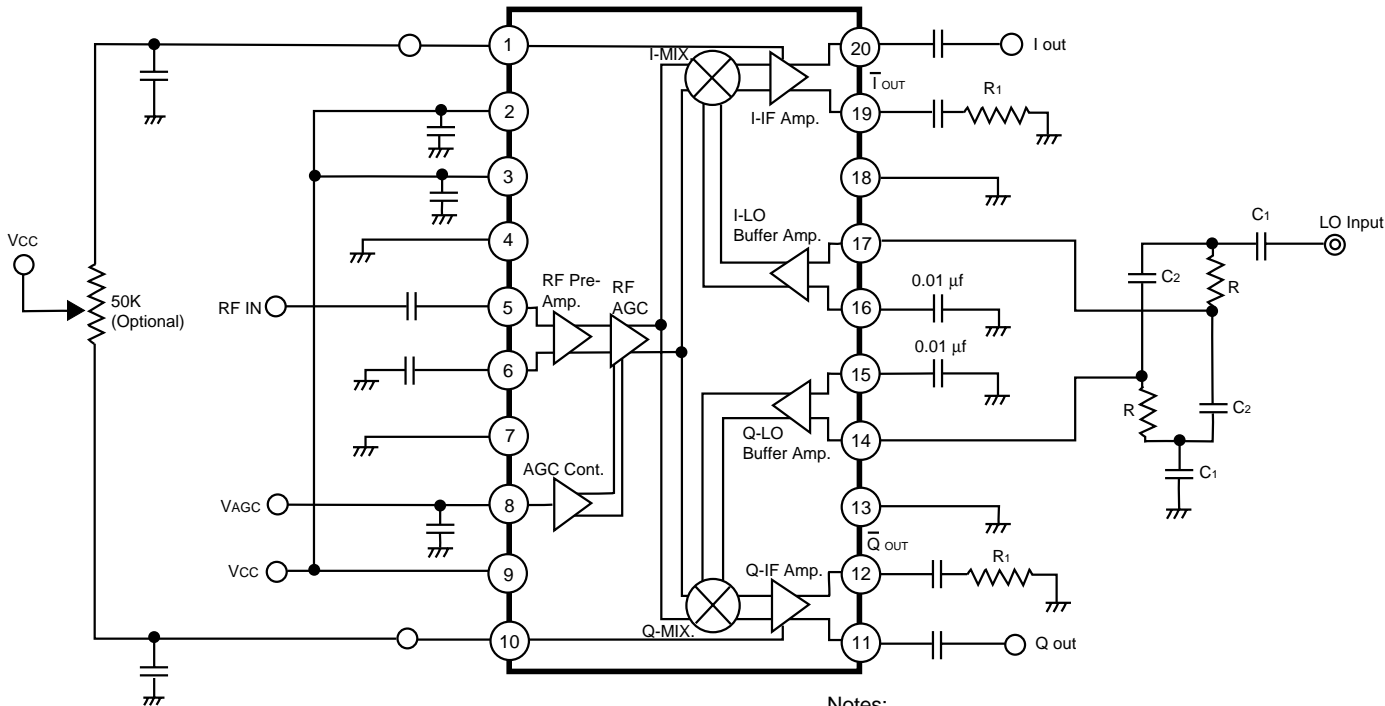


TEST CIRCUIT



- Notes:
1. All capacitors are 1000 pF unless otherwise noted.
 2. Low Pass Filter on I and QOUT minimizes LO Leakage.

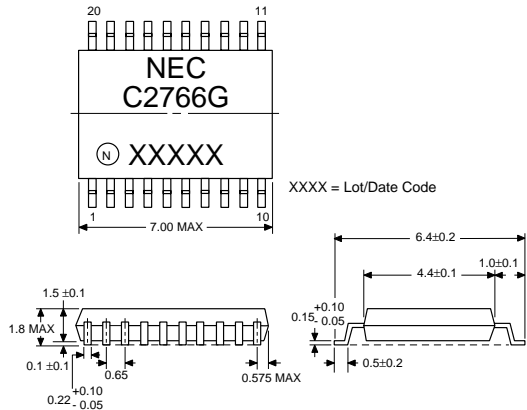
APPLICATION CIRCUIT



- Notes:
1. All capacitors are 1000 pF unless otherwise noted.
 2. Phase shifter element values
 $X_{C1} \ll R @ f_{LO}$
 $X_{C2} = R @ f_{LO}$
 3. Set R1 of IOUT and QOUT ports to match the load of IOUT and QOUT ports

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE SSOP 20

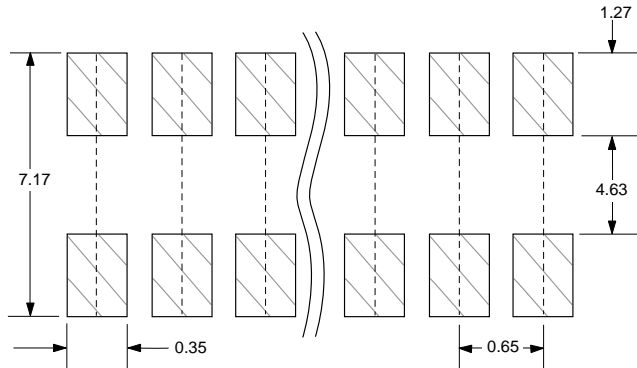


Lead Material: Alloy 42
 Lead Plating: Lead Tin Alloy

LEAD CONNECTIONS

- | | |
|-----------------|---------------|
| 1. I BIAS TRIM | 11. Q OUT |
| 2. Vcc (IFi) | 12. Q OUT |
| 3. Vcc (RF) | 13. GND (IFq) |
| 4. GND (RF) | 14. LOq |
| 5. RF IN | 15. LOq |
| 6. RF IN | 16. LOi |
| 7. GND (RF) | 17. LOi |
| 8. VAGC | 18. GND (IFi) |
| 9. Vcc (IFq) | 19. I OUT |
| 10. Q BIAS TRIM | 20. I OUT |

RECOMMENDED PCB LAYOUT (Units in mm)



ORDERING INFORMATION

PART NUMBER	QUANTITY
UPC2766GR-E1	2500/Reel

Note:
 Embossed Tape, 12 mm wide.

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11/14/2000