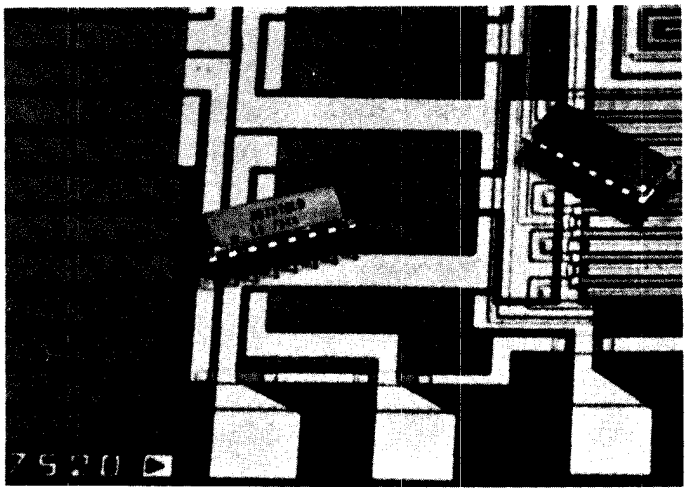
CMOS 10&12-Bit Monolithic Multiplying D/A Converters

AD7520, AD7521

FEATURES

- AD7520: 10 Bit Resolution
- AD7521: 12 Bit Resolution
- Linearity: 8, 9 and 10 Bit
- Nonlinearity Tempco: 2ppm of FSR/°C
- Low Power Dissipation: 20mW
- Current Settling Time: 500ns
- Feedthrough Error: 1/2LSB @ 100kHz
- TTL/DTL/CMOS Compatible



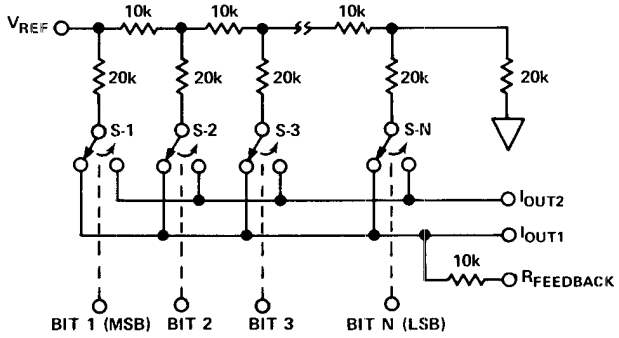
GENERAL DESCRIPTION

The AD7520 (AD7521) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The devices use advanced CMOS and thin film technologies providing up to 10-bit accuracy with TTL/DTL/CMOS compatibility.

The AD7520 (AD7521) operates from +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical AD7520 (AD7521) applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

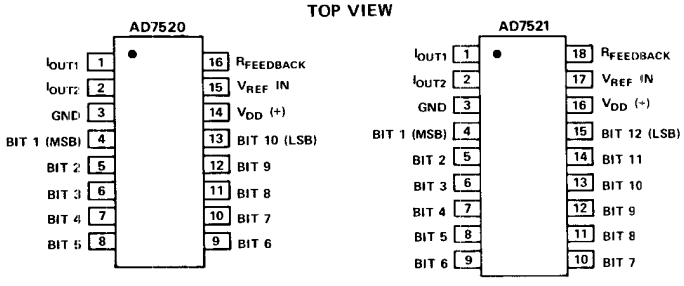
AD7520: N=10
AD7521: N=12
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7521JN	AD7520JD AD7521JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7521KN	AD7520KD AD7521KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7521LN	AD7520LD AD7521LD	AD7520UD AD7521UD

PIN CONFIGURATION

TOP VIEW



PACKAGE IDENTIFICATION

Suffix D: Ceramic DIP package
Suffix N: Plastic DIP package

SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER		AD7520	AD7521	TEST CONDITIONS
DC ACCURACY[1]				
Resolution		10 Bits	12 Bits	
Nonlinearity (See Figure 5)				
		J, 0.2% of FSR max (8 Bit)	*	S,T,U: over -55°C to +125°C
		S, 0.2% of FSR max (8 Bit)	*	$-10V \leq V_{REF} \leq +10V$
		K, 0.1% of FSR max (9 Bit)	*	
		T, 0.1% of FSR max (9 Bit)	*	
		L, 0.05% of FSR max (10 Bit)	*	
		U, 0.05% of FSR max (10 Bit)	*	
Nonlinearity Tempco		2ppm of FSR/°C max	*	$-10V \leq V_{REF} \leq +10V$
Gain Error[2]		0.3% of FSR typ	*	$-10V \leq V_{REF} \leq +10V$
Gain Error Tempco[2]		10ppm of FSR/°C max	*	$-10V \leq V_{REF} \leq +10V$
Output Leakage Current (either output)		200nA max	*	Over specified temperature range
Power Supply Rejection (See Figure 6)		50ppm of FSR%/°C typ	*	
AC ACCURACY				To 0.05% of FSR
Output Current Settling Time (See Figure 10)		500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error (See Figure 9)		10mV p-p max		V_{REF} = 20V p-p, 100kHz
			*	All digital inputs low
REFERENCE INPUT				
Input Resistance[4]		5kΩ min	*	
		10kΩ typ	*	
		20kΩ max	*	
ANALOG OUTPUT				
Output Capacitance (See Figure 8)	I_{OUT1}	120pF typ	*	All digital inputs high
	I_{OUT2}	37pF typ	*	All digital inputs high
	I_{OUT1}	37pF typ	*	All digital inputs low
	I_{OUT2}	120pF typ	*	All digital inputs low
Output Noise (both outputs) (See Figure 7)		Equivalent to 10kΩ typ Johnson noise	*	
DIGITAL INPUTS[3]				
Low State Threshold		0.8V max	*	Over specified temperature range
High State Threshold		2.4V min	*	Over specified temperature range
Input Current (low to high state)		1μA typ	*	Over specified temperature range
Input Coding		Binary	*	See Tables 1 & 2 under Applications
POWER REQUIREMENTS				
Power Supply Voltage Range		+5V to +15V	*	
I_{DD}		5nA typ	*	All digital inputs at GND
		2mA max	*	All digital inputs high or low
Total Dissipation (Including ladder)		20mW typ	*	

NOTES:
[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
[2] Using the internal $R_{FEEDBACK}$.
[3] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
[4] Ladder and feedback resistor tempco is approximately -150ppm/°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{REF} (to GND) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Output Voltage (Pin 1, Pin 2) . . . . . -100mV to V_{DD}
Power Dissipation (package)
up to +75°C 450mW
derates above +75°C by . . . . . 6mW/°C
Operating Temperature
JN, KN, LN Versions . . . . . 0 to +70°C
JD, KD, LD Versions . . . . . -25°C to +85°C
SD, TD, UD Versions . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V unless otherwise noted

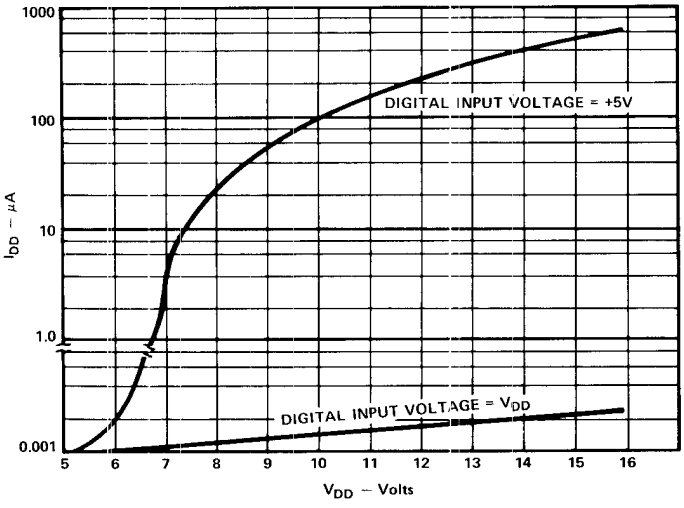


Figure 1. Supply Current vs. Supply Voltage

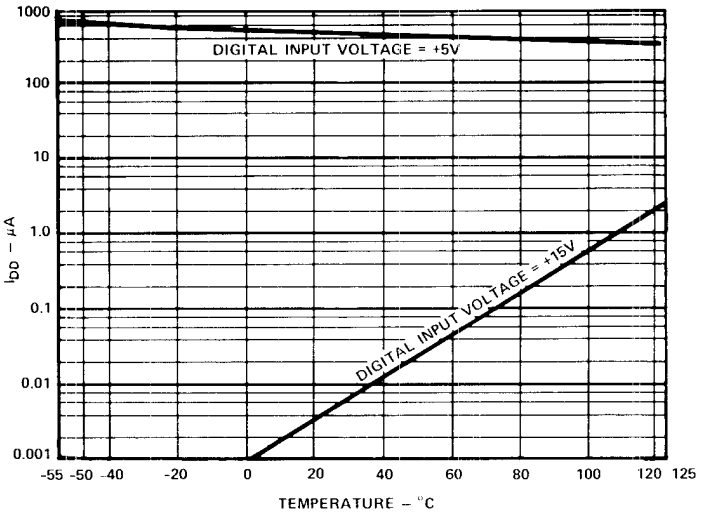


Figure 2. Supply Current vs. Temperature

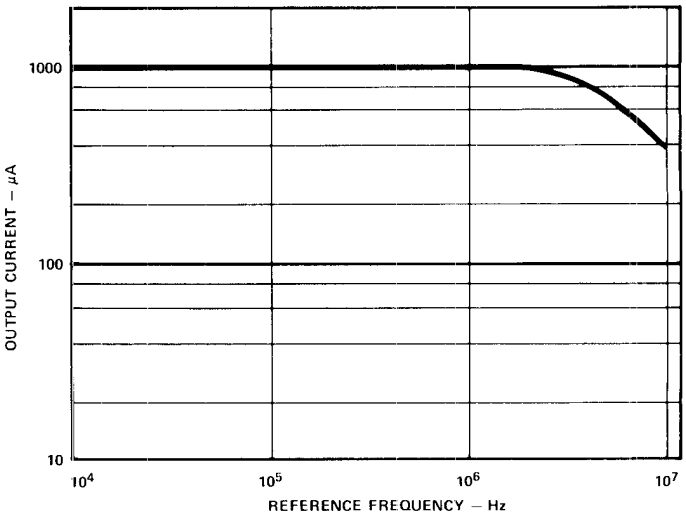


Figure 3. Output Current Bandwidth

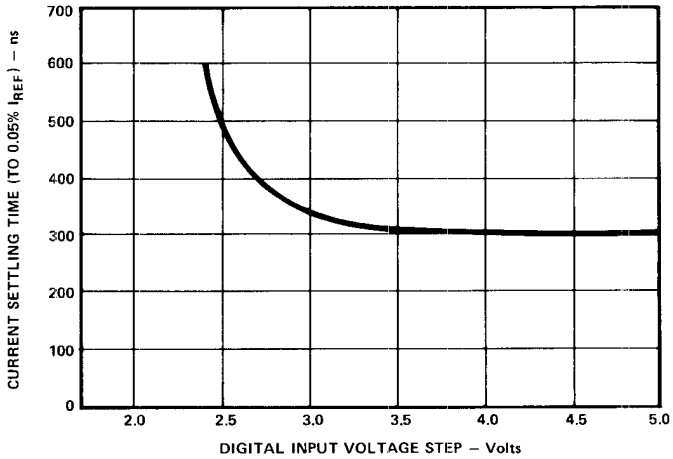


Figure 4. Output Current Settling Time vs. Digital Input Voltage

TEST CIRCUITS

Note: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7521.

DC PARAMETERS

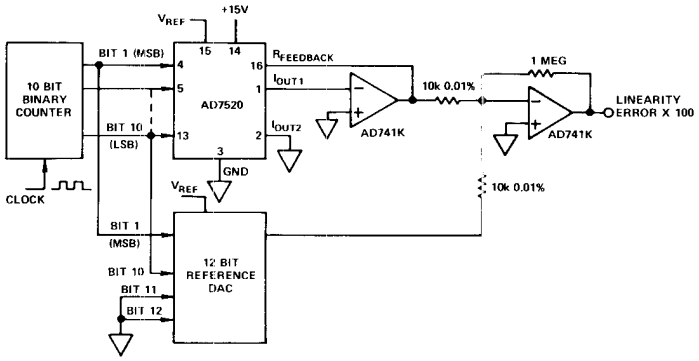


Figure 5. Nonlinearity

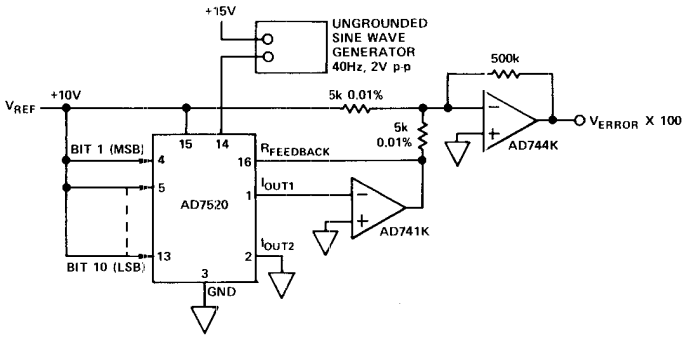


Figure 6. Power Supply Rejection

AC PARAMETERS

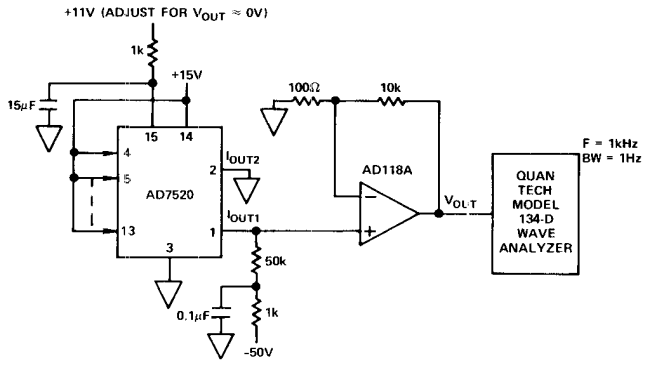


Figure 7. Noise

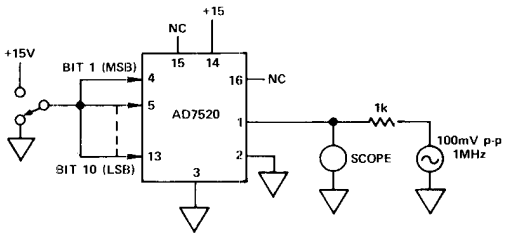


Figure 8. Output Capacitance

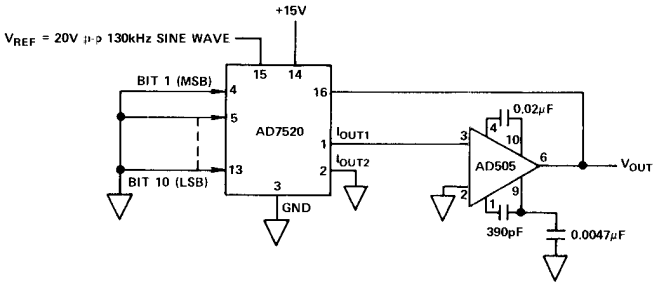


Figure 9. Feedthrough Error

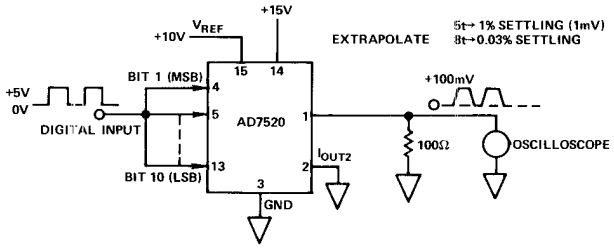


Figure 10. Output Current Settling Time

TERMINOLOGY

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

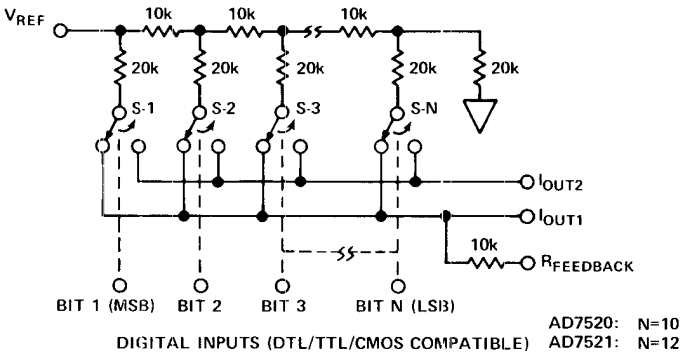
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7521), a 10-bit (12-bit) multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten (twelve) CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 11. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.



(Switches shown for Inputs "High")

Figure 11. AD7520 (AD7521) Functional Diagram

One of the CMOS current switches is shown in Figure 12. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the first six switches are binarily scaled so the voltage drop across each switch is the same. For example, switch-1 of Figure 12 was designed for an "ON" resistance of 20 ohms, switch-2 of 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

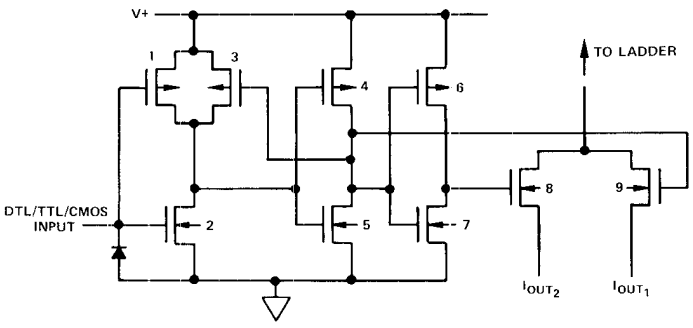


Figure 12. CMOS Switch

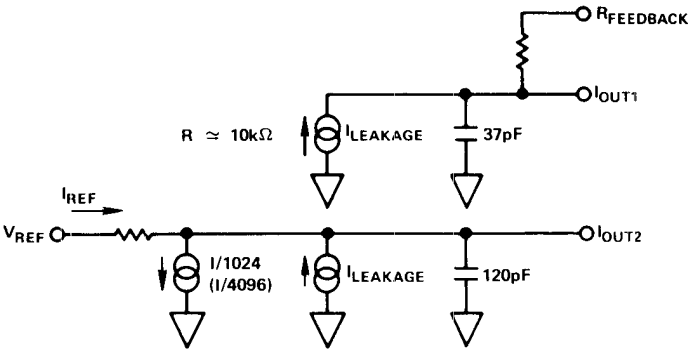


Figure 13. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 13 and 14. In Figure 13 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}\left(\frac{I}{4096}\right)$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 120pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 37pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 14 is similar to Figure 13; however, the "ON" switches are now on terminal I_{OUT1}, hence the 120pF at that terminal.

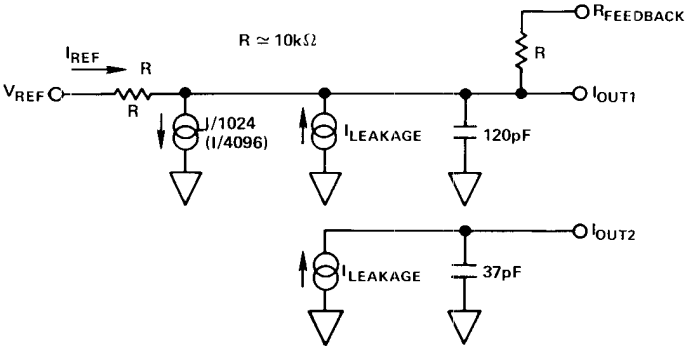


Figure 14. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs High

APPLICATIONS

UNIPOLAR BINARY OPERATION

Figure 15 shows the circuit connections required for unipolar operation using the AD7520. Since V_{REF} can assume either positive or negative values, the circuit is also capable of 2-quadrant multiplication. The input code/output range table for unipolar binary operation is shown in Table 1.

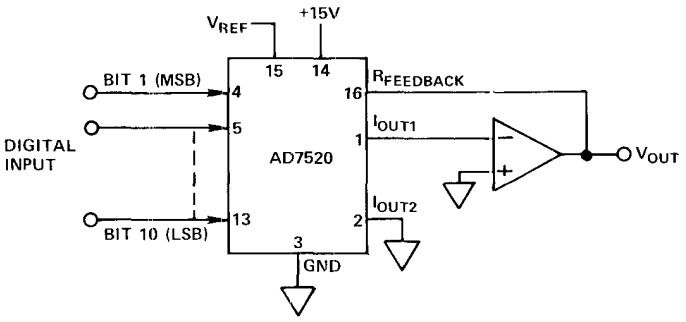


Figure 15. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Tie all digital inputs to the AD7520 (AD7521) to GND potential.
2. Adjust the offset trimpot on the output operational amplifier for 0V ±1mV at V_{OUT}.

Gain Adjustment

1. Tie all digital inputs to the AD7520 (AD7521) to the +15V supply.
2. To increase V_{OUT}, place a resistor R in series with the amplifier output terminal and $R_{FEEDBACK}$ of the AD7520 (AD7521) (R = 0 to 500Ω)
3. To decrease V_{OUT}, place a resistor R in series with V_{REF}. (R = 0 to 500Ω)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table 1. Code Table — Unipolar Binary Operation

BIPOLAR (OFFSET BINARY) OPERATION

Figure 16 illustrates the AD7520 connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. Input coding is offset binary (modified 2's complement) as shown in Table 2.

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

Table 2. Code Table — Bipolar (Offset Binary) Operation

When a switch's control input is a Logical "1", that switch's current is steered to I_{OUT1}, forcing the output of amplifier #1 to

$$V_{OUT} = -(I_{OUT1})(10k)$$

where 10k is the value of the feedback resistor.

A Logical "0" on the control input steers the switch's current to I_{OUT2}, which is terminated into the summing junction of amplifier #2. Resistors R1 and R2 need not track the internal R-2R circuitry; however, they should closely match each other to insure that the voltage at amplifer #2's output will force a current into R2 which is equal in magnitude but opposite in polarity to the current at I_{OUT2}. This creates a push-pull effect which halves the resolution but doubles the output range for changes in the digital input.

With the MSB a Logic "1" and all other bits a Logic "0", a 1/2 LSB difference current exists between I_{OUT1} and I_{OUT2}, creating an offset of 1/2 LSB. To shift the transfer curve to zero, resistor R-9 is used to sum 1/2 LSB of current into the I_{OUT2} terminal.

Offset Adjustment

1. Make V_{REF} approximately +10V.
2. Tie all digital inputs to +15V (Logic "1").
3. Adjust amplifier #2 offset trimpot for 0V ±1mV at amplifier #2 output.
4. Tie MSB (Bit 1) to +15V, all other bits to ground.
5. Adjust amplifier #1 offset trimpot for 0V ±1mV at V_{OUT}.

Gain Adjustment

Gain adjustment is the same as for unipolar operation.

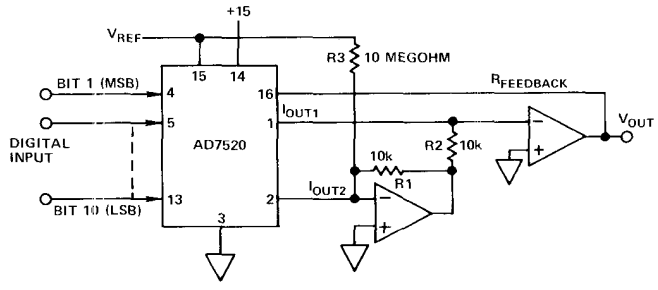


Figure 16. Bipolar Operation (4-Quadrant Multiplication)

DYNAMIC PERFORMANCE CHARACTERISTICS

The following circuits and associated waveforms illustrate the dynamic performance which can be expected using some commonly available IC amplifiers. All settling times are to 0.05% of 10V.

AD741J

Small Signal Bandwidth: 180kHz
Settling Time: 20μs

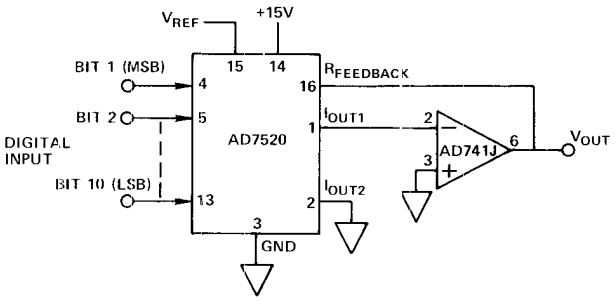


Figure 17. DAC Circuit Using AD741J

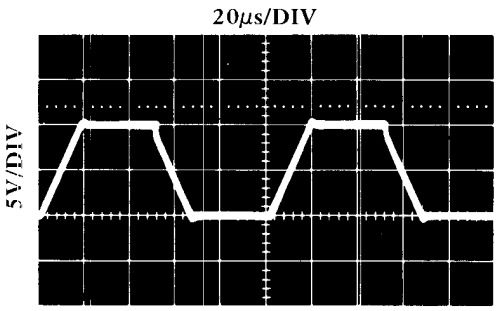


Figure 18. Output Waveform

AD518K

Small Signal Bandwidth: 1.0MHz
Settling Time: 6.0μs

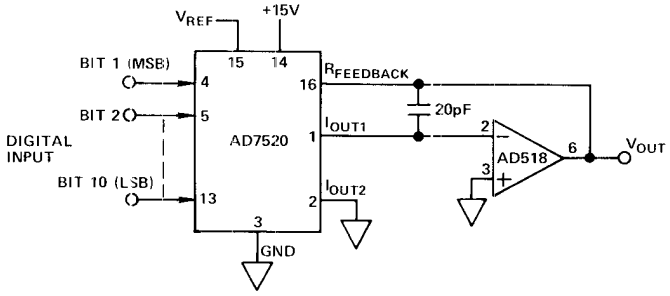


Figure 19. DAC Circuit Using AD518K

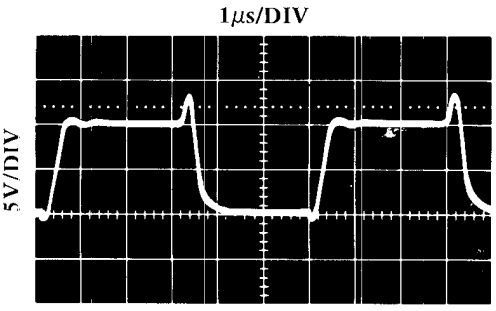


Figure 20. Output Waveform

AD505J

Small Signal Bandwidth: 1.0MHz
Settling Time: 2.5μs

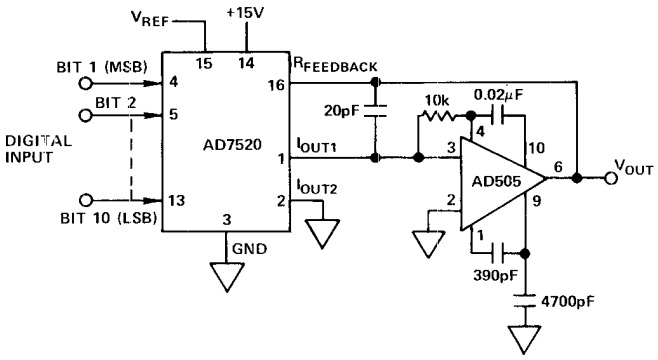


Figure 21. DAC Circuit Using AD505J

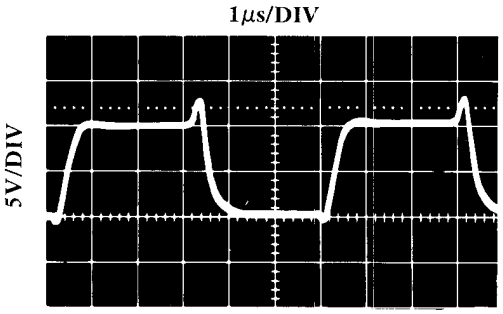


Figure 22. Output Waveform

AD509K

Small Signal Bandwidth: 1.6MHz
Settling Time: 2.0μs

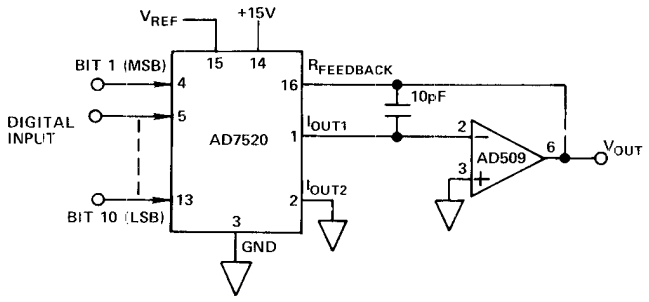


Figure 23. DAC Circuit Using AD509K

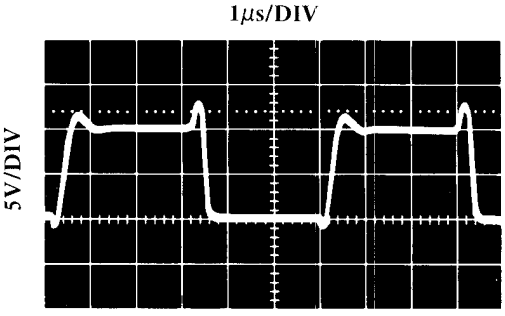


Figure 24. Output Waveform

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 25, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit 10) ON, the gain is 1024. With all bits ON, the gain is 1 (±1 LSB).

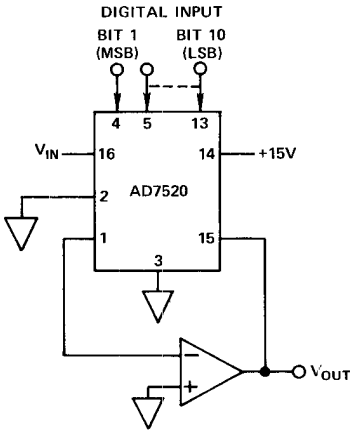
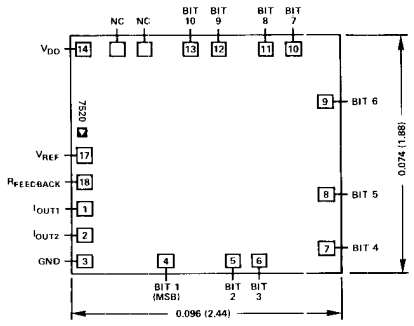


Figure 25. Analog/Digital Divider

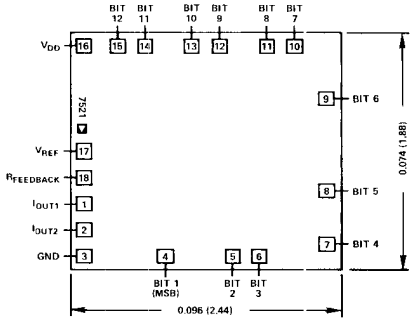
BONDING DIAGRAMS

Dimensions shown in inches and (mm).

AD7520



AD7521

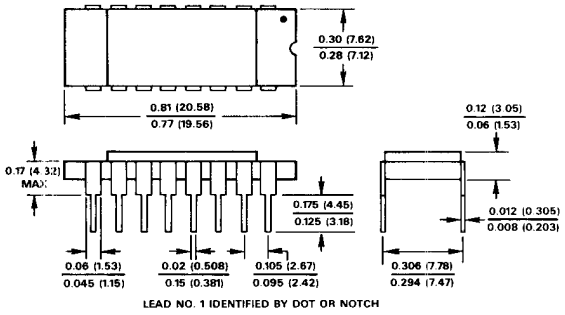


OUTLINE DIMENSIONS

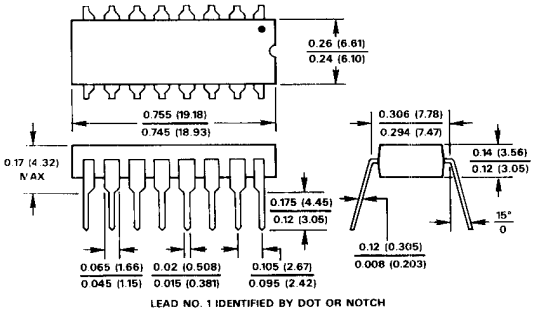
Dimensions shown in inches and (mm).

AD7520

16 PIN CERAMIC DIP

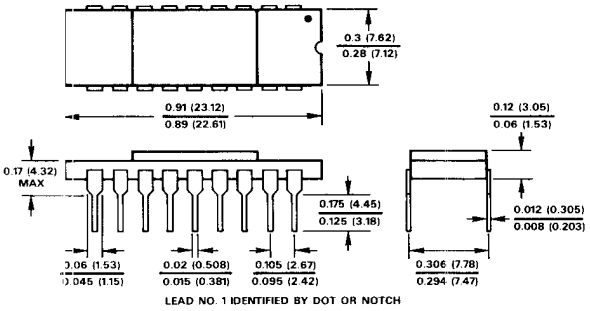


16 PIN PLASTIC DIP



AD7521

18 PIN CERAMIC DIP



18 PIN PLASTIC DIP