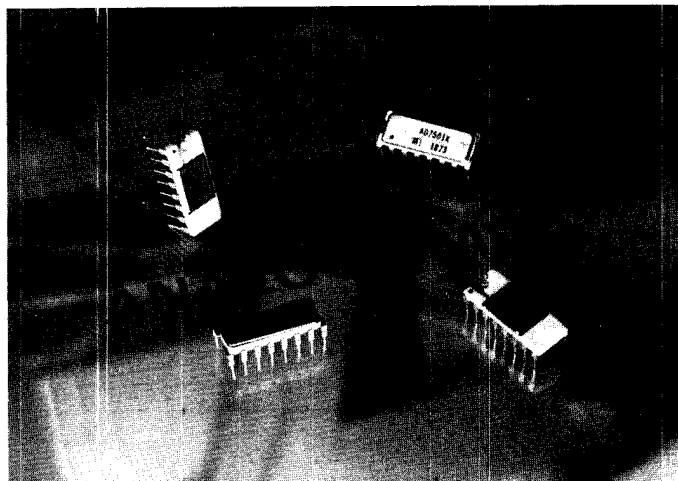


FEATURES

- DTL/TTL/CMOS Direct Interface
- Power Dissipation: 30 μ W
- R_{ON}: 170 Ω
- Output "Enable" Control
- AD7503 Replaces HI-1818



GENERAL DESCRIPTION

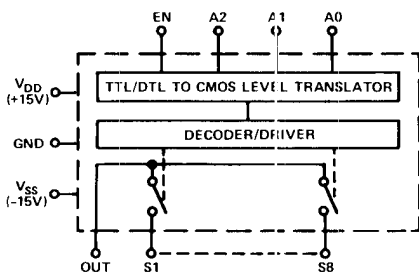
The AD7501 and AD7503 are monolithic CMOS, 8 channel analog multiplexers which switches one of 8 inputs to a common output depending on the state of three binary address lines and an "enable" input. The AD7503 is identical to the AD7501 except its "enable" logic is inverted. All digital inputs are TTL/DTL and CMOS logic compatible.

The AD7502 is a monolithic CMOS dual 4-channel analog multiplexer. Depending on the state of 2 binary address inputs and an "enable", it switches two output busses to two of 8 inputs.

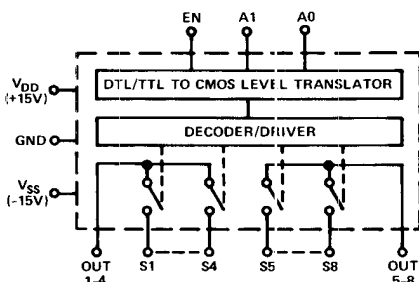
The AD7502 is an excellent example of a high breakdown CMOS process combined with a double layer interconnect for high density. Silicon nitride passivation ensures long term stability and reliability.

FUNCTIONAL DIAGRAMS

AD7501, AD7503



AD7502



ABSOLUTE MAXIMUM RATINGS

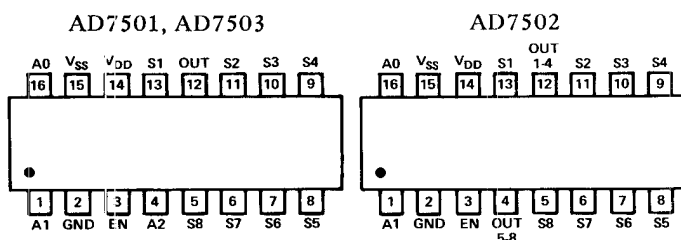
(T_A = +25°C unless otherwise noted)

| | |
|--|------------------------|
| V _{DD} - GND | +17V |
| V _{SS} - GND | -17V |
| V Between Any Switch Terminals | .25V |
| Switch Current (I _S , Continuous) | 35mA |
| Switch Current (I _S , Surge) | |
| 1ms duration, 10% duty cycle | 50mA |
| Digital Input Voltage Range | V _{DD} to GND |
| Power Dissipation (package) | |
| 16 pin Ceramic DIP | |
| Up to +75°C | 450mW |
| Derates above +75°C by | 6mW/°C |
| 16 pin Plastic DIP | |
| Up to +70°C | 670mW |
| Derates above +70°C by | 8.3mW/°C |
| Operating Temperature | |
| Plastic | 0 to +75°C |
| Ceramic (J, K versions) | -25°C to +85°C |
| Ceramic (S version) | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |

CAUTION:

1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

PIN CONFIGURATIONS (Top View)



SPECIFICATIONS

($V_{DD} = +15V$, $V_{SS} = -15V$ unless otherwise noted)

| PARAMETER | VERSION ¹ | SWITCH CONDITION | @25°C | | OVER SPECIFIED TEMP. RANGE | | TEST CONDITIONS |
|--|----------------------|------------------|------------------------|--------------------|----------------------------|-----------|---|
| | | | AD7501, AD7503 | AD7502 | AD7501, AD7503 | AD7502 | |
| ANALOG SWITCH | | | | | | | |
| R_{ON} | All | ON | 170Ω typ, 300Ω max | * | | | $-10V \leq V_S \leq +10V$ $I_S = 1.0mA$ |
| R_{ON} vs. V_S | All | ON | 20% typ | * | | | |
| R_{ON} vs. Temperature | All | ON | 0.5%/°C typ | * | | | $V_S = 0V$, $I_S = 1.0mA$ |
| ΔR_{ON} Between Switches | All | ON | 4% typ | * | | | |
| R_{ON} vs. Temperature Between Switches | All | ON | $\pm 0.01\%/^{\circ}C$ | * | | | |
| I_S | J, K | OFF | 0.2nA typ, 2nA max | * | 50nA max | * | $V_S = -10V$, $V_{OUT} = +10V$ and $V_S = +10V$, $V_{OUT} = -10V$ |
| | S | OFF | 0.5nA max | * | 50nA max | * | |
| I_{OUT} | J, K | OFF | 1nA typ, 10nA max | 0.6nA typ, 5nA max | 250nA max | 125nA max | $V_S = -10V$, $V_{OUT} = +10V$ and $V_S = +10V$, $V_{OUT} = -10V$ AD7501: Enable HIGH AD7502, 03: Enable LOW |
| | S | OFF | 5nA max | 3nA max | 250nA max | 125nA max | |
| $ I_{OUT} - I_S $ | J, K | ON | 12nA max | 7nA max | 300nA max | 175nA max | $V_S = 0$ |
| | S | ON | 5.5nA max | 3.5nA max | 300nA max | 175nA max | |
| DIGITAL CONTROL | | | | | | | |
| V_{INL} | All | | | | 0.8V max | * | |
| V_{INH} | J | | | | 3.0V min | * | Note 2 |
| | K, S | | | | 2.4V min | * | |
| I_{INL} or I_{INH} | All | | 10nA typ | * | | | |
| C_{IN} | All | | 3pF typ | * | | | |
| DYNAMIC CHARACTERISTICS³ | | | | | | | |
| t_{ON} | All | | 0.8μs typ | * | | | $V_{IN} = 0$ to $+5.0V$ (See Test Circuit 2) |
| t_{OFF} | All | | 0.8μs typ | * | | | |
| C_S | All | OFF | 5pF typ | * | | | |
| C_{OUT} | All | OFF | 30pF typ | 15pF typ | | | |
| C_{SOUT} | All | OFF | 0.5pF typ | * | | | |
| C_{SS} Between Any Two Switches | All | OFF | 0.5pF typ | * | | | |
| POWER SUPPLY | | | | | | | |
| I_{DD} | J, K | | 1μA typ, 100μA max | * | | | All Digital Inputs Low |
| | J, K | | 1μA typ, 100μA max | * | | | |
| | S | | 500μA max | * | 500μA max | * | |
| | S | | 500μA max | * | 500μA max | * | |
| I_{SS} | J, K | | 200μA typ, 500μA max | * | | | All Digital Inputs High |
| | J, K | | 1μA typ, 100μA max | * | | | |
| | S | | 800μA max | * | 800μA max | * | |
| | S | | 800μA max | * | 800μA max | * | |

NOTES:

*Same specifications as AD7501 and AD7503.

¹JN, KN versions specified for 0 to +75°C; JD, KD versions for -25°C to +85°C; and SD versions for -55°C to +125°C.

²A pullup resistor, typically 1-2kΩ is required to make the AD7501J, AD7502J and AD7503J compatible with TTL/DTL levels. The maximum value is determined by the output leakage current of the driver gate when in the high state.

³AC parameters are sample tested to ensure conformance to specifications.

Specifications subject to change without notice.

TRUTH TABLES

| A ₂ | A ₁ | A ₀ | E _N | "ON" |
|----------------|----------------|----------------|----------------|------|
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 2 |
| 0 | 1 | 0 | 1 | 3 |
| 0 | 1 | 1 | 1 | 4 |
| 1 | 0 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 6 |
| 1 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 8 |
| X | X | X | 0 | None |

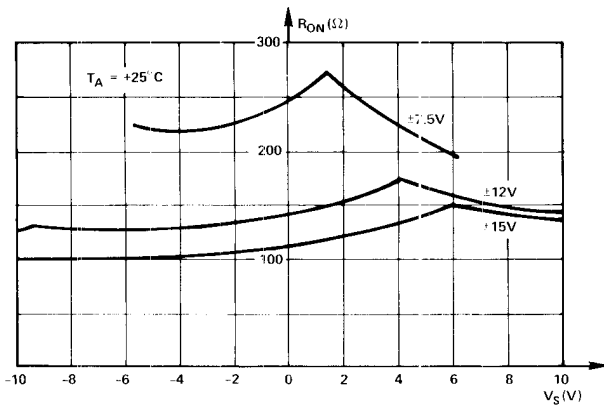
| A ₂ | A ₁ | A ₀ | E _N | "ON" |
|----------------|----------------|----------------|----------------|------|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 0 | 3 |
| 0 | 1 | 1 | 0 | 4 |
| 1 | 0 | 0 | 0 | 5 |
| 1 | 0 | 1 | 0 | 6 |
| 1 | 1 | 0 | 0 | 7 |
| 1 | 1 | 1 | 0 | 8 |
| X | X | X | 1 | None |

| A ₁ | A ₀ | E _N | "ON" |
|----------------|----------------|----------------|-------|
| 0 | 0 | 1 | 1 & 5 |
| 0 | 1 | 1 | 2 & 6 |
| 1 | 0 | 1 | 3 & 7 |
| 1 | 1 | 1 | 4 & 8 |
| X | X | 0 | None |

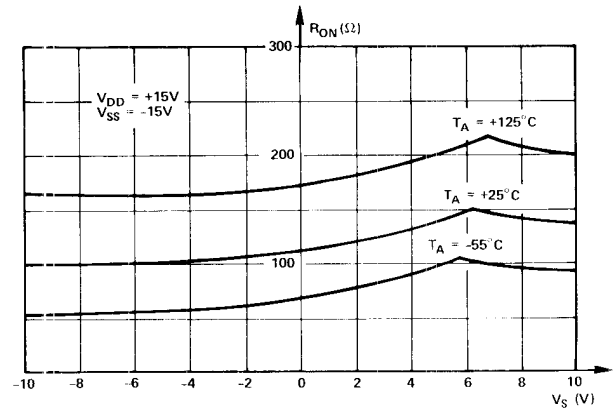
ORDERING INFORMATION

| Plastic (Suffix N) | Ceramic (Suffix D) | Operating Temperature Range |
|--|--|-----------------------------|
| AD7501JN AD7501KN AD7503JN AD7503KN | | 0 to +75°C |
| | AD7501JD AD7501KD AD7503JD AD7503KD | -25°C to +85°C |
| | AD7501SD AD7503SD | -55°C to +125°C |
| AD7502JN AD7502KN | | 0 to +75°C |
| | AD7502JD AD7502KD | -25°C to +85°C |
| | AD7502SD | -55°C to +125°C |

1. R_{ON} As A Function Of Switch Voltage (V_S)

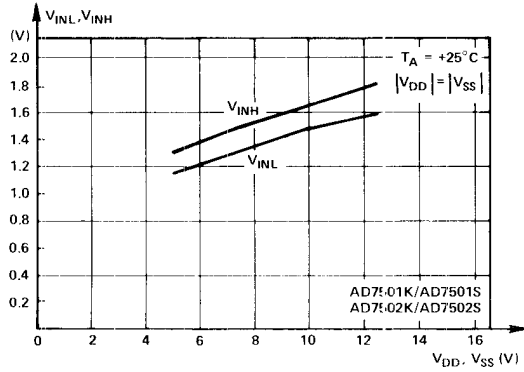


At Different Power Supplies

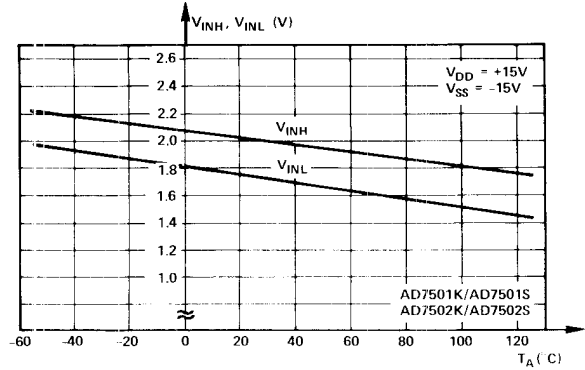


At Different Temperatures

2. Digital Threshold Voltage (V_{INH} , V_{INL})

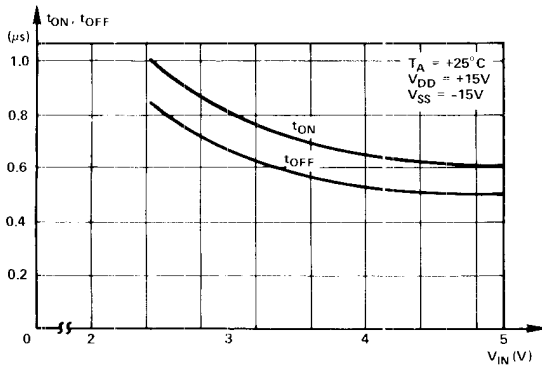


vs. Power Supply



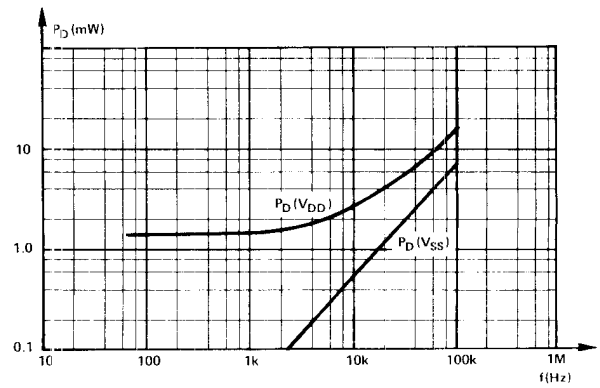
vs. Temperature

3. t_{ON} , t_{OFF}



vs. Digital Input Voltage

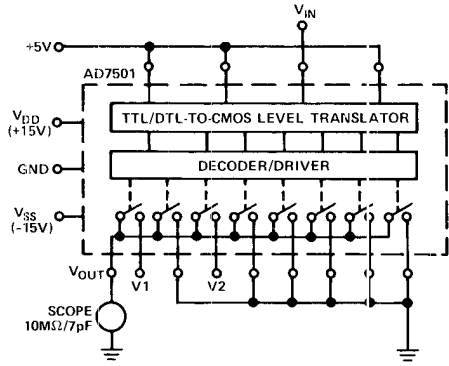
4. Power Dissipation



vs. Logic Frequency (50% Duty Cycle)

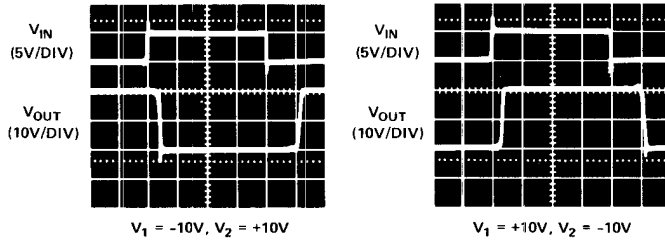
TYPICAL SWITCHING CHARACTERISTICS

TEST CIRCUIT 1

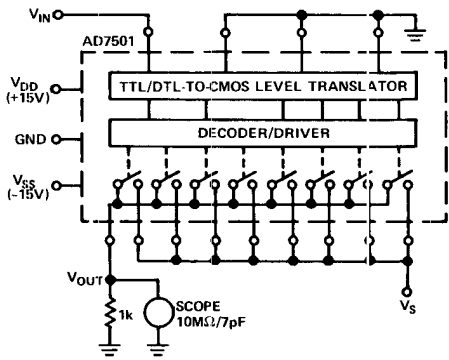


1μs/DIV

1μs/DIV

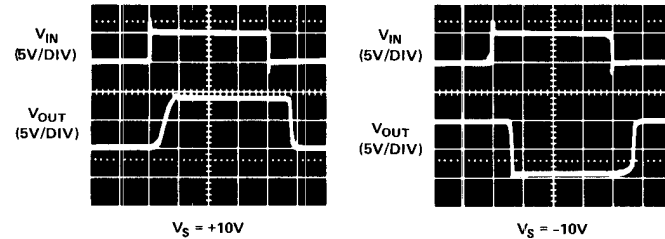


TEST CIRCUIT 2

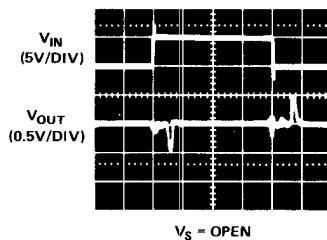


1μs/DIV

1μs/DIV



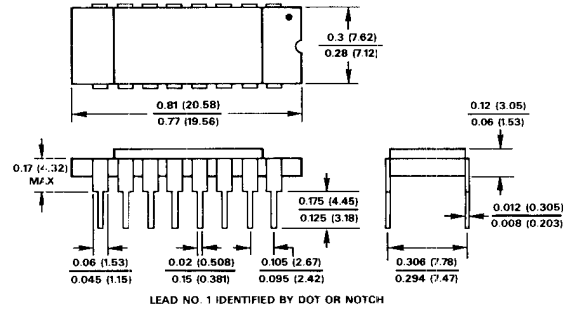
1μs/DIV



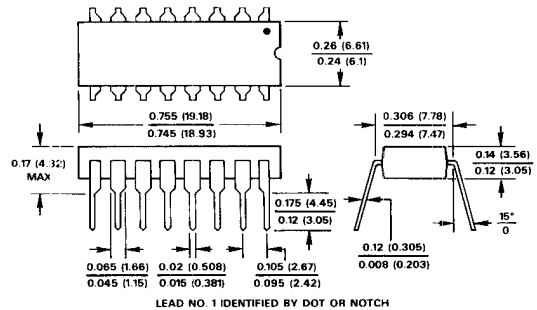
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-PIN CERAMIC DIP (SUFFIX D)

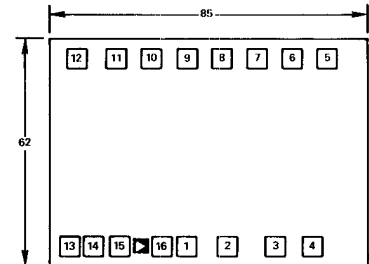


16-PIN PLASTIC DIP (SUFFIX N)

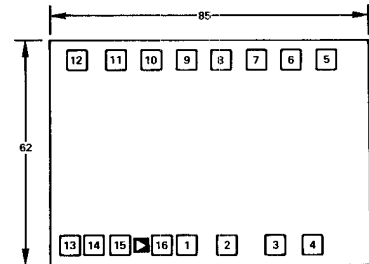


BONDING DIAGRAMS

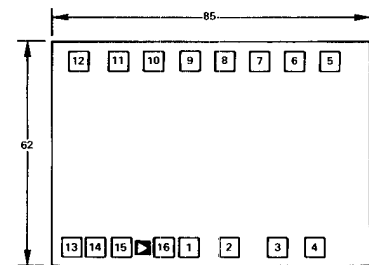
AD7501



AD7502



AD7503



All bonding pads are 4 x 4 MIL.
All pad numbers correspond with DIP package pin configuration.