

# BIPOLAR ANALOG INTEGRATED CIRCUIT

# $\mu$ PC1679G

### 5 V-BIAS, +15.5 dBm OUTPUT, 1.8 GHz WIDEBAND Si MMIC AMPLIFIER

#### DESCRIPTION

The  $\mu$ PC1679G is a silicon monolithic integrated circuit designed as medium output power amplifier for high frequency system applications. Due to +13 dBm TYP. output at 1 GHz, this IC is recommendable for transmitter stage amplifier of L Band wireless communication systems. This IC is packaged in 8-pin plastic SOP.

This IC is manufactured using NEC's 20 GHz fr NESAT™IV silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

#### FEATURES

- Supply voltage :  $V_{CC} = 4.5$  to  $5.5$  V
- Saturated output power :  $P_{O(sat)} = +15.5$  dBm TYP. @  $f = 500$  MHz with external inductor
- Wideband response :  $f_u = 1.8$  GHz TYP. @ 3 dB bandwidth
- Isolation : ISL = 34 dB TYP. @  $f = 500$  MHz
- Power Gain :  $G_P = 21.5$  dB TYP. @  $f = 500$  MHz

#### ORDERING INFORMATION

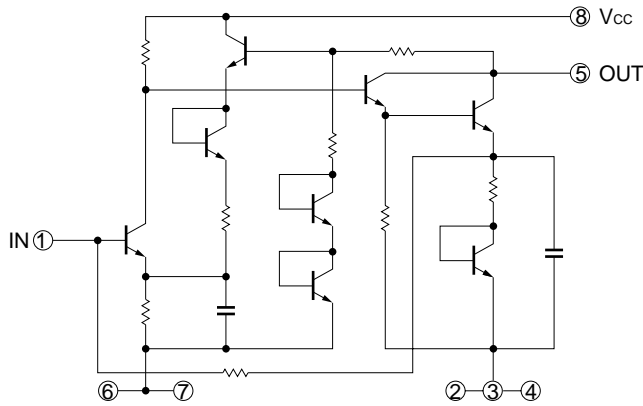
Part Number	Package	Marking	Supplying Form
$\mu$ PC1679G-E1	8-pin plastic SOP (225 mil)	1679	Embossed tape 12 mm wide. 1 pin is tape pull-out direction. Qty 2.5 kp/reel.
$\mu$ PC1679G-E2			Embossed tape 12 mm wide. 1 pin is tape roll-in direction. Qty 2.5 kp/reel.

**Remark** To order evaluation samples, please contact your local NEC sales office.  
(Part number for sample order:  $\mu$ PC1679G)

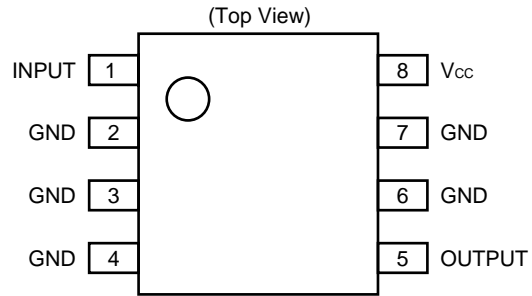
**Caution** Electro-static sensitive devices.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

EQUIVALENT CIRCUIT



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	$V_{CC}$	$T_A = +25\text{ }^\circ\text{C}$ , pin 5, pin 8	6	V
Input Power	$P_{in}$	$T_A = +25\text{ }^\circ\text{C}$	+10	dBm
★ Power Dissipation	$P_D$	Mounted on double copper clad $50 \times 50 \times 1.6\text{ mm}$ epoxy glass PWB ( $T_A = +85\text{ }^\circ\text{C}$ )	360	mW
Operating Ambient Temperature	$T_A$		-45 to +85	$^\circ\text{C}$
Storage Temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

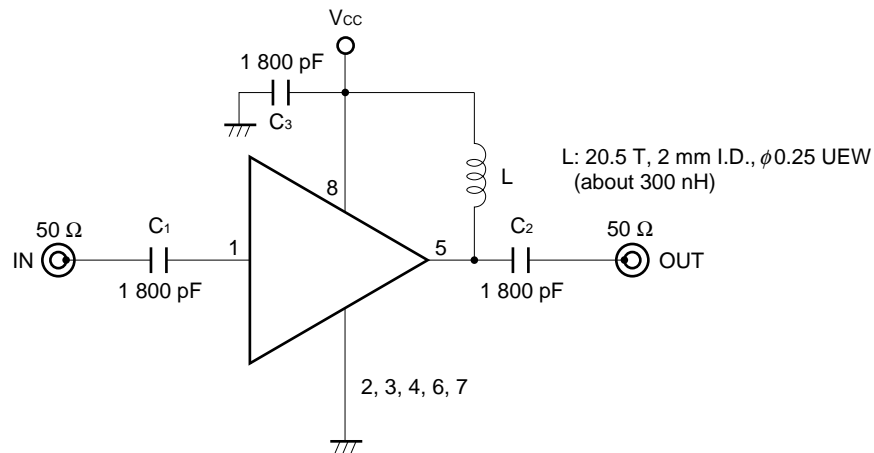
RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Notice
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	The same voltage should be applied to pin 5 and 8
Operating Ambient Temperature	$T_A$	-45	+25	+85	$^\circ\text{C}$	

ELECTRICAL CHARACTERISTICS ( $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC} = V_{out} = 5.0\text{ V}$ ,  $Z_s = Z_L = 50\ \Omega$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	$I_{CC}$	No signal	32	40	49	mA
Power Gain	$G_P$	$f = 500\text{ MHz}$	19.5	21.5	23.5	dB
Noise Figure	NF	$f = 500\text{ MHz}$	-	6.0	8.0	dB
Upper Limit Operating Frequency	$f_u$	3 dB down below the gain at 0.1 GHz	1.5	1.8	-	GHz
Isolation	ISL	$f = 500\text{ MHz}$	29	34	-	dB
Input Return Loss	$RL_{in}$	$f = 500\text{ MHz}$	9	12	-	dB
Output Return Loss	$RL_{out}$	$f = 500\text{ MHz}$	1	3	-	dB
Saturated Output Power	$P_{O(sat)}$	$f = 500\text{ MHz}$ , $P_{in} = +3\text{ dBm}$	+13.5	+15.5	-	dBm

## TEST CIRCUIT



## INDUCTOR FOR THE OUTPUT PIN

The internal output transistor of this IC consumes 30 mA, to output medium power. To supply current for output transistor, connect an inductor between the  $V_{CC}$  pin (pin 8) and output pin (pin 5). Select large value inductance, as listed above.

The inductor has both DC and AC effects. In terms of DC, the inductor biases the output transistor with minimum voltage drop to output enable high level. In terms of AC, the inductor make output-port impedance higher to get enough gain. In this case, large inductance and Q is suitable.

CAPACITORS FOR THE  $V_{CC}$ , INPUT AND OUTPUT PINS

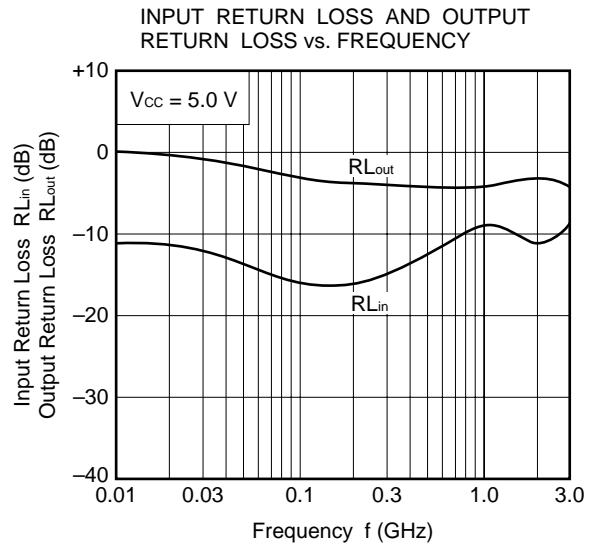
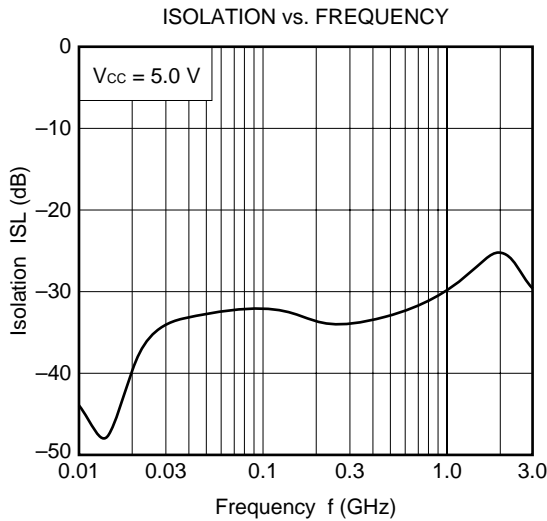
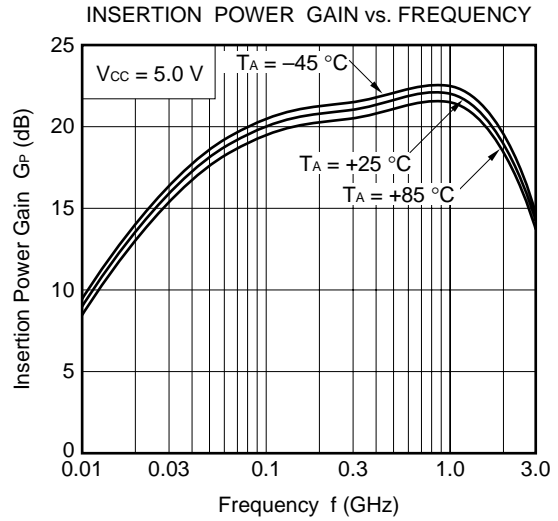
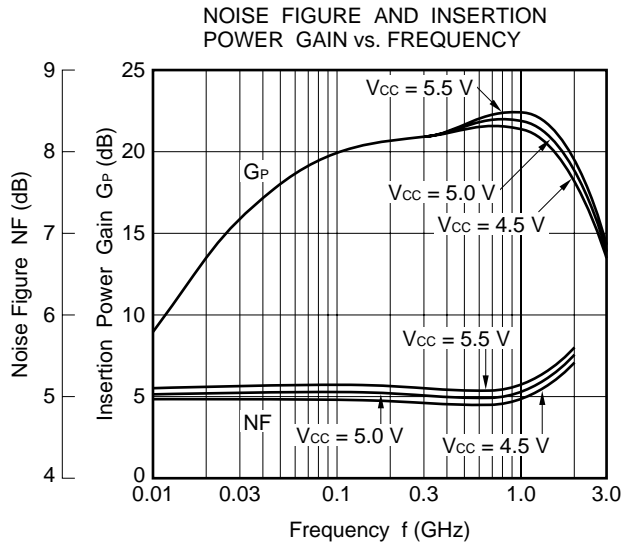
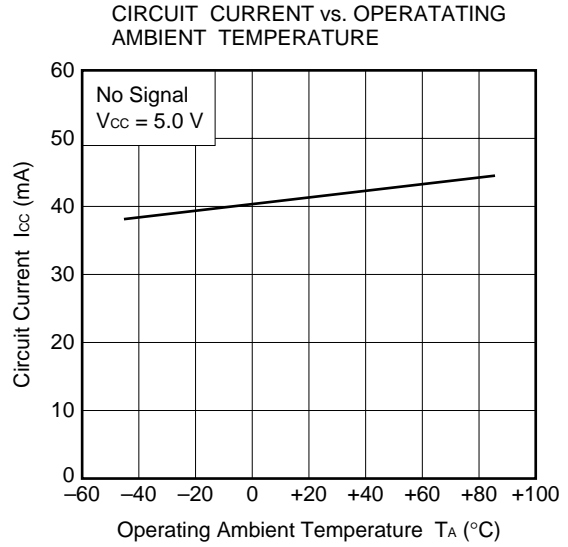
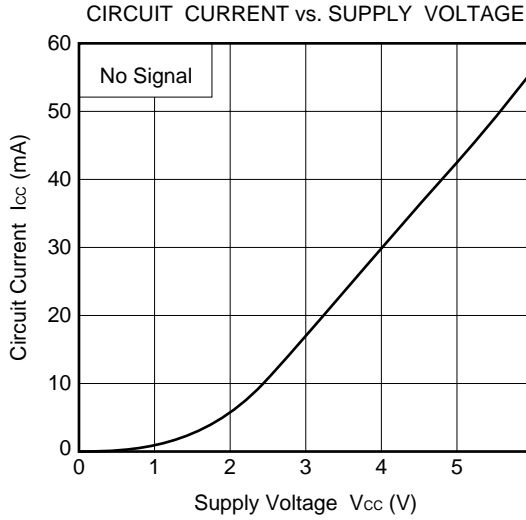
Capacitors of 1 800 pF are recommendable as the bypass capacitor for the  $V_{CC}$  pin and the coupling capacitors for the input and output pins.

The bypass capacitor connected to the  $V_{CC}$  pin is used to minimize ground impedance of  $V_{CC}$  pin. So, stable bias can be supplied against  $V_{CC}$  fluctuation.

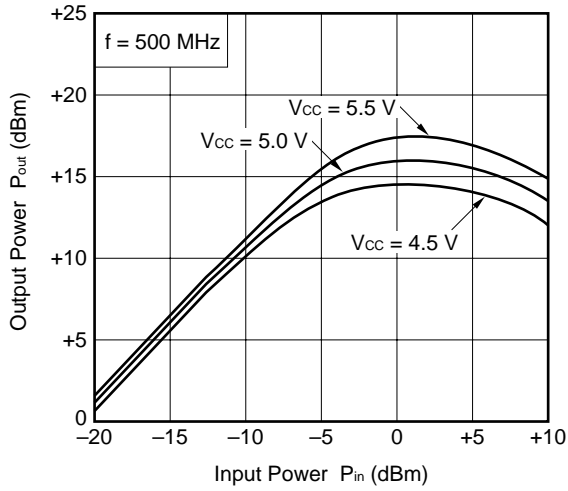
The coupling capacitors, connected to the input and output pins, are used to cut the DC and minimize RF serial impedance. Their capacitance are therefore selected as lower impedance against a 50  $\Omega$  load. The capacitors thus perform as high pass filters, suppressing low frequencies to DC.

To obtain a flat gain from 100 MHz upwards, 1 800 pF capacitors are used in the test circuit. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 10 000 pF. Because the coupling capacitors are determined by equation,  $C = 1/(2 \pi R f c)$ .

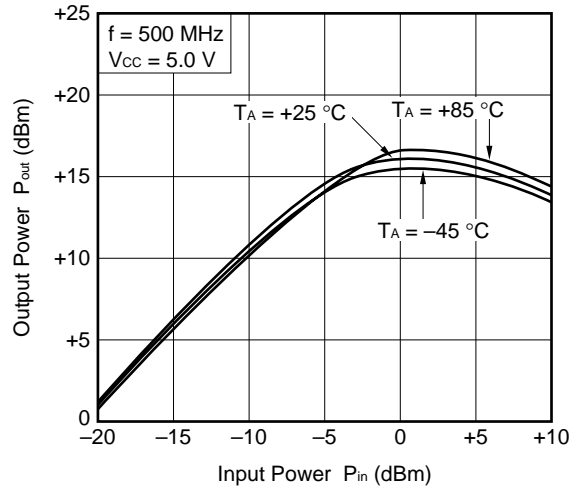
**TYPICAL CHARACTERISTICS (Unless otherwise specified,  $T_A = +25\text{ }^\circ\text{C}$ )**



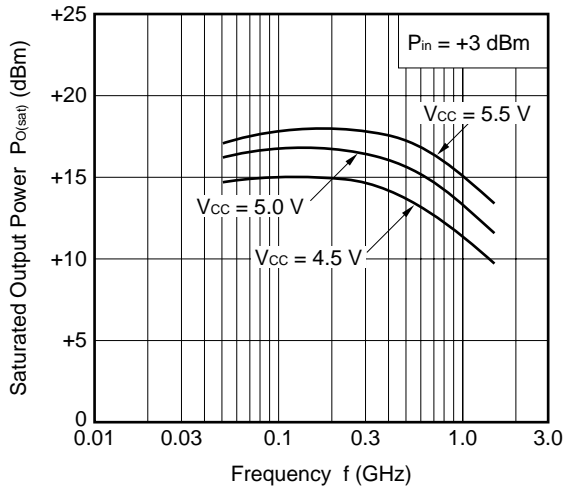
OUTPUT POWER vs. INPUT POWER



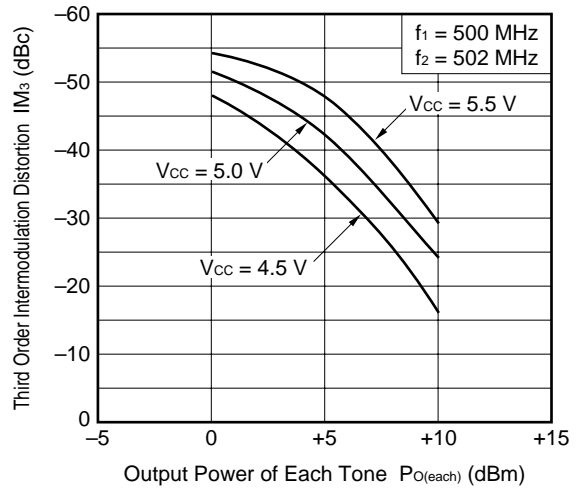
OUTPUT POWER vs. INPUT POWER



SATURATED OUTPUT POWER vs. FREQUENCY

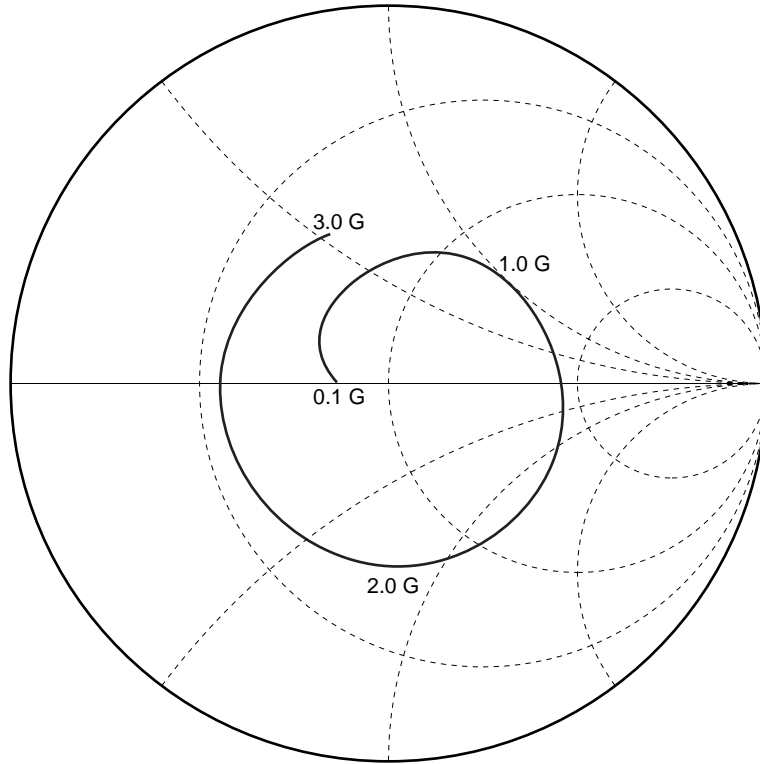


THIRD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE

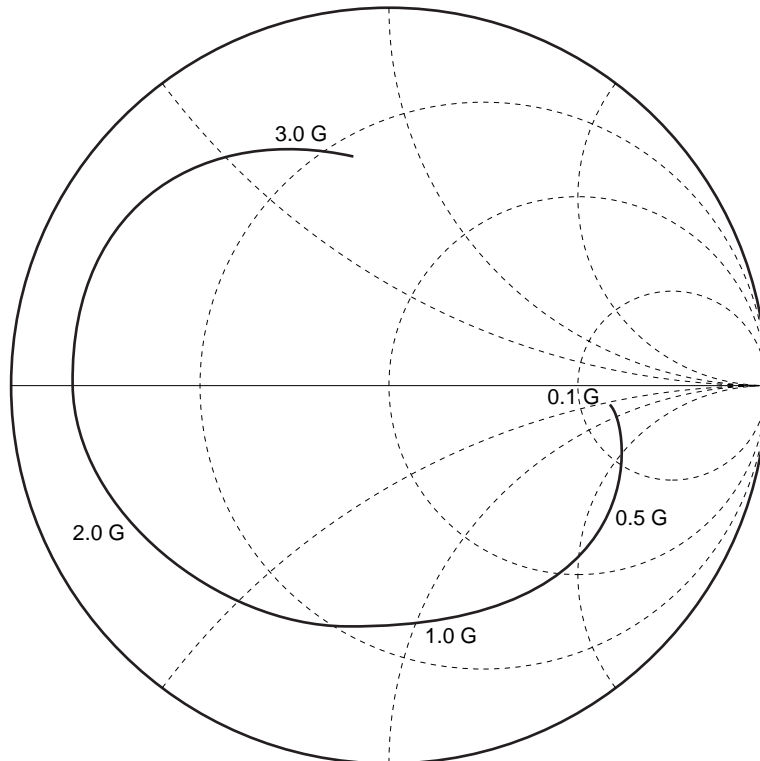


S-PARAMETER ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{out} = 5.0\text{ V}$ )

S<sub>11</sub>-FREQUENCY



S<sub>22</sub>-FREQUENCY



TYPICAL S-PARAMETER VALUES

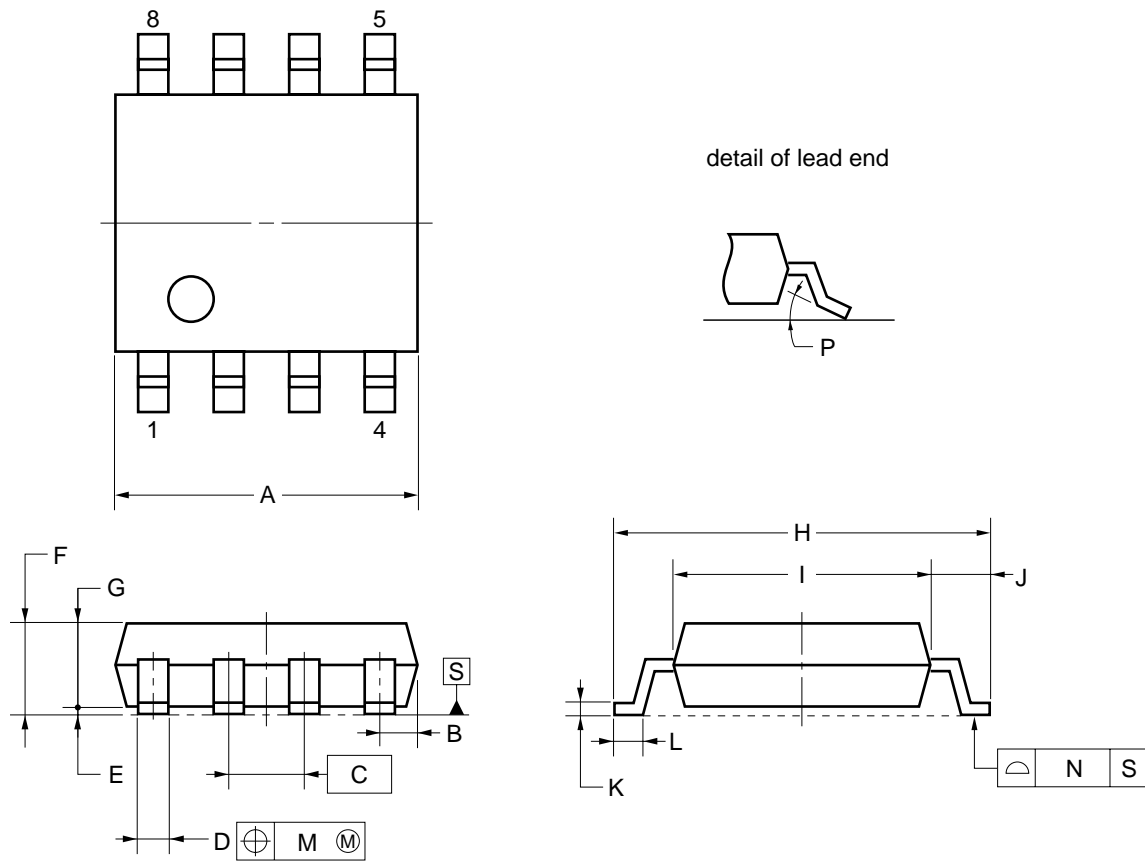
μ PC1679G

V<sub>CC</sub> = V<sub>out</sub> = 5.0 V, I<sub>CC</sub> = 40 mA

FREQUENCY MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>		K
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	
100.0000	0.133	177.2	11.167	-4.7	0.024	-4.9	0.589	-3.9	1.40
200.0000	0.154	171.2	11.585	-9.8	0.022	-10.3	0.620	-9.7	1.41
300.0000	0.184	159.6	12.121	-16.1	0.018	-3.0	0.648	-17.3	1.51
400.0000	0.217	147.3	12.690	-23.9	0.015	4.9	0.669	-25.9	1.63
500.0000	0.247	132.4	13.210	-32.2	0.015	20.0	0.681	-35.1	1.42
600.0000	0.279	117.7	13.509	-40.9	0.017	35.5	0.680	-44.3	1.15
700.0000	0.307	102.8	13.902	-51.0	0.021	42.6	0.674	-53.6	0.88
800.0000	0.333	88.3	13.966	-59.8	0.026	44.8	0.659	-62.0	0.71
900.0000	0.342	76.4	13.895	-69.5	0.027	42.5	0.628	-70.6	0.72
1000.0000	0.412	60.4	14.401	-78.5	0.033	52.0	0.646	-75.4	0.48
1100.0000	0.419	46.1	14.244	-87.9	0.037	46.1	0.636	-83.6	0.46
1200.0000	0.434	31.7	14.249	-97.3	0.041	42.5	0.635	-90.1	0.43
1300.0000	0.450	18.1	14.096	-106.9	0.043	41.8	0.640	-97.8	0.41
1400.0000	0.461	3.2	13.945	-116.9	0.047	35.8	0.655	-105.0	0.39
1500.0000	0.481	-12.2	13.888	-125.9	0.051	34.1	0.664	-112.7	0.39
1600.0000	0.486	-27.2	13.645	-136.5	0.053	30.5	0.691	-120.6	0.39
1700.0000	0.487	-43.7	13.460	-147.3	0.053	27.3	0.707	-129.2	0.42
1800.0000	0.486	-61.2	13.043	-157.9	0.056	21.6	0.742	-138.5	0.44
1900.0000	0.479	-78.4	12.509	-170.0	0.058	17.7	0.771	-147.7	0.48
2000.0000	0.469	-95.6	11.678	179.0	0.057	13.6	0.794	-158.3	0.53
2100.0000	0.467	-113.5	10.720	168.4	0.057	9.9	0.819	-169.0	0.59
2200.0000	0.454	-130.9	9.763	158.2	0.056	3.5	0.840	179.9	0.63
2300.0000	0.450	-148.4	8.754	150.0	0.054	-1.4	0.846	168.7	0.71
2400.0000	0.449	-165.0	7.849	142.4	0.050	-6.4	0.852	157.1	0.78
2500.0000	0.443	179.3	7.022	135.4	0.045	-9.9	0.829	145.9	0.90
2600.0000	0.441	163.8	6.289	130.2	0.037	-13.3	0.790	133.6	1.11
2700.0000	0.430	149.9	5.800	126.1	0.029	-11.1	0.733	124.7	1.49
2800.0000	0.426	139.0	5.277	121.8	0.027	-1.1	0.697	117.2	1.75
2900.0000	0.429	128.2	5.108	116.7	0.027	6.1	0.672	110.0	1.84
3000.0000	0.432	118.6	4.894	114.0	0.025	15.9	0.635	103.2	2.02
3100.0000	0.419	110.7	4.541	107.4	0.028	31.2	0.598	98.0	2.05

★ PACKAGE DIMENSIONS

8 PIN PLASTIC SOP (225 mil) (Unit: mm)



**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2±0.2
B	0.85 MAX.
C	1.27 (T.P.)
D	0.42 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.1±0.1
F	1.57±0.2
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	0.17 <sup>+0.08</sup> <sub>-0.07</sub>
L	0.6±0.2
M	0.12
N	0.10
P	3° <sup>+7°</sup> <sub>-3°</sub>



**NOTE ON CORRECT USE**

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation). All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
- (3) The bypass capacitor should be attached to Vcc line.
- (4) The inductor must be attached between Vcc and output pins. The inductance value should be determined in accordance with desired frequency.
- (5) The DC cut capacitor must be attached to input pin.

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235 °C or below Time: 30 seconds or less (at 210 °C) Count: 3, Exposure limit: None <sup>Note</sup>	IR35-00-3
VPS	Package peak temperature: 215 °C or below Time: 40 seconds or less (at 200 °C) Count: 3, Exposure limit: None <sup>Note</sup>	VP15-00-3
Wave Soldering	Soldering bath temperature: 260 °C or below Time: 10 seconds or less Count: 1, Exposure limit: None <sup>Note</sup>	WS60-00-1
Partial Heating	Pin temperature: 300 °C Time: 3 seconds or less (per side of device) Exposure limit: None <sup>Note</sup>	—

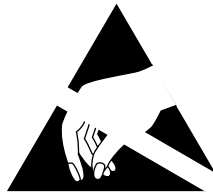
**Note** After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

**Caution** Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

[MEMO]



## ATTENTION

OBSERVE PRECAUTIONS  
FOR HANDLING  
ELECTROSTATIC  
SENSITIVE  
DEVICES

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