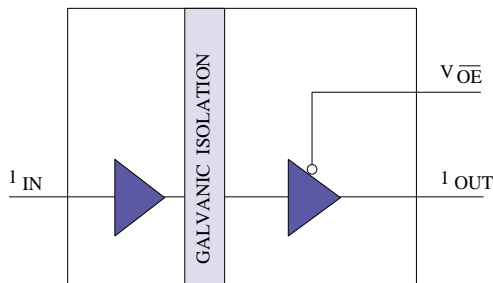


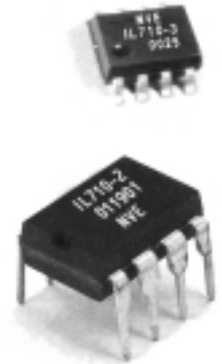
High Speed Digital Isolator

Functional Diagram



Features

- +5V and +3.3V CMOS Compatible
- 2 ns Typical Pulse Width Distortion
- 4 ns Typical Propagation Delay Skew
- 10 ns Typical Propagation Delay
- High Speed: 100 MBd
- 30 kV/μs Typical Common Mode Rejection
- Tri State Output
- 2500V_{RMS} Isolation (1 Min.)
- UL1577 Approved (File # E207481)
- IEC 61010-1 Approved (Report # 607057)



Truth Table

V _I	V _{OE}	V _O
L	L	L
H	L	H
L	H	Z
H	H	Z

Applications

- Digital Fieldbus Isolation
- Multiplexed Data Transmission
- Computer Peripheral Interface
- Noise Reduction in High Speed Digital Systems
- Isolated Data Interfaces
- Logic Level Shifting

Ordering Information

Model	Package Type	
	8-PDIP	8-SOIC
IL710	-2	-3

IL710-2 an 8-PDIP package

IL710-3 an 8-SOIC package

Description

The IL710 is a CMOS digital isolator integrated with NVE's patented* IsoLoop® technology, which gives the IL710 high speed performance and excellent transient immunity specifications. The symmetric magnetic coupling barrier gives this device a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns, giving the IL710 the best specifications of any isolator device. The IL710 also has a 100 Mbaud data rate, making it the world's fastest digital isolator. The IL710 is ideally suited for isolating such applications as PROFIBUS, RS-485, RS422, etc. It is available in 8-pin PDIP and 8-pin SOIC packages, and is specified over the temperature range of -40°C to +100°C.

IsoLoop® is a registered trademark of NVE Corporation
* US Patent number 5,831,426; 6,300,617 and others

IL710 ^{IsoLoop®}

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Storage Temperature	T _S	-55	175	°C
Ambient Operating Temperature ⁽¹⁾	T _A	-55	125	°C
Supply Voltage	V _{DD1} , V _{DD2}	-0.5	7	Volts
Input Voltage	V _I	-0.5	V _{DD1} +0.5	Volts
Input Voltage	V _{OE}	-0.5	V _{DD2} +0.5	Volts
Output Voltage	V _O	-0.5	V _{DD2} +0.5	Volts
Output Current Drive	I _O		10	mAmps
Lead Solder Temperature(10s)			260	°C
ESD	2kV Human Body Model			

Recommended Operating Conditions

Parameters	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T _A	-40	100	°C
Supply Voltage	V _{DD1} , V _{DD2}	3.0	5.5	Volts
Logic High Input Voltage	V _{IH}	2.4	V _{DD1}	Volts
Logic Low Input Voltage	V _{IL}	0	0.8	Volts
Input Signal Rise and Fall Times	t _{IR} , t _{IF}		1	µsec

Insulation Specifications

Parameter	Condition	Min.	Typ.	Max.	Units
Barrier Impedance			>10 ¹¹ 3		Ω pF
Creepage Distance (External)		7.036 (PDIP) 4.026 (SOIC)			mm
Leakage Current	240 V _{RMS} 60Hz		0.2		µAmps

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Capacitance (Input-Output) ⁽⁵⁾	C _{I-O}		1.1		pF	f= 1MHz
Thermal Resistance (PDIP)	θ _{JCT}		150		°C/W	Thermocouple located at center underside of package
(SOIC)	θ _{JCT}		240		°C/W	
Package Power Dissipation	P _{PD}			150	mW	

IEC61010-1

TUV Certificate Numbers: B 01 07 44230 001 (PDIP)
B 01 07 44230 002 (SOIC)

Classification as Table 1.

Model	Pollution Degree	Material Group	Max Working Voltage	Package Type	
				8-PDIP	8-SOIC
IL710-2	II	III	300 V _{RMS}	✓	
IL710-3	II	III	150 V _{RMS}		✓

UL 1577

Component Recognition program. File # E207481
Rated 2500Vrms for 1min.

Electrical Specifications

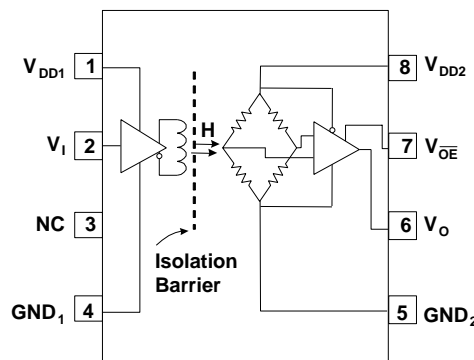
Electrical Specifications are T_{min} to T_{max} unless otherwise stated.

Parameter	Symbol	3.3 Volt Specifications			5 Volt Specifications			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
DC Specifications									
Input Quiescent Supply Current	I_{DD1}		4.5	7		6	10	μA	
Output Quiescent Supply Current	I_{DD2}		2.2	3.3		4	5	mA	
Logic Input Current	I_I	-10		10	-10		10	μA	
Logic High Output Voltage	V_{OH}	$V_{DD2}-0.1$ $0.8*V_{DD2}$	V_{DD2} $V_{DD2}-0.5$		$V_{DD2}-0.1$ $0.8*V_{DD2}$	V_{DD2} $V_{DD2}-0.5$		V	$I_O = -20 \mu A, V_I = V_{IH}$ $I_O = -4 \text{ mA}, V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0 0.5	0.1 0.8		0 0.5	0.1 0.8	V	$I_O = 20 \mu A, V_I = V_{IL}$ $I_O = 4 \text{ mA}, V_I = V_{IL}$
Switching Specifications									
Maximum Data Rate		100	110		100	110		MBd	$C_L = 15 \text{ pF}$
Pulse Width	PW	10			10			ns	
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18		10	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18		10	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High to High Impedance)	t_{PHZ}		3	5		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (Low to High Impedance)	t_{PLZ}		3	5		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to High)	t_{PZH}		3	5		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to Low)	t_{PZL}		3	5		3	5	ns	$C_L = 15 \text{ pF}$
Pulse Width Distortion ⁽²⁾			2	3		2	3		
Propagation Delay Skew ⁽³⁾	t_{PSK}		4	6		4	6	ns	$C_L = 15 \text{ pF}$
Output Rise Time (10-90%)	t_R		2	4		1	3	ns	$C_L = 15 \text{ pF}$
Output Fall Time (10-90%)	t_F		2	4		1	3	ns	$C_L = 15 \text{ pF}$
Common Mode Transient Immunity (Output Logic High or Logic Low) ⁽⁴⁾	$ CMH $ $ CML $	20	30		20	30		kV/ μs	$V_{cm} = 300V$

Pin Connections

1	V_{DD1}	Input Power Supply
2	V_I	Logic Input Signal
3	NC	No Internal Connection
4	GND_1	Input Power Supply Ground
5	GND_2	Output Power Supply Ground
6	V_O	Output Logic Signal
7	V_{OE}	Logic Output Enable*
8	V_{DD2}	Output Power Supply

*Held low Internally



IL710^{isoLoop®}

Notes:

1. Absolute Maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to the PWD divided by the pulse width.
3. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8 V$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1-4 shorted and pins 5-8 shorted.

Application Notes:

Power Consumption

isoLoop® devices achieve their low power consumption from the manner by which they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5ns wide, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers whose power consumption is heavily dependent on its on-state and frequency.

The approximate power supply current per channel for *isoLoop*® is: $I(\text{input}) = 40 \cdot \frac{f}{f_{\text{max}}} \cdot \frac{1}{4} \text{ mA}$

where $f =$ operating frequency
 $f_{\text{max}} = 50 \text{ MHz}$

Power Supplies

It is recommended that low ESR ceramic capacitors be used to decouple the supplies. 10nF capacitors should be placed as close to the device as possible between V_{DD1} and GND_1 , as well as between V_{DD2} and GND_2 .

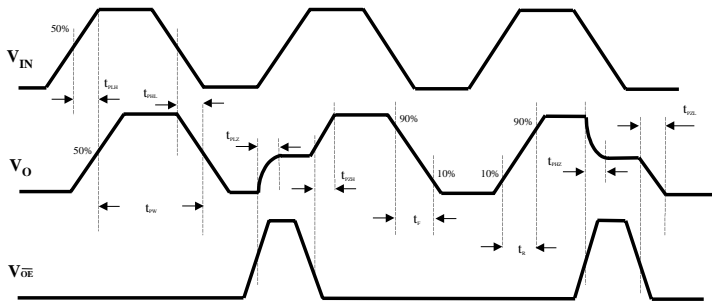
Signal Status on Start-up and Shut Down

To minimize power dissipation, the input signal to the IL710 is differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider the inclusion of an initialization signal in his start-up circuit.

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

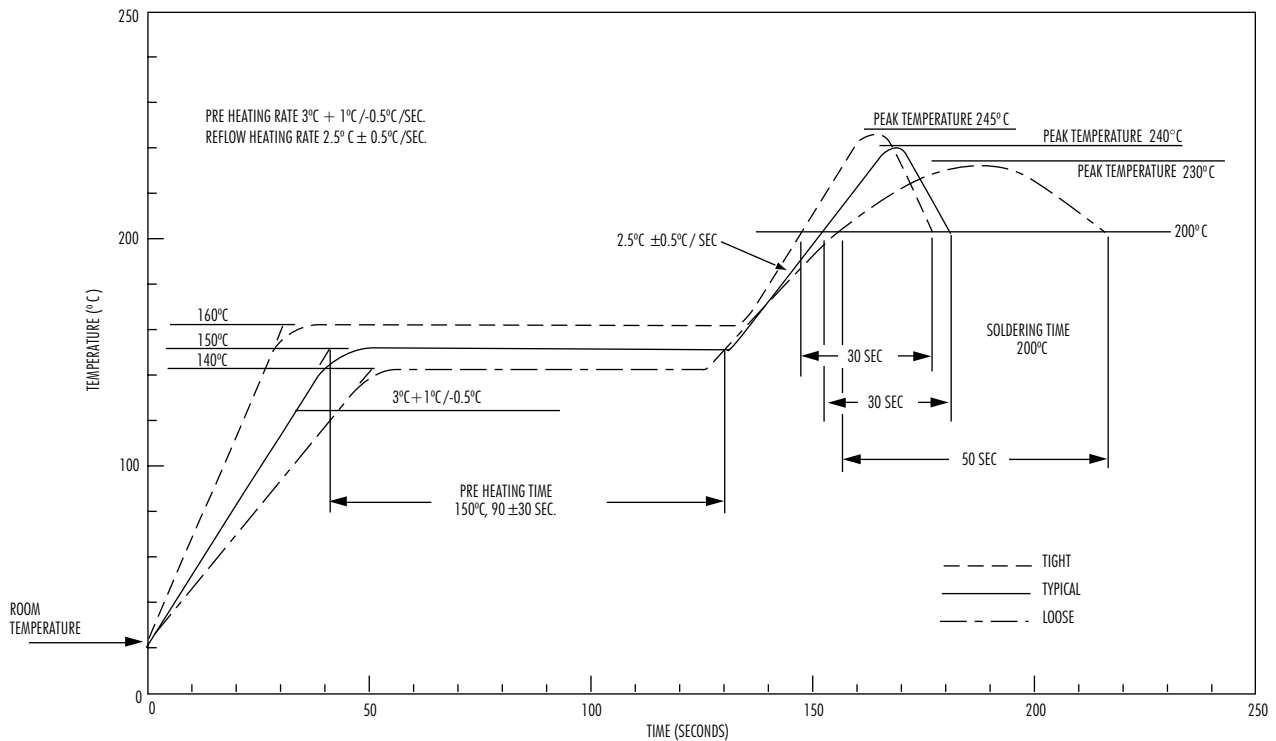
Timing Diagram



Legend

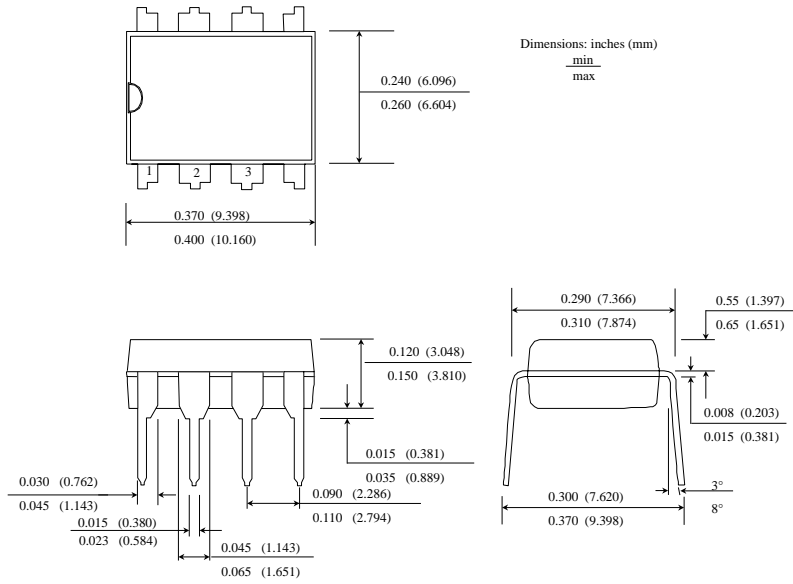
t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_{PLZ}	Propagation Delay, Low to High Impedance
t_{PZH}	Propagation Delay, High Impedance to High
t_{PHZ}	Propagation Delay, High to High Impedance
t_{PZL}	Propagation Delay, High Impedance to Low
t_R	Rise Time
t_F	Fall Time

IR Soldering Profile

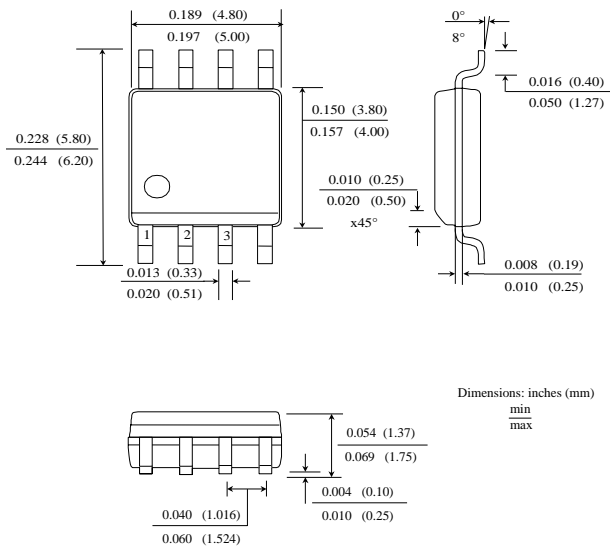


IL710 ^{IsoLoop®}

IL710-2 (8-Pin PDIP Package)

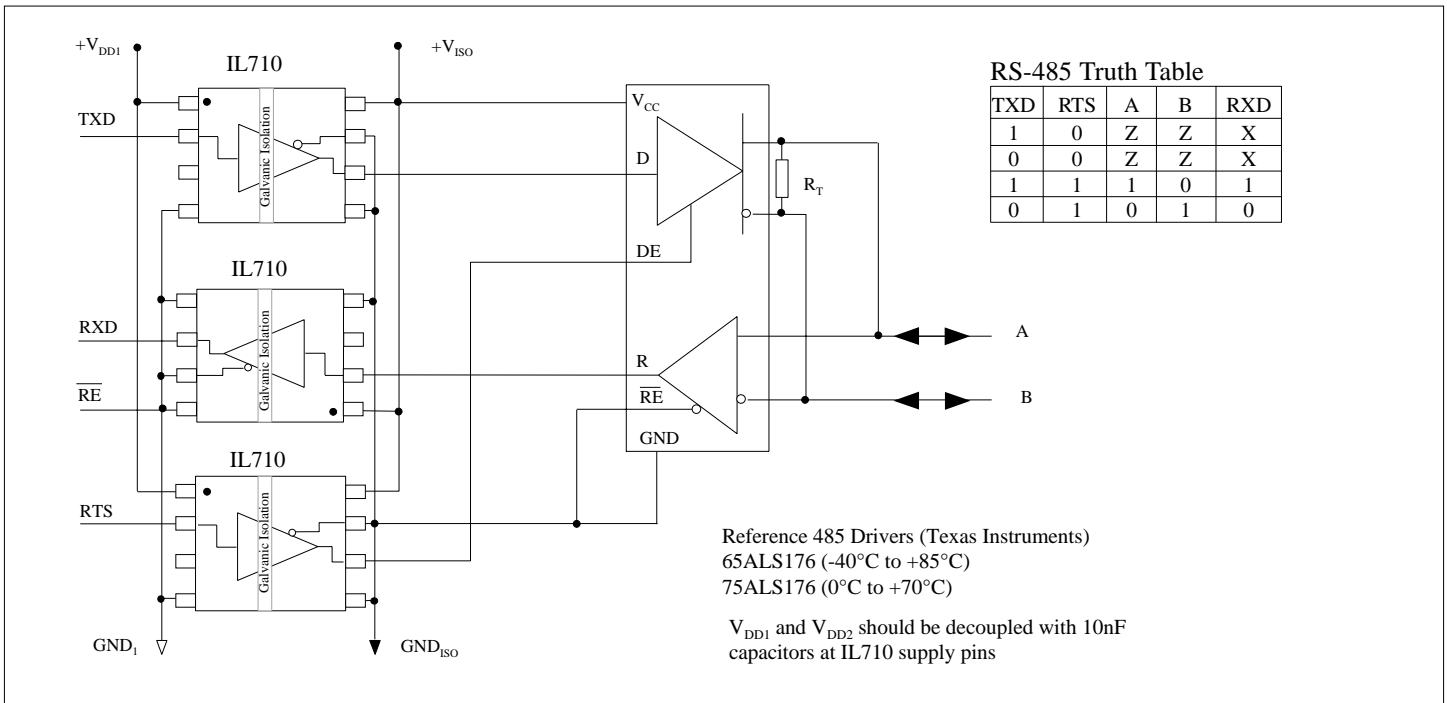


IL710-3 (Small Outline SOIC-8 package)



Applications

Isolated PROFIBUS / RS-485



Isolated DeviceNet / CAN Transceiver

