ICM515NB
Color CMOS Image Sensor
With 574x483 Pixel NTSC Composite Video Output

Data Sheet
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Features

- 277,242 (574x483) pixels, used with 1/4" optical system
- Output: NTSC-M, NTSC-J composite video
- Input interface: SIF
- Automatic exposure control
- Electronic exposure control
- On-chip 9-bit ADC
- Correlated double sampling
- On-chip digital signal processing
- Real-time color interpolation
- Automatic white balancing and color correction
- Programmable hue and contrast saturation
- Programmable luma and chroma
- Programmable gamma correction
- Automatic optical black compensation
- Horizontal & vertical images
- Low lux indicator pin(optional package)
- Scrambling control pin(optional package)
- Single 3.3 V power supply
- Low power consumption
- Capable of digital CVBS signal output

General Description

ICM-515NB is a single-chip digital color video imaging device. It incorporates a 574x483 sensor array (584x493 in physical layout) operating at 30 frames per second (60 fields/sec) in interlaced manner. Correlated double sampling is performed by the internal ADC and timing circuitry. Depending on the brightness of the scene, the raw data can be adjusted by an automatic (or manual) exposure control (AE). The raw data are further processed by a color interpolation module so that each pixel gets a complete set of RGB values. To correct or enhance color, white balancing and color correction are also performed automatically on chip. At the next stage, the gamma correction can also be performed. After these digital processing steps, the signal is fed to an embedded NTSC encoder that generates composite video output to be sent to a TV for display.

Application

- Digital camcorder
- Security system
- Visual toy
- Environment monitor system

Key Parameters

- Number of Active Pixels: 574x483
- Number of Physical Pixels: 584x493
- Frame Rate: 30 fps (60 fields/sec)
- Pixel Size: 6 μm x 5.5 μm
- Sensor Area: 3.5 mm x 2.7 mm (~ 4:3)
- Main Clock Frequency: 21.47727MHz
  (6x of 3.579545MHz)

- Exposure Time: 63.5 μs (@ 60 fps, 1 line), (33.27 ms for 524 lines)
- Sensitivity: 1.0 V/lux-sec (555 nm)
- Quantum Efficiency: 38% (555 nm)
- Dynamic Range: 57 dB (analog), 54 dB (digital)
- Digital Gain: 1/32 ~ 8X for all pixels adjust step: 0.032X
- Fill Factor: 28%
- RGB Gain: 11 bits format 3.8(default), 1/256 to 8 for individual color pattern pixels, AWB can adjust in 0.016X step
- S/N Ratio: 40 dB @ 75% full signal level
- Sensitive to infrared illumination source
- Power Supply: 3.3 V
- Power Requirement: 60 mA
- Package: Small Plastic LCC48

1. Pin Assignment (Preliminary, subject to change)

Pin #	Name	Class*	Function
13	XIN	A, I	Crystal input / external clock input
14	XOUT	A, O	Crystal output
35	PCLK (LLLED)*	D, O	Pixel clock output; (Low-lux Indicator, 1: low-lux, 0: normal)
33	SIF ID (SLWTSEL)*	D, I, N	Lsb of SIF slave address (0: 0x20 , 1: 0x21) (Wavetable selection with short(0) or long IRST(1))
34	MSSEL (ENCRYPT)*	D, I, U (D,I,N)	SIF master/slave selection. 0: slave, 1: master (Scrambling mode; 0: normal(default), 1: scrambled)
1	SCL	D, I/O	SIF clock
48	SDA	D, I/O	SIF data
17	RSET	A, I	Resistor to ground = 30 KΩ
9	RSETD	A, I	Resistor to ground = 560 Ω for CVBS output adjust
10	RSTN	D, I, U	Chip reset, active low
3	VSYNC	D, I/O	Vertical sync signal Output or Input
2	HSYNC	D, I/O	Horizontal sync signal Output Or Input
7	CPOUT(CVBS)	A, O	NTSC composite video output
15	POWERDN	D, I, U	Power down control, 0: power down, 1: active
18	AFSEL	D, I, N	Anti-flickering selection; 0: 60Hz(default), 1: 50Hz
47, 46,45, 44, 43, 40, 39, 38, 37, 36	DOUT[9:0]	D, I/O	Digital input & output for analysis purpose only
16	RAMP	A, O	Analog ramp output
11, 32	VDDA	P	Sensor analog power
12, 31	GNDA	P	Sensor analog ground
30	VDDD	P	Sensor digital power
19	GNDD	P	Sensor digital ground
6	VDDC	P	DAC analog power
8	GNDC	P	DAC analog ground
4, 41	VDDK	P	Digital power
5, 42	GNDK	P	Digital ground

Class Code: A – Analog signal; D – Digital signal; I – Input; O – Output; P – Power or ground; U – Internal pull-up; N – Internal pull-down

* Option thru different bonding at packaging

2. Functional Description

ICM-515NB is a single-chip digital color imaging device. It includes a 574x483 sensor array, 574 column-level ADC, correlated double sampling circuitry, an automatic exposure control module, a color interpolation module, programmable white balancing, a color correction module and a programmable gamma correction module. All the programmable parameters are set by writing into the SIF interface which can address the register file consisting of 8-bit registers. The output format is NTSC composite video, which includes horizontal and vertical sync signals.

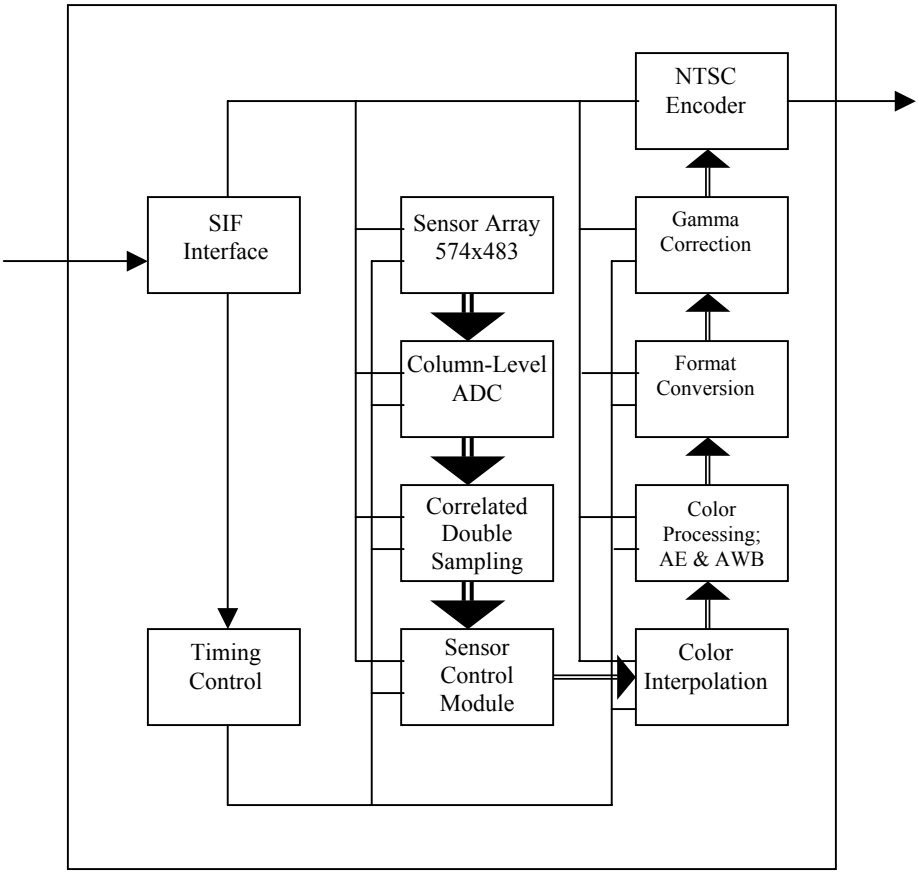


Figure 1. Block diagram

2.1 Image Array

The image array consists of 574x483 pixels. Each pixel has a light sensitive photo diode and a set of control and transfer transistors. At the beginning of the cycle, a row of pixels is pre-charged to its maximum value. Then the row is exposed to light for several lines worth of time and sampled by the ADC. A "Correlated Double Sampling (CDS)" process is performed with subtracting the reset value (sampled right before sampling the signal) from the signal value. The purpose of CDS is to eliminate the point-wise fixed pattern noise (FPN). The output of CDS is approximately proportional to the amount of received light, ranging from 0 to 512.

2.2 Color Filters and Image Signal Processing

Each pixel is covered by a color (R, G, or B) filter. Since each pixel only gets part of the spectral band, the data need further processing (i.e., color interpolation and color correction) in order to produce the full visible spectrum for best image quality.

ICM-515NB incorporates the following digital signal processing functions.

An automatic exposure (AE) time control to accommodate for different brightness, the AE feature will adjust the exposure time thru various gain control mechanisms to achieve the appropriate brightness.

An anti-flickering control circuit to eliminate flickering caused by a 50Hz or 60Hz light source normally found indoors.

A color interpolation and Automatic White Balance (AWB) module to perform color interpolation and gain on each color pixel to obtain a set of correlated RGB value for each pixel. The result of this operation is a data stream consisting of 24-bit RGB per pixel with balanced color components.

A color control module to adjust color contrast, hue, and saturation.

To boost darker signal to match the video monitor characteristic, gamma correction are performed:

$$V_o = V_i^{1/\gamma}$$

where V_i is normalized (ranged from 0 to 1) R, G, or B signal coming from the white balancing module, and V_o is normalized final output. The parameter γ is programmable with default value of 2.2.

2.3 Output Format

The output format of ICM-515NB is analog composite video output suitable for TV display. This output is tied through a parallel 75 Ω ohms resistor to ground, and to a pi-network of one 1.7 μH inductor and two 560 pF capacitors, before connecting to a 75 Ω cable.

3. SIF Registers

Address	Name	Default	Description
0x00	PART_CONTROL	0x4a	Processing control [0] Reserved [1] (One shot) Auto-slope, 1:enable, 0: disable; [2] Exposure time control, writing a 1 will activate the new value set in AD_EXPOSE_TIME, when read back from it, 0 means the exposure time change is finished. 1 means either the exposure time change is still in progress [3] dead pixel filter 1:enable 0:disable. [4] Scrambling mode control, 0: normal, 1:enable [5]Reserved [6] Reserved [7] Latent change, writing a 1 means the changed latent registers now starts taking effect, when the entire operation is done, the read back value of this bit will change from 1 to 0.
0x01 0x02	TIMING_CONTROL_LOW TIMING_CONTROL_HIGH	0x4041	Timing control [0] Column count enable, set to 0 when filling wave table, set to 1 when normal operation. [1] HSYNC polarity, 0: active low, 1: active high. [2] VSYNC polarity, 0: active low, 1: active high. [7][3] Auto dark correction control: 00: disable auto dark, 01:when AE update,Auto dark function 10,11: enable auto dark [4] Wavetable select, 0: wavetable timing (default, register setting, short IRST), 1: Fixed setting timing(long IRST) [5] ET_fast enable, 1: expose time update at once 0:expose time update with a step and time control [6] DOUT input or output select, to decide output data or load data form outside 0: input 1: output [8] IRST select, 0: from wave table, 1: from IRST_NUMBER register [10][9] RGBG Pattern starting point RG1BG2 pattern: 00: RG1BG2 01:G1BG2R 10:BG2RG1 11:G2RG1B G2BG1R pattern: 00: G2BG1R 01: BG1RG2 10:G1RG2B 11:RG2BG1 [11] vsync for Field or Frame, 1:field 0:frame

			[12] Out-of-array exposure pointer control 0: point to stop row (default 490, see Reg. 0x16). 1: point to row 493 (a non-existent row) [13] Column stop, when exceeding real array column: 0: point to column 584 (a non-existent column) 1: sensor column keeps counting every row [14] hsync,vsync input or output select, to decide hsync and vsync in master mode or slave mode 1:output, 0:input, [15] RG1BG2 or G2BG1R pattern select 0:RG1BG2 pattern 1:G2BG1R pattern
0x03	AD_FIELD1_BEGINL*	0x04	[7:0] field1[7:0] Beginning of Field 0 in terms of line counter
0x04	AD_FIELD_BEGINH*	0x04	[1:0] field1[9:8] [3:2] field2[9:8] [7:4]Reserved
0x05	AD_FIELD2_BEGINL*	0x0A	[7:0] field2[7:0] Beginning of Field 1 in terms of line counter
0x07	TABLE_LEN	0x10	[4:0] Wave table length
0x09 0x0A	IRST_NUMBER_LOW IRST_NUMBER_HIGH	0	[9:0] IRST duration in terms of multiples of 1024 clock cycles (167 ns each)
0x0B	AD_ROW2_BEGINL*	0x19	[7:0] Beginning of sensor row for field2 in terms of line position, row_begin2[7:0]
0x0C 0x0D	AD_WIDTHL* AD_WIDTHH*	0x0555 (1365)	[10:0] Frame width
0x0E 0x0F	AD_HEIGHTL* AD_HEIGHTH*	0x020D (525)	[9:0] Frame height
0x10 0x11	AD_COL_BEGINL* AD_COL_BEGINH*	0x0094 (148)	[10:0] Beginning of active line in terms of column position [11] Left-right Mirror image enable [12] Up-Down Mirror image enable
0x12 0x13	AD_SCOL_ENDL* AD_SCOL_ENDH*	0x0247 (583)	[9:0] End of sensor array in terms of column position, count by pclk
0x14	AD_ROW1_BEGINL*	0x12	[7:0] Row begin1 [7:0], Beginning of sensor row for field1, in terms of line position,
0x15	AD_ROW_BEGINH*	0x14	[1:0] row_begin1[9:8] [3:2] row_begin2[9:8] [5:4] stop_row_high[9:8]
0x16	AD_STOP_ROWL	0xEA	[7:0] stop_row[7:0], stop row low bits
0x17	AD_ROW_DELTA*	0x04	[4:0] the max Expose time change step when ET_fast=0
0x18 0x19	AD_HSYNC_ENDL AD_HSYNC_ENDH	0x0040 (64)	[10:0] End of horizontal sync in terms of col_ cnt,count by clk
0x1A 0x1B	AD_VSYNC_ENDL AD_VSYNC_ENDH	0x0003 (3)	[9:0] End of vertical sync in terms of line position
0x1C 0x1D	AD_EXPOSE_TIMEL AD_EXPOSE_TIMEH	0x020C (524)	[9:0] Exposure time in terms of number of lines
0x20 0x21	AD_M1_L* AD_M1_H	0x140 (320)	[10:0] Gain coefficient (R) , in unsigned 3.8(default) format

0x22 0x23	AD_M2_L* AD_M2_H	0x140 (320)	[10:0] Gain coefficient (G1) , in unsigned 3.8 (default) format
0x24 0x25	AD_M3_L* AD_M3_H	0x240 (576)	[10:0] Gain coefficient.(B) , in unsigned 3.8 (default) format
0x26 0x27	AD_M4_L* AD_M4_H	0x140 (320)	[10:0] Gain coefficient.(G2) , in unsigned 3.8 (default) format
Contrast, Hue, Brightness, Gamma, Saturation parameters			
0x28	AD_CONTRAST*	0x03	[2:0] Adjust Y Contrast, 0: 0.25 1: 0.5 2: 0.75 3: 1 4: 1.25 5: 1.5 6: 1.75 7: 2
0x29	AD_SIN*	0x00	[6:0] SIN value(abs), 0.7 format [7] sign bit, 1:negative, 0:positive
0x2A	AD_COS*	0x7F	[6:0] COS value(abs), 0.7 format [7] sign bit, 1:negative, 0:positive
0x2B	AD_BRIGHT_OFFSET*	0x00	[7:0] Y = Y + Bright_offset [6:0] Bright_offset value(abs), [7] sign bit, 1:negative, 0:positive
0x2C	AD_GAMMA*	0x2a	[1:0] R Gamma Correction [3:2] G Gamma Correction [5:4] B Gamma Correction 0: modified 2.2 1: 1.9 2: NTSC 2.2 (default)
0x2D	AD_SATURATION*	0x40	[6:0] Saturation Factor, (U,V) = (U,V) * Saturation Factor, 2.5 format,x2 for default
DSP Test, Edge sharpening, digital gain, white balance parameters			
0x2E	AD_DSP_TEST	0xaa	[7:0] DSP input Test Register, [9:8] in AD_CNTRL_W3
0x2F	AD_DSP_CTRL	0x00	[2:0] DSP input source selection 0,7: 9bit RAW data, default 1: control signal, 9bitX2 2: row address, 9bitX2 3: column address, 10bit 4: Test Register, 10bit 5: Data from DOUT, 10bit 6: line count 10bit [4:3] DSP output selection 0:Y,Cb,Cr after AWB correction 1: Y,Cb,Cr after sharpen and Hue,saturation adjust 2: Y,Cb,Cr after sharpen,Gamma,and Hue,saturation adjust 3: Y,Cb,Cr after Sharpen ,Gamma , offset , Hue,saturation adjust
0x30	AD_SP_CTRL*	0x09	[4] 1: average interpolation, 0: adjacent interpolation [3] 1: sharpness enable, 0: sharpness disable [2:0] sharpness high tone weight, 0: 0.5 1: 1 (default) 2: 1.5 3: 2

			4: 2.5 5: 3 6: 3.5 7: 4
0x31	AD_SP_Hith	0x0A (10)	[7:0] sharpness high tone threshold
0x33	AD_AWB_CTRL*	0xC7	[0] 0:disable AWB 1:enable AWB [1] 0: G, R, B has range limit, R>G/2 & G>R/2 & B>G/2 & G>B/2 1: Gray Wall method [2] Image changing low pass filter, 0:disable 1:enabl [3] low pass adjust step, 0: 1/8, 1:1/4 [6] 0: Disable AWB either at low lux or AE is changing; 1: AWB is always ON. [7] AWB sampling area selection 0:Center 1:whole Frame
0x1E	AD_AWB_GAIN_CTRL	0xF8	Min value: [3:0]x1/8; Max value: [7:4]x1/4
0x1F	AD_AWB_WF_CTRL	0xB0	[4:0] AWB sampling frequency in terms of frame period: [4:0]x2; [7:5] White pixel limit: 2^([7:5]+4)
0x34	AD_AWB_OVERFLOW*	0xFE (254)	[7:0] AWB overflow limit, if "R,G,B" of pixel > (overflowx2+1), this pixel will not be satisfied.
0x35	AD_AWB_BRIGHTTH*	0x00	[7:0] AWB Bright limit, if "G"/2 of pixel > Bright limit, this pixel will be satisfied.
0x36	AD_DG_GAIN*	0x20	[7:0] digital gain, 3.5 format When AE on, read back AE`s Digital Gain
0x37	AD_WB_RED*	0x70	[7:0] white balance red gain, 2.6 format
0x38	AD_WB_GREEN*	0x80	[7:0] white balance green gain, 2.6 format
0x39	AD_WB_BLUE*	0x90	[7:0] white balance blue gain, 2.6 format
Auto exposure control parameters			
0x3A	AD_AE_CTRL*	0xF7	[0] 0:disable AE, 1:enable AE [1] 0:disable Digital Gain compensation, 1:enable Digital Gain compensation [2] 0:disable Anti-Flicker, 1:enable Anti-Flicker [3] ET_fast control, 0:ET search start from former ET, 1:ET search start from 524 [7:4] x2: The image change frame number tolerance
0x3B	AD_AETARGET	0x38 (56)	[7:0] AE Y target, Y=(2R/8+5G/8+B/8)*1/2
0x3C	AD_AETOLE	0x08	[7:0] AE Y change tolerance
0x3D 0x3E	AD_BLL AD_BLH	0xC0	[10:0] bright pixel number limit,10% of sampling pixel number:2040 ,if the bright pixel number > limit, this frame is over exposed, AE target is reduced automatically by 10
0x40	AD_AEGAIN_CTRL	0x78	Digital gain limit [3:0] x1/8: min digital gain limit [7:4] x1/2 max digital gain limit
0x43	AD_AESTEP	0xBF	AE adjust step ratio to expected step [2:0]: 1/2^[2:0]: the ratio for ET increase step; min step is (1/32) [5:3:] 1/2^[5:3]: the ratio for ET decrease step; min step is (1/32)

			[7:6]: 1/2^([7:6]+2): the ratio for Digtal gain adjusting step
0x44	AD_AFSTEP	0x83	[7:0] Anti Flicker Exposure time adjust step under 30 fps, 131(60Hz), 158(50Hz)
0x45	AD_YBRIGHT	0x68 (104)	[7:0] Bright Limit, if "Y" > Birght Limit, the pixel is bright pixel
AE and AWB status parameters for controller debugging purpose(read only)			
0x46	AD_YCAverage®		[7:0] Y average value for center of a frame
0x47	AD_Yaverage®		7:0] Y average value for a whole frame
0x48 0x49	AD_NTBPL® AD_NTBPH		[10:0] Number of too bright pixel
0x4A	AD_AWBR®		[7:0] R average value for a frame
0x4B	AD_AWBG®		[7:0] G average value for a frame
0x4C	AD_AWBB®		[7:0] B average value for a frame
0x4D 0x4E	AD_AWBpixelL® AD_AWBpixelH		[10:0] The number of pixel which is valid AWB criteria
0x4F	AD_AWBRGBH®		R,G,B average MSB [0] Raverage[8] [1]Gaverage[8] [2]Baverage[8]
Output format, CDS and dead pixel control parameters			
0x52	AD_INOUTSEL**	0x0b	[7] Reserved [6] choose the DAC source 0: CVBS(TV) 1:DSP input source according to AD_DSP_CTRL [5] swap Cb,Cr sequence when output YCbCr [4:0] Normal output select [4] 0:ouput DSP 1: output NTSC [4:0]: 5'h0: 3.8 format rawdata after auto dark 5'h1: 4.7 format rawdata after auto dark 5'h2: 5.6 format rawdata after auto dark 5'h3: 6.5 format rawdata after auto dark 5'h4: rawdata after deadpixel remove and sign process 5'h5: R channel data after interpolation 5'h6: G channel data after interpolation 5'h7: B channel data after interpolation 5'h8: control siganl adc_vector[8:0] 5'h9: sensor row[8:0] 5'ha: sensor column[9:0] 5'hb: DSP input source according to AD_DSP_CTRL 5'hc: Reserved 5'hd: Y channel output according to AD_DSP_CTRL output 5'he: YCbYCr or YCrYCb output according to [5] 5'hf: CbYCrY or CrYCbY output according to [5] 5'h10: digital CVBS output 5'h11: digital Chrominance(C) output 5'h12: digital luminance(Y) output

			5'h13: digital Y signal after lpf with Sync,black,blank signal 5'h14: digital Cb signal after lpf with Burst,blank signal 5'h15: digital Cr signal after lpf with Blank signal 5'h16: digital Chrominance(C) output without adjustment
0x53	AD_BGREFSEL	0	[7] External bandgap reference voltage enable
0x54 0x55	AD_DSRSTL AD_DSRSTH	0x0000	[9:0] Reset (DA1) overflow value
0x56 0x57	AD_DSDATAL AD_DSDATAH	0x03FF (1023)	[9:0] Data (DA2) overflow value
0x5C	AD_RSTSEL	0x40	[7:6] RSTL voltage select 0: 0.7V 1:0.9V 2: 1.1V
0x68 0x69 0x6A	AD_DEADC0L AD_DEADC0H AD_DEADR0L	0xFF0FFF	[7:0] Dead Pixel #0 Column Adress[7:0] [1:0]: Column Adress[9:8],[3:2]:Row Adress[9:8] [7:0] Dead Pixel #0 Row Adress[7:0]
0x6C 0X6D 0x6E	AD_DEADC1L AD_DEADC1H AD_DEADR1L	0xFF0FFF	[7:0] Dead Pixel #1 Column Adress[7:0] [1:0]: Column Adress[9:8],[3:2]:Row Adress[9:8] [7:0] Dead Pixel #1 Row Adress[7:0]
0x70 0x71 0x72	AD_DEADC2L AD_DEADC2H AD_DEADR2L	0xFF0FFF	[7:0] Dead Pixel #2 Column Adress[7:0] [1:0]: Column Adress[9:8],[3:2]:Row Adress[9:8] [7:0] Dead Pixel #2 Row Adress[7:0]
0x74 0x75 0x76	AD_DEADC3L AD_DEADC3H AD_DEADR3L	0xFF0FFF	[7:0] Dead Pixel #3 Column Adress[7:0] [1:0]: Column Adress[9:8],[3:2]:Row Adress[9:8] [7:0] Dead Pixel #3 Row Adress[7:0]
0x78 0x79 0x7A	AD_DEADC4L AD_DEADC4H AD_DEADR4L	0xFF0FFF	[7:0] Dead Pixel #4 Column Adress[7:0] [1:0]: Column Adress[9:8],[3:2]:Row Adress[9:8] [7:0] Dead Pixel #4 Row Adress[7:0]
0x7C 0x7D 0x7E	AD_DEADC5L AD_DEADC5H AD_DEADR5L	0xFF0FFF	[7:0] Dead Pixel #5 Column Adress[7:0] [1:0]: Column Adress[9:8],[3:2]:Row Adress[9:8] [7:0] Dead Pixel #5 Row Adress[7:0]
Chip ID and NTSC encoder parameters			
0x80	AD_LADJL	0x70	Luma (Y) adjust, format 1.7
0x81	AD_CADJL	0x80	Chrominace(C) adjust, format 1.7 NTSC-M:8'h80 NTSC-J:8'h8a
0x82 0x83	AD_IDL AD_IDH	0xD152	[3:0] Sub ID ,[15:4] Device ID, default 0xD15, can be configured using SIF
0x85	AD_HSYLEVEL	0x08	HSYNC Level [7:0]x2
0x86	AD_BURLEVEL	0x70(112)	Burst Level [7:0]
0x87	AD_BLACKLEVEL	0x78 (120)	Black level: [7:0]*2
0x88	AD_BLANKLEVEL	0x78 (120)	Blank level: [7:0]*2

0x89	AD_CNTRL_W3	0x20	DAC control [0] Look-ahead 1:enble [1] DAC power down 1:power down [2] SVB of DAC [3] TSTA of DAC [5:4] MSB[9:8] for DSP input Test Register
Wound pixel filter, autodark, dark offset parameters			
0x8A	AD_Limit_H	0x6A	[7:4]: turn-on threshold for low lux wound pixel removal: ([7:4]+1)x1/4 [3] 1: enable wound pixel removal [2] lowluxlimit[8] [1] highlimit[8], [0]:lowlimit[8]
0x8B	AD_HighLimit_L	0x90	highlimit[7:0]
0x8C	AD_LowLimit_L	0x00	lowlimit[7:0]
0x8D	AD_LowHighLimit_L	0x06	High limit for Lowluxlimit[7:0]
0x84	AD_DARK1_OFFSET	0x00	R dark offset [7] sign bit in 2's complement
0x7F	AD_DARK2_OFFSET	0x00	G1 dark offset [7] sign bit in 2's complement
0x8E	AD_DARK3_OFFSET	0x00	B dark offset [7] sign bit in 2's complement
0x8F	AD_DARK4_OFFSET	0x00	G2 dark offset [7] sign bit in 2's complement
0x90	AD_DARK_DATA	0	[7:0]x2: When auto dark correction is disabled, serve as the subtrahend for dark correction
Sensor array control parameters			
0x91	AD_SLOPEREG	0x87	[3:0] Slope rate select, larger value means steeper ramp slope, resulting in smaller value [7:4] Slope begin voltage select 0: 1.0 V 1: 1.1 V 2: 1.2 V 3: 1.3 V 4: 1.4 V 5: 1.5 V 6: 1.6 V 7: 1.7 V 8: 1.8 V(default) 9: 1.9 V a: 2.0 V b: 2.1 V c: 2.2 V
0x92	AD_TXRSTSEL	0x22	[3:0] TXH voltage select 0: 1.4 V 1: 1.5 V 2: 1.7 V (default) 3: 1.9 V 4: 2.0 V 5: 2.1 V 6: 2.2 V 7: 2.3 V 8: Vdd 9: Vdda-0.1V a: Vdda-0.2V b: Vdda-0.3V c: Vdda [6:4] TXL voltage select 0: 0.0 V 1: 0.6 V 2: 0.7 V (default) 3: 0.8 V 4: 1.0 V
0x93	AD_SUBPH_PULSE	0x10 (16)	[3:0] Width of CDS subtraction pulse 0: 1 clock width 1: 2 clock width [7:4] Period of CDS subtraction pulse 0: 1 clock width 1: 2 clock width
0x94	AD_BITCONTROL	0x00	[6]: enable small amount of current into the

			tracking pixel 1:enable 0:disable [7]:Ramp beginning reference scheme selection 0: referenct to gnd 1:enable tracking circuit
0x97 0x98	AD_WT_BEGINL** AD_WT_BEGINH	0x0	[10:0] Wave table start point, according to col_cnt
0x99 0x9A	AD_WT_ENDL** AD_WT_ENDH	0x0555 (1365)	[10:0] Wave table end point, when it is reached, the waveform will remain fixed until the start of next row
0x9B 0x9C	AD_SUB_EN_TIMEL AD_SUB_EN_TIMEH	0x0537 (1335)	[10:0] col_cnt position where the CDS subtraction pulse is applied
Registers for AE and AWB debug (Read only)			
0xA0	AD_AWBRgain®		AWB Red Gain,format 2.6
0xA1	AD_AWBBgain®		AWB Blue Gain,format 2.6
0xA2	AD_AEHIGHTH_OUT®		Current AE Y average max value
0xA3	AD_AELOW_OUT®		Current AE Y average min Value
0xA4 oxA5	AD_AEETL® AD_AEETH		Expose time after AE without antiflicker
0xA6 0xA7	AD_AEF_ETL® AD_AEF_ETH		Expose time after antiflicker,the final value to adjust
0xA8	AD_TESTPIN®		AE FSM test Register [3:0]: AE_state[3:0] [4]: ETTYPE [5]: AWBActive [6]: ET_LOOP [7]: SScene Change
0xAB 0xAC	AD_DATAOUTL® AD_DATAOUTH		the DOUT value Register DOUT[9:0]
0xAD	AD_PART_CONTROL_C®	0x40	[7:0] Current part control setting, read only
0xB1	AD_YASTBALE®		Current AE Yavg_stable value
0xB2	AD_DIFFABS®		Current AE diff_abs value
0xB3 0xB4	AD_INCSTEPL ® AD_INCSTEPH		current AE ET inc_step[9:0] value
0xB5 0xB6	AD_DECSTEPL® AD_DECSTEPH		current AE ET dec_step[9:0] value
0xB7 0xB8	AD_YFPXLL® AD_YFPXLH	0x7F8 (2040)	whole Frame sampling pixel number
0xB9 0xBA	AD_YCPXLL® AD_YCPXLH	0x7F8 (2040)	center Frame sampling pixel number
Wavetable registers			
0xC0	WAVE0_L WAVE0_M WAVE0_H	0x2C003	wave_table Register [10:0]: the state hold time in col_cnt, count by clk [19:11]: adc_vector[8:0]
0xC3	WAVE1_L WAVE1_M WAVE1_H	0x2C014	wave_table Register dalinit: adc_vector[8]; sen_row_sel adc_vector[7]; iword adc_vector[6]; irst adc_vector[5];
0xC6	WAVE2_L WAVE2_M WAVE2_H	0x3C015	

0xC9	WAVE3_L WAVE3_M WAVE3_H	0x2C019	// suben:1 adc_vector[4]; itx adc_vector[3]; bitfast adc_vector[2]; dalsel adc_vector[1]; slopeen adc_vector[0];
0xCC	WAVE4_L WAVE4_M WAVE4_H	0x6C01D	
0XCF	WAVE5_L WAVE5_M WAVE5_H	0x6C020	
0XD2	WAVE6_L WAVE6_M WAVE6_H	0xEC022	
0XD5	WAVE7_L WAVE7_M WAVE7_H	0x6C024	
0xD8	WAVE8_L WAVE8_M WAVE8_H	0x6CB26	
0xDB	WAVE9_L WAVE9_M WAVE9_H	0x6C328	
0xDE	WAVE10_L WAVE10_M WAVE10_H	0x6D333	
0xE1	WAVE11_L WAVE11_M WAVE11_H	0xFD335	
0xE4	WAVE12_L WAVE12_M WAVE12_H	0x7D337	
0xE7	WAVE13_L WAVE13_M WAVE13_H	0x6D22B	
0xEA	WAVE14_L WAVE14_M WAVE14_H	0x6D554	
0xED	WAVE15_L WAVE15_M WAVE15_H	0x68000	
0xEF	WAVE16_L WAVE16_M WAVE16_H	0x68000	
0xF3	WAVE17_L WAVE17_M WAVE17_H	0x68000	
0xF3	WAVE17_L WAVE17_M WAVE17_H	0x68000	
0xF6	WAVE18_L WAVE18_M WAVE18_H	0x68000	

0xF9	WAVE19_L WAVE19_M WAVE19_H	0x68000	

(*) Synchronized with frame begin.
(**) Need PART_CONTROL[7] to change value, which synchronizes with frame begin.
® Read only

ICM515NB can work in three modes:

a. Normal Mode: RAW sensor data output from DOUT[9:0], TV signal output on CPOUT
b. DSP Test Mode: Test patterns including column addresses generated on-chip as input, encoded as digital CVBS output to DOUT[9:0]
c. DAC Test Mode: external data can be applied to pins DOUT[9:0] to test DAC directly. When captured by rising edge of PCLK, the output may have 1 clock delay if using DAC's LOOKAHEAD structure. Normal DAC mode will not have delay.

The three modes are controlled by:
AD-INOUTSEL(0X52), AD_DSP_CTRL(0X2f), TIMING_CONTROL_LOW(0X01)

AD_INOUTSEL	AD_DSP_CTRL	TIMING_CONTROL_LOW	MODE	Comment
8'h0b	8'h00	8'h41	a	Default
8'h10	8'h03	8'h41	b	Part_control[7] sync
8'h4b	8'h05	8'h11	c	Part_Control[7] sync

4. Electrical Characteristics

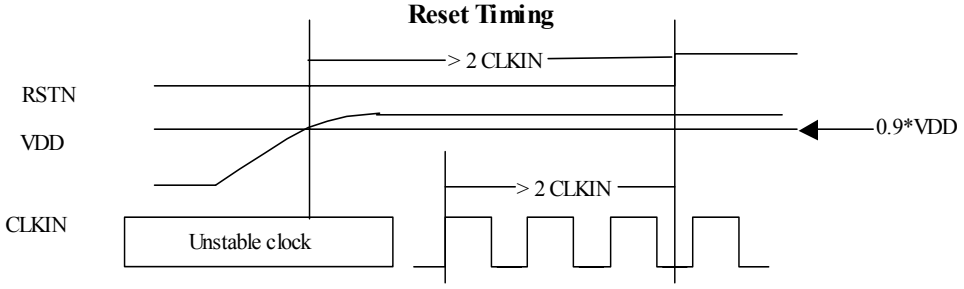
4.1 DC Characteristics

Symbol	Parameter	Rating			Unit
		Minimum	Typical	Maximum	
V_{CCA}	Absolute Power Supply	-0.3		3.8	V
V_{INA}	Absolute Input Voltage	-0.3		V_{CC} + 0.3	V
V_{OUTA}	Absolute Output Voltage	-0.3		V_{CC} + 0.3	V
T_{STG}	Storage Temperature	0	25	65	°C
V_{CC}	Operating Power Supply	3.0	3.3	3.6	V
V_{IN}	Operating Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	0	25	55	°C
I_{DD}	Operating Current @ V_{CC}=3.3 V, 25 °C		30		mA
I_{IL}	Input Low Current	-1		1	µA
I_{IH}	Input High Current	-1		1	µA
I_{OZ}	Tri-state Leakage Current	-10		10	µA
C_{IN}	Input Capacitance		3		pF
C_{OUT}	Output Capacitance		3		pF
C_{BID}	Bi-directional Buffer		3		pF

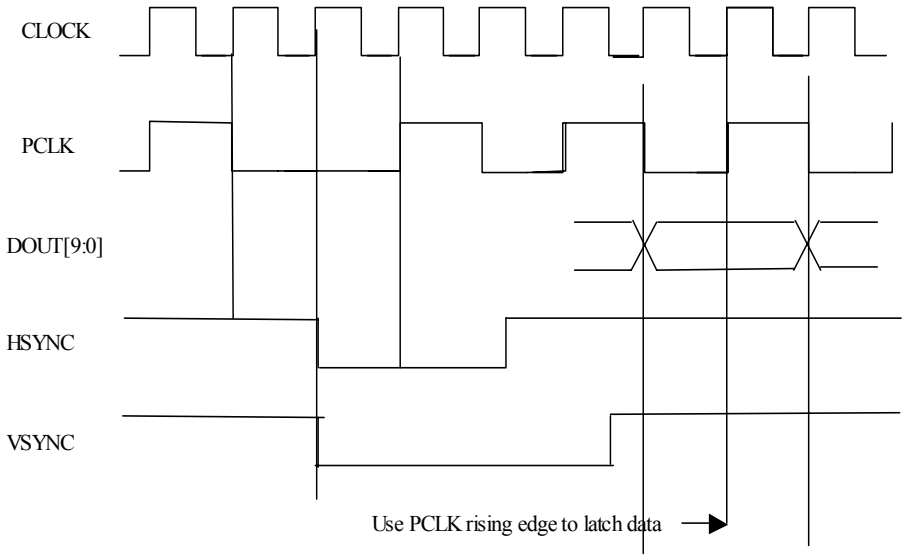
	Capacitance				
V_{IL}	Input Low Voltage			0.3 * V_{CC}	V
V_{ILS}	Schmitt Input Low Voltage		1.1		V
V_{IH}	Input High Voltage	0.7 * V_{CC}			V
V_{IHS}	Schmitt Input High Voltage		1.8		V
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V
R_L	Input Pull-up/down Resistance		50		KΩ

4.2 Sensor Array Timing

Reset Timing

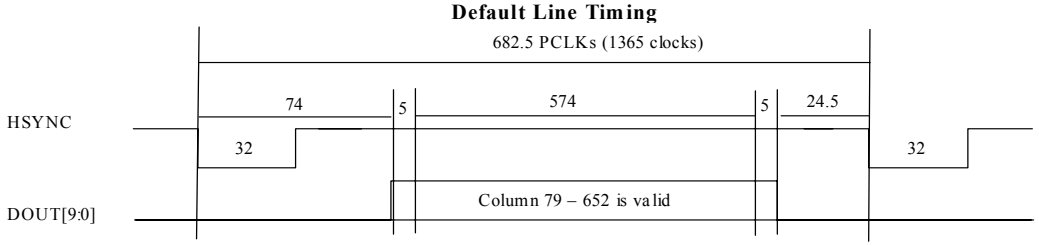


Pixel Timing

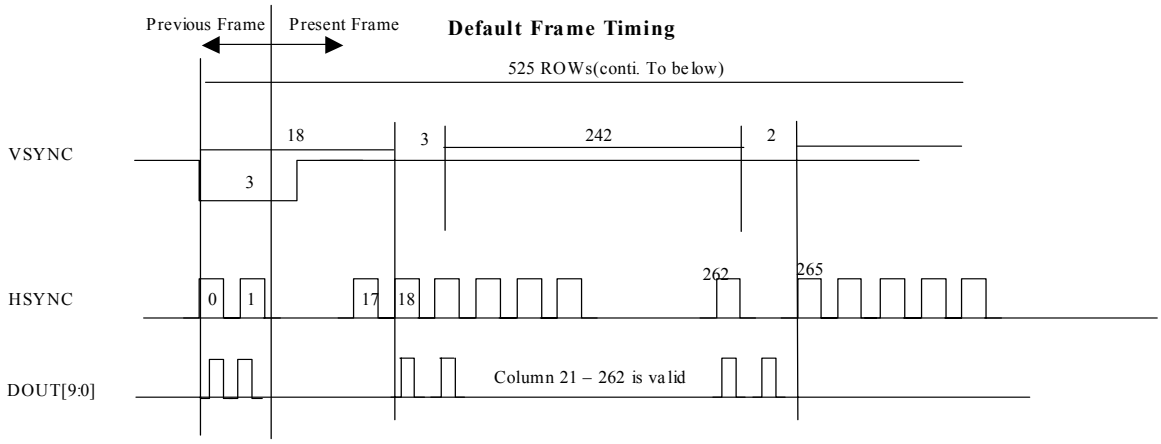


 1/17/2003

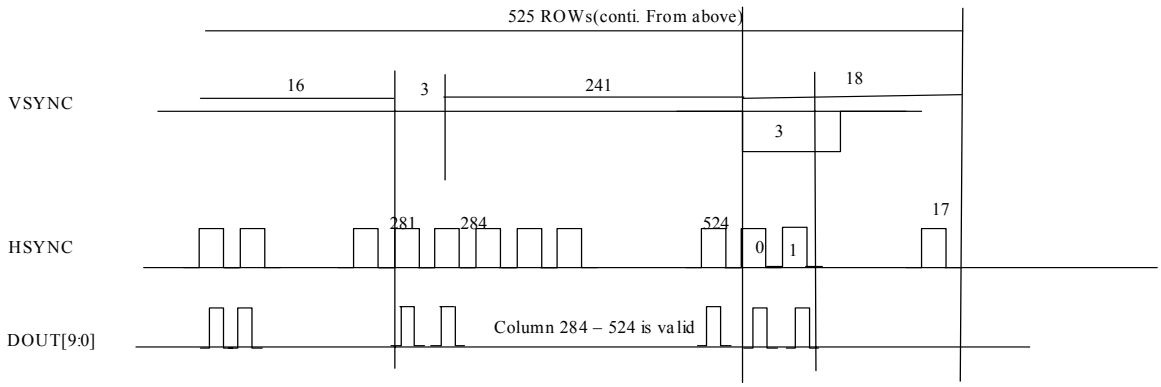
Default Line Timing



Default Frame Timing

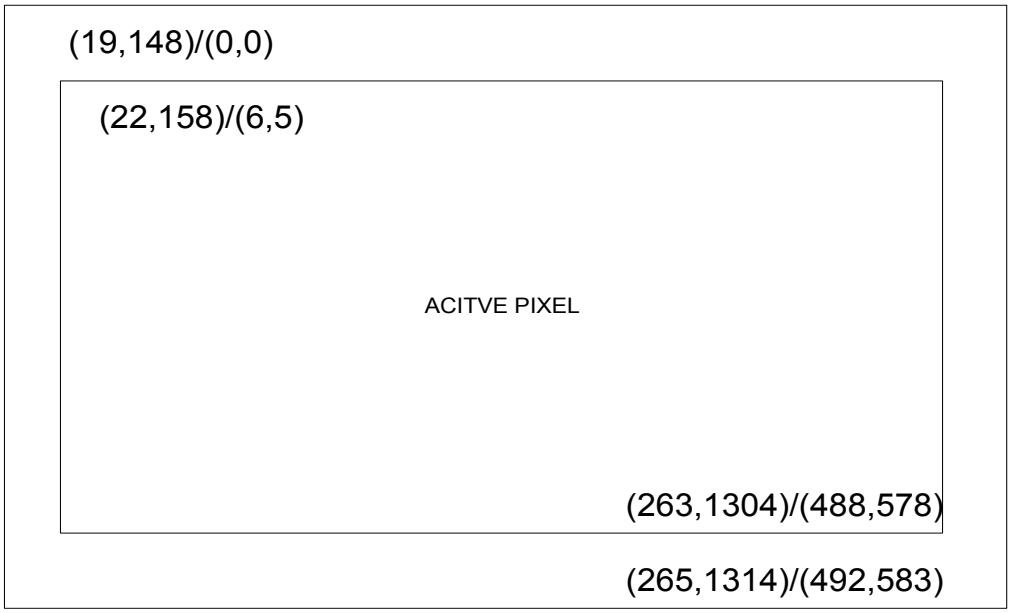


Default Frame Timing(conti. From above)

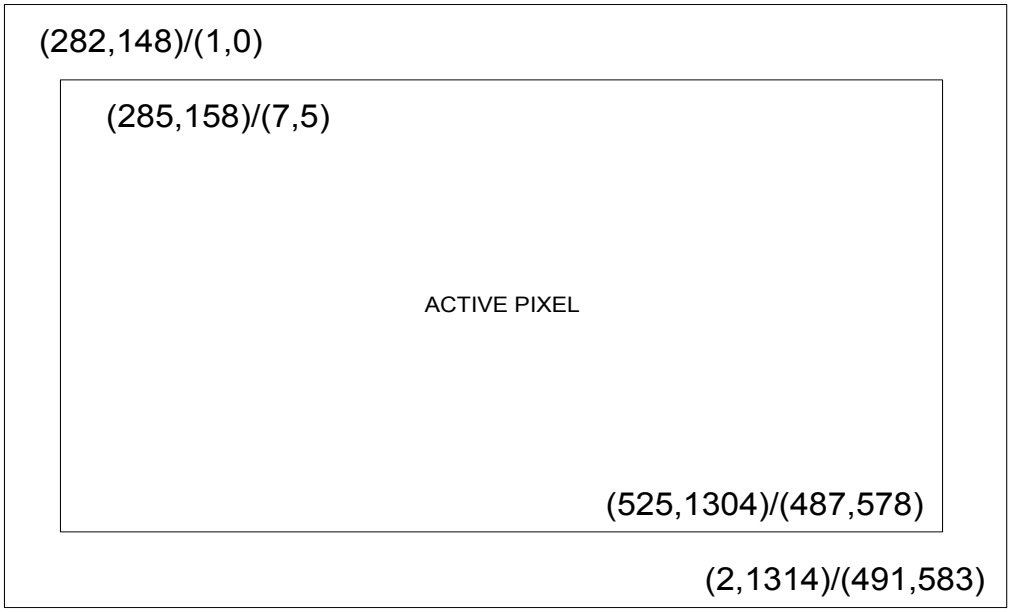


ODD Field Pixels

Legend:(line_cnt,col_cnt)/(sensor_row, sensor_column)



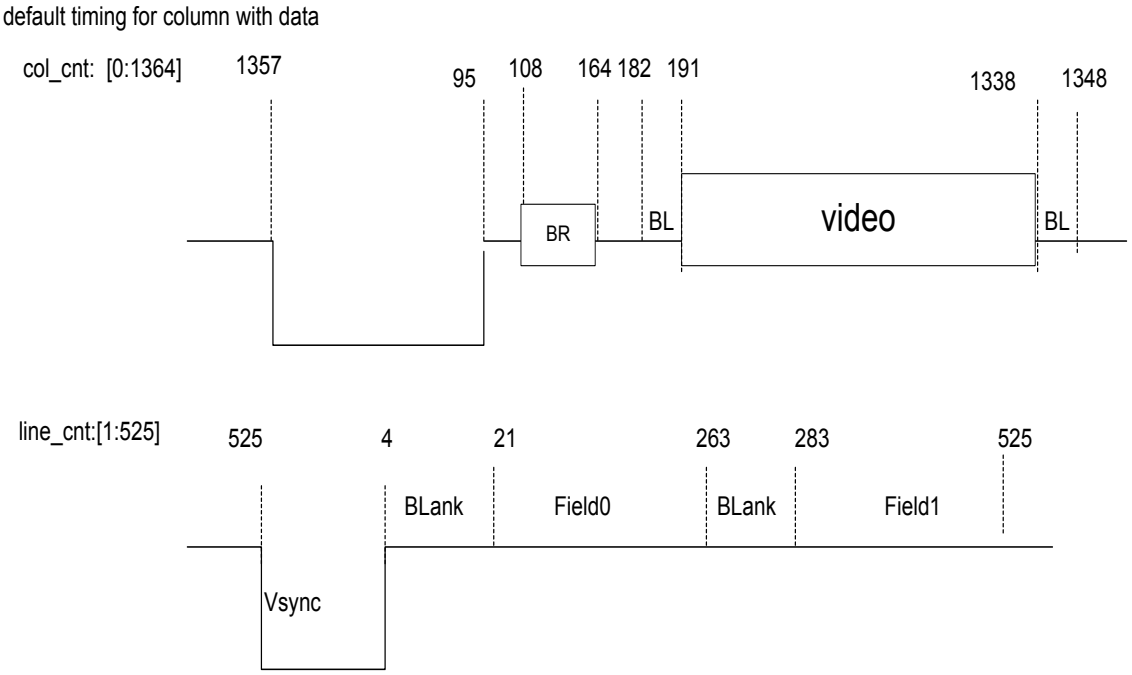
Even Field Pixels

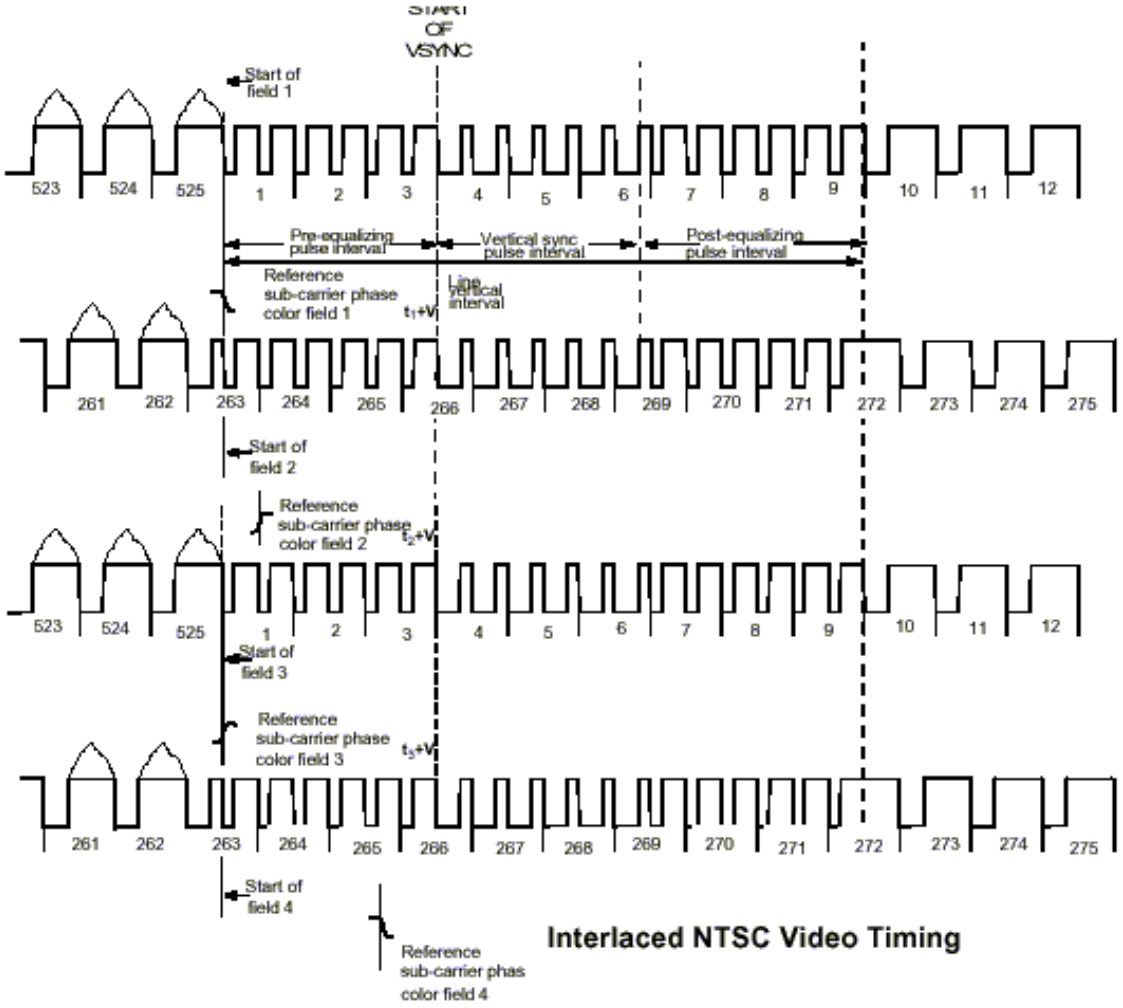


Active pixel: ODD:242X574 EVEN:241X574

4.3 TV output timing:

TV timing according to the column counter





Interlaced NTSC Video Timing

5. Mechanical Information

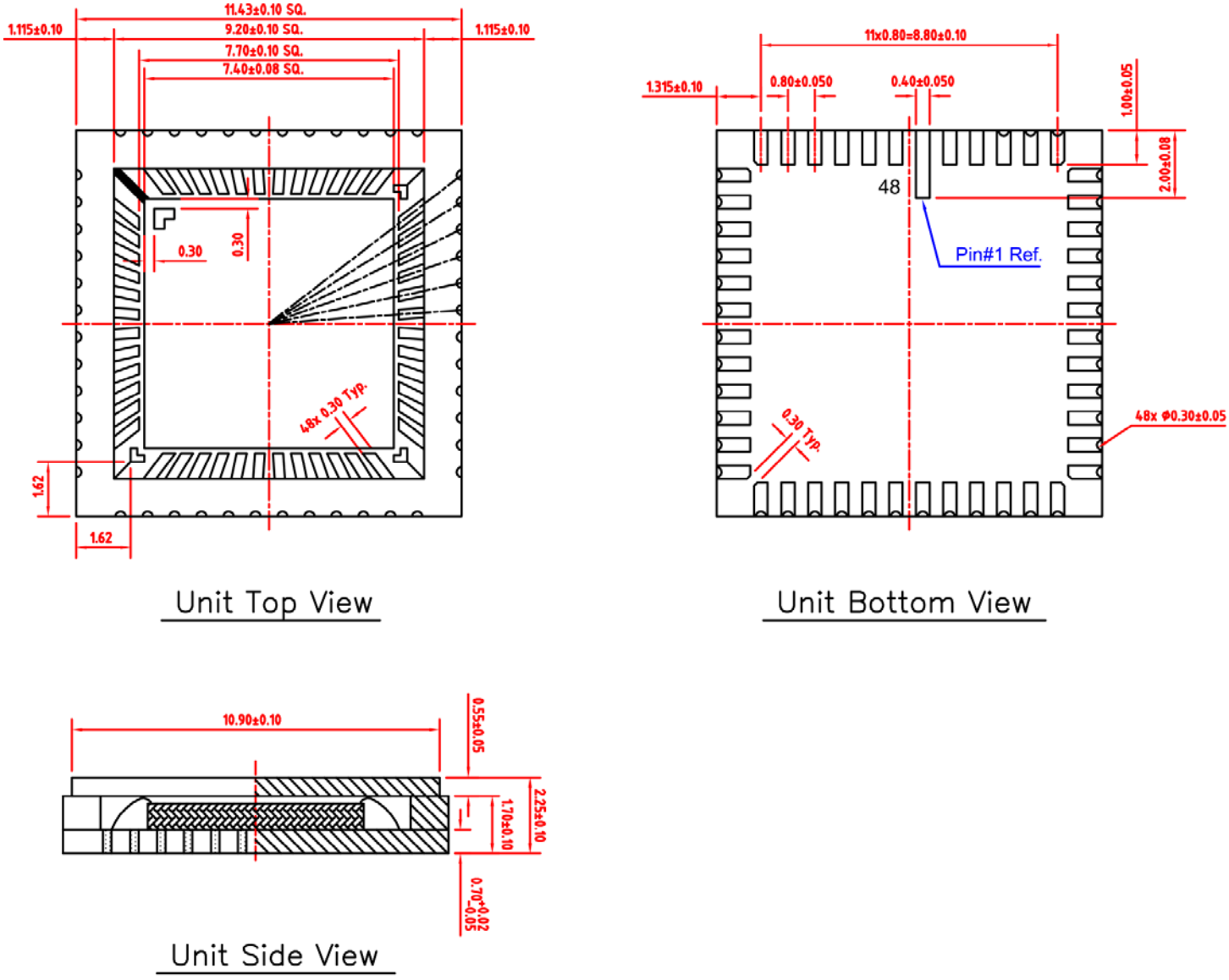


Figure 3. S Type Shrunk Plastic LCC48 Packaging

6. Ordering Information

Description	*Part Number*
Shrunk Plastic LCC48 package, VGA resolution sensor (3.3V)	ICM-515NBsa

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