

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

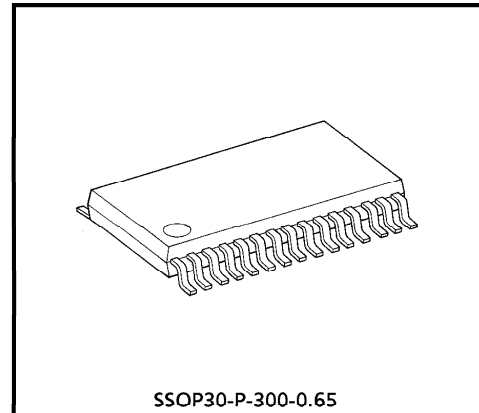
# TA8482FN

## BRIDGE DRIVER + SENSOR AMP 1-CHIP IC FOR DC MOTORS

TA8482FN is a loading motor driver for video camera. It is a 1-chip IC with tape top/end sensor amplifiers, reel FG amplifiers, and buffer amplifiers for servo error L.P.F.

### FEATURES

- 4 Modes : Forward Rotation, Reverse Rotation, Stop, and Brake
- Built-in Current Limiter
- Built-in Thermal Shutdown Circuit
- Built-in Tape Top/End Sensor Amplifiers
- 2 Built-in Reel FG Amplifiers
- 2 Built-in Buffer Amplifiers for Servo Error L.P.F.
- Built-in Buffer Limiter
- Package : VSOP-30

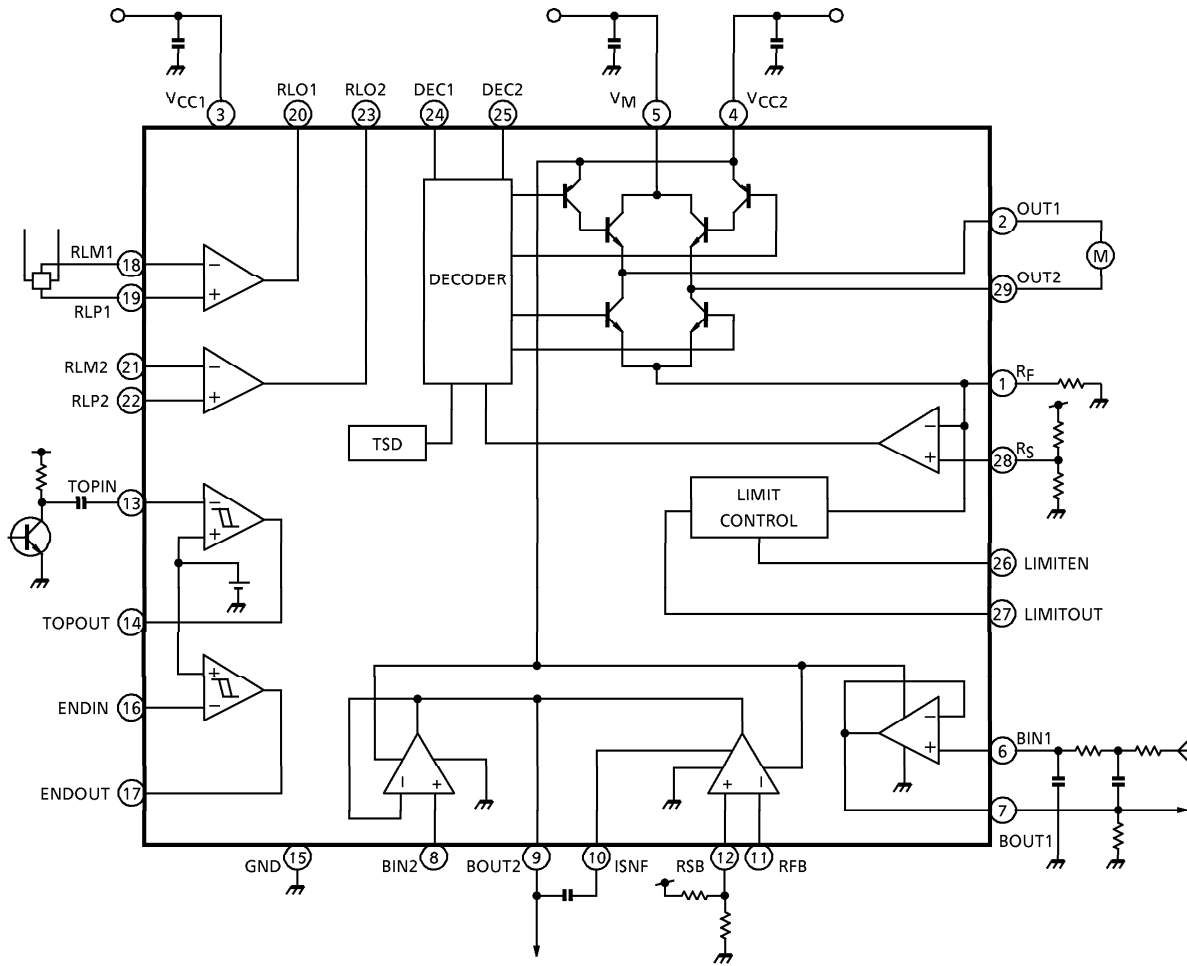


Weight : 0.17g (Typ.)

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BLOCK DIAGRAM



**PIN FUNCTION**

PIN No.	SYMBOL	PIN NAME
1	R <sub>F</sub>	Output current detect pin
2	OUT1	Motor drive output pin 1
3	V <sub>CC1</sub>	Power supply input pin 1
4	V <sub>CC2</sub>	Power supply input pin 2
5	V <sub>M</sub>	Motor drive voltage input pin
6	BIN1	Buffer amp 1 input pin
7	BOUT1	Buffer amp 1 output pin
8	BIN2	Buffer amp 2 input pin
9	BOUT2	Buffer amp 2 output pin
10	ISNF	Buffer limiter amp phase compensating pin
11	RFB	Buffer limiter amp input pin
12	RSB	Buffer limiter amp reference voltage input pin
13	TOPIN	Tape-top sensor amp input pin
14	TOPOUT	Tape-top sensor output pin
15	GND	GND pin
16	ENDIN	Tape-end sensor amp input pin
17	ENDOUT	Tape-end sensor amp output pin
18	RLM1	Reel FG amp 1 negative side input pin
19	RLP1	Reel FG amp 1 positive side input pin
20	RLO1	Reel FG amp 1 output pin
21	RLM2	Reel FG amp 2 negative side input pin
22	RLP2	Reel FG amp 2 positive side input pin
23	RLO2	Reel FG amp 2 output pin
24	DEC1	Decoder input pin 1
25	DEC2	Decoder input pin 2
26	LIMITEN	Limiter controller input pin
27	LIMITOUT	Limiter controller output pin
28	R <sub>S</sub>	Limiter amp reference voltage input pin
29	OUT2	Motor drive output pin 2
30	N.C	—

**TRUTH TABLE**  
DECODER CIRCUIT

DEC1	DEC2	OUT1	OUT2
L	L	Z	Z
H	L	H	L
L	H	L	H
H	H	L	L

Z : High impedance

LIMITER CONTROLLER CIRCUIT

LIMITEN	LIMITER AMP CIRCUIT	LIMITOUT
H	When operated (when output current is detected)	L
	When not operated	H
L	H	

**MAXIMUM RATINGS** (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Small Signal Section Supply Voltage	V <sub>CC1</sub>	10	V
Output Section Supply Voltage	V <sub>CC2</sub>	11	V
Output Section Supply Voltage	V <sub>M</sub>	8	V
Output Current	I <sub>O</sub>	0.6	A
Power Dissipation	P <sub>D</sub>	0.86 (Note 1)	W
		1.13 (Note 2)	
Operating Temperature	T <sub>opr</sub>	- 20~80	°C
Storage Temperature	T <sub>stg</sub>	- 55~150	°C

(Note 1) Single body

(Note 2) Substrate mounting (50×50×1.6mm Cu 40%)

(\*) Devices may break outside the range of maximum rating.

**OPERATING SUPPLY VOLTAGE RANGE** (Ta = 25°C)

CHARACTERISTIC	SYMBOL	OPERATING RANGE	UNIT
Small Signal Section Supply Voltage	V <sub>CC1</sub>	2.7~4.0	V
Output Section Supply Voltage	V <sub>CC2</sub>	V <sub>CC1</sub> ~9.0	V
Output Section Supply Voltage	V <sub>M</sub>	1.0~7.0 (Note 3)	V

(Note 3) V<sub>CC2</sub> ≥ V<sub>M</sub>

(\*) The range of operating conditions covers normal operations under the condition specified for electrical characteristics.

ELECTRICAL CHARACTERISTICS (V<sub>CC1</sub> = 3.0V, V<sub>CC2</sub> = 4.75V, V<sub>M</sub> = 3.0V, Ta = 25°C)

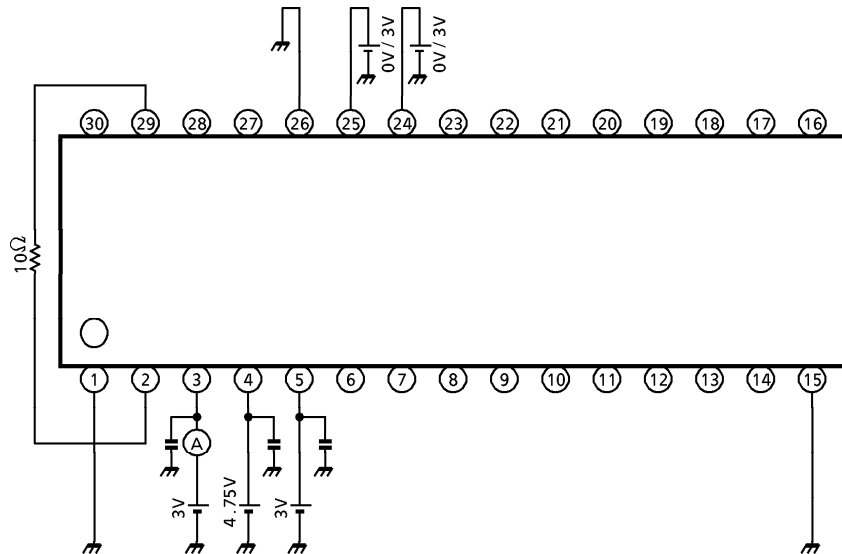
CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT			
Supply Current			I <sub>CC11</sub>	1	R <sub>L</sub> = 10Ω DEC1 : L, DEC2 : L	—	3	4.2	mA			
			I <sub>CC12</sub>		R <sub>L</sub> = 10Ω DEC1 : H/L, DEC2 : L/H	—	20	30				
			I <sub>CC13</sub>		R <sub>L</sub> = 10Ω DEC1 : H, DEC2 : H	—	42	60				
						I <sub>CC21</sub>	2	R <sub>L</sub> = 10Ω, V <sub>CC1</sub> = 0V DEC1 : L, DEC2 : L	—	—	1	μA
						I <sub>CC22</sub>		R <sub>L</sub> = 10Ω DEC1 : L, DEC2 : L	—	0.7	1	mA
						I <sub>CC23</sub>		R <sub>L</sub> = 10Ω DEC1 : H/L, DEC2 : L/H	—	20	30	
						I <sub>CC24</sub>		R <sub>L</sub> = 10Ω DEC1 : H, DEC2 : H	—	0.7	1	
			I <sub>M</sub>	3	R <sub>L</sub> = 10Ω DEC1 : L, DEC2 : L	—	—	1	μA			
Decoder Circuit	Input Voltage	"H" level	V <sub>IN1</sub>	4	R <sub>L</sub> = 10Ω	2.0	—	—	V			
		"L" level	V <sub>IN2</sub>		R <sub>L</sub> = 10Ω	—	—	0.6				
	Input Current		I <sub>IN</sub>		V <sub>IN</sub> = 3.0V	—	—	3	μA			
	Input Leakage Current		I <sub>INL</sub>		V <sub>IN</sub> = 0V	—	—	1				
Output Circuit	Saturation Voltage (Upper Side + Lower side)		V <sub>sat</sub> (H + L)	5	I <sub>O</sub> = 0.2A	—	0.3	0.45	V			
					I <sub>O</sub> = 0.4A	—	0.6	0.75				
Current Limiter Amp	Reference Voltage Input Range		V <sub>RS</sub>	6		0.05	—	1.0	V			
	Detecting Voltage		V <sub>LIMIT</sub>	7	R <sub>L</sub> = 10Ω, R <sub>F</sub> = 1Ω V <sub>RS</sub> = 0.2V	0.18	0.2	0.22				
Current Limiter Controller	Input Voltage	"H" level	V <sub>LE</sub> (H)	8	R <sub>L</sub> = 10Ω	2.0	—	—	V			
		"L" level	V <sub>LE</sub> (L)		R <sub>L</sub> = 10Ω	—	—	0.6				
	Input Current		I <sub>LC</sub>		V <sub>LE</sub> = 3.0V	—	—	3	μA			
	Input Leakage Current		I <sub>LCL</sub>		V <sub>LE</sub> = 0V	—	—	1				
	Output Voltage	"H" level	V <sub>LO</sub> (H)		I <sub>O</sub> = 10μA	V <sub>CC1</sub> - 0.5	—	—	V			
		"L" level	V <sub>LO</sub> (L)		I <sub>O</sub> = 10μA	—	—	0.4				

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reel FG Amp	Common-Phase Voltage Range	V <sub>CMRFG</sub>	9		1.0	—	2.0	V
	Input Current	I <sub>FG</sub>	10	V <sub>CMRFG</sub> = 1.5V	—	—	1	μA
	Output Offset Voltage	V <sub>OFFG</sub>			—	0	±290	mV
	Closed Loop Voltage Gain	G <sub>VFG</sub>	11	f <sub>FG</sub> = 1kHz	27	29	31	dB
	Open Loop Voltage Gain	G <sub>VOFG</sub>	—	f <sub>FG</sub> = 1kHz Design assurance	—	55	—	dB
	Output Residual Voltage	V <sub>sat-FG (H)</sub>	12	I <sub>O</sub> = 10μA (Upper side)	—	—	0.2	V
V <sub>sat-FG (L)</sub>		I <sub>O</sub> = 10μA (Lower side)		—	—	0.2		
Top / End Sensor Amp	Input Resistance	R <sub>IN</sub>	13		4	5	6	kΩ
	Minimum Input Sensitivity	V <sub>HS</sub>	—	Design assurance	30	40	50	mV <sub>p-p</sub>
Buffer Amp	Input Voltage Range	V <sub>CMRB</sub>	14		0	—	V <sub>CC2</sub>	V
	Input Current	I <sub>B</sub>		V <sub>BIN</sub> = 0V, (Note)	—	—	1	μA
	Input Offset Voltage	V <sub>OFB</sub>		V <sub>BIN</sub> = 1.5V	—	0	±7	mV
	Output Voltage (Upper Side)	V <sub>OB (H)</sub>	15	R <sub>L</sub> = 20kΩ (against GND)	V <sub>CC2</sub> - 1.7	—	—	V
	Output Voltage (Lower Side)	V <sub>OB (L)</sub>		V <sub>BOUT</sub> = 0V, R <sub>L</sub> = 500kΩ (against V <sub>CC2</sub> )	—	—	0.1	V
	Band Width	f <sub>B</sub>	—	Design assurance	—	800	—	kHz
Buffer Limiter Amp	Common-Phase Input Voltage Range	V <sub>CMRBL</sub>	16		0	—	V <sub>CC2</sub> - 1.7	V
	Input Current	I <sub>BL</sub>	17	V <sub>BL</sub> = 0V	—	—	1	μA
	Input Offset Voltage	V <sub>OFBL</sub>	18	V <sub>RSB</sub> = 1.5V	—	0	±7	mV
Thermal Shutdown Circuit Operating Temperature		T <sub>SD</sub>	—	Design assurance	—	150	—	°C

(Note) Design target value is fixed at 0.5μA (Max.)

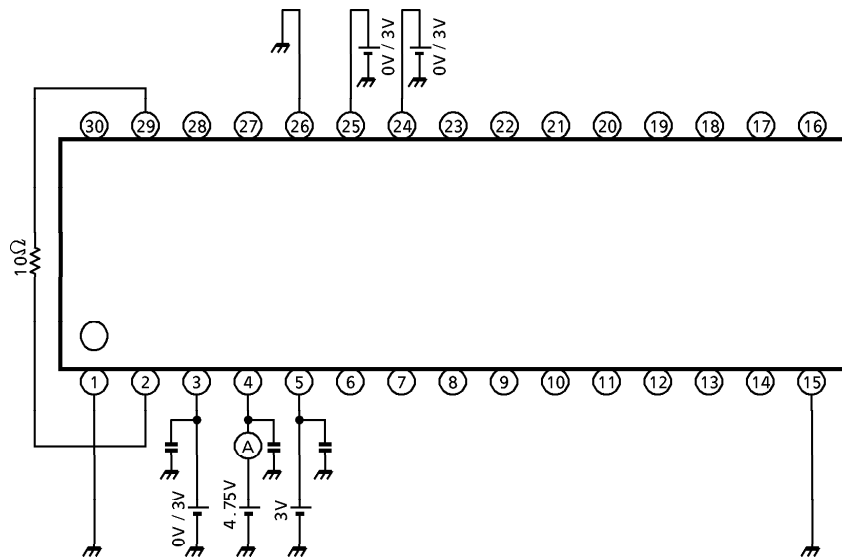
TEST CIRCUIT

1. I<sub>CC1</sub>, I<sub>CC2</sub>, I<sub>CC3</sub>



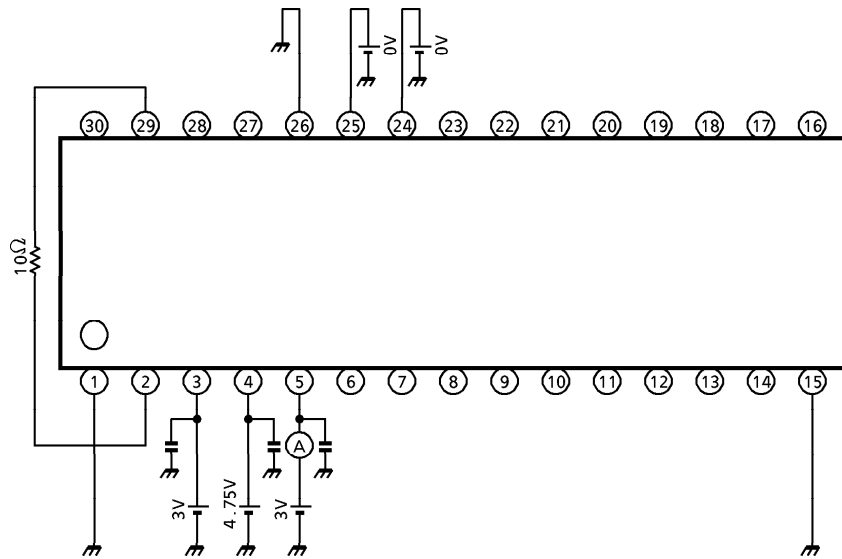
- I<sub>CC1</sub>  
DEC1 = L, DEC2 = L
- I<sub>CC2</sub>  
DEC1 = H, DEC2 = L  
and  
DEC1 = L, DEC2 = H
- I<sub>CC3</sub>  
DEC1 = H, DEC2 = H

2. I<sub>CC21</sub>, I<sub>CC22</sub>, I<sub>CC23</sub>, I<sub>CC24</sub>



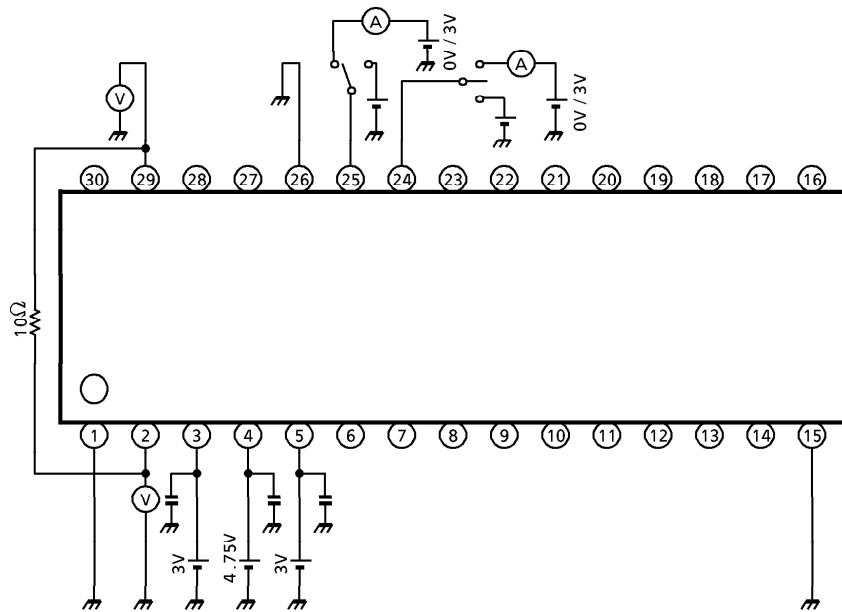
- I<sub>CC21</sub>  
V<sub>CC1</sub> = 0V, DEC1 = L, DEC2 = L
- I<sub>CC22</sub>  
V<sub>CC1</sub> = 3V, DEC1 = L, DEC2 = L
- I<sub>CC23</sub>  
DEC1 = H, DEC2 = L  
and  
DEC1 = L, DEC2 = H
- I<sub>CC24</sub>  
DEC1 = H, DEC2 = H

3.  $I_M$



- $I_M$   
DEC1 = L, DEC2 = L

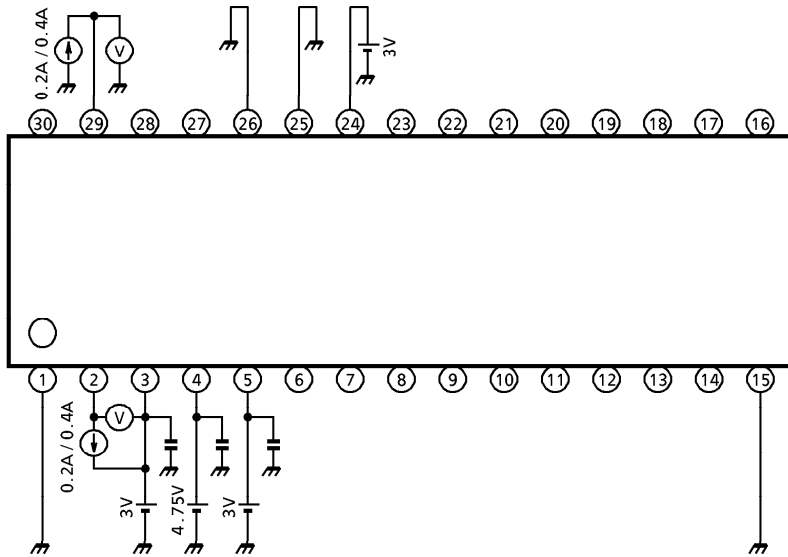
4.  $V_{IN1}$ ,  $V_{IN2}$ ,  $I_{IN1}$ ,  $I_{INL}$



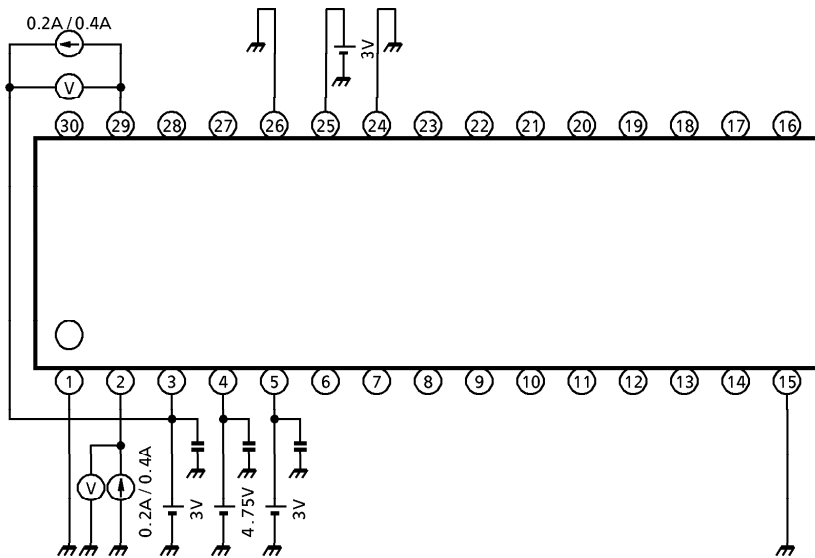
- $V_{IN1}$ ,  $V_{IN2}$   
 $V_{DEC1} = 0.6V$ ,  $V_{DEC2} = 2.0V$   
 $V_{DEC1} = 2.0V$ ,  $V_{DEC2} = 0.6V$   
 $V_{DEC1} = 2.0V$ ,  $V_{DEC2} = 2.0V$   
 Check the output functions on the above-mentioned three conditions.
- $I_{IN1}$   
 $V_{IN} = 3.0V$
- $I_{INL}$   
 $V_{IN} = 0V$



5.  $V_{sat} (H + L)$



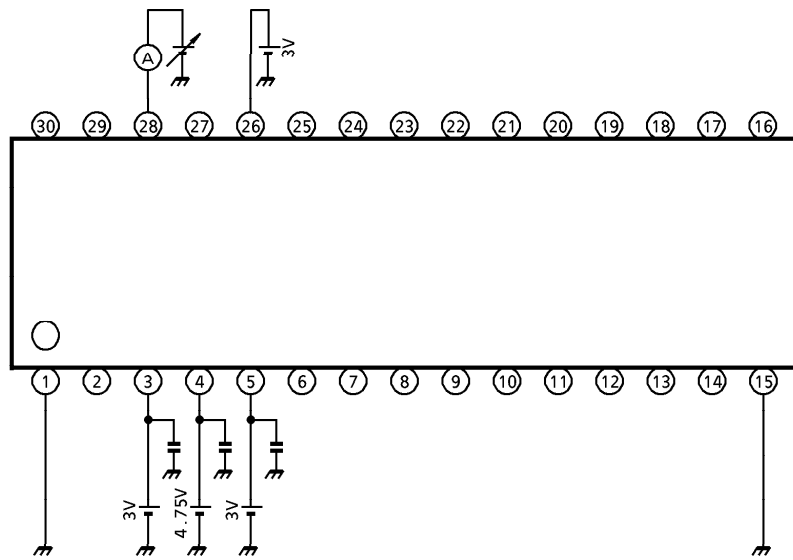
- $V_{sat} (H + L)$   
Input DEC1 = H, DEC2 = L, and measure OUT1 (upper side) and OUT2 (lower side) with regard to  $I_O = 0.2A / 0.4A$ .



- $V_{sat} (H + L)$   
Input DEC1 = H, DEC2 = L, and measure OUT1 (upper side) and OUT2 (lower side) with regard to  $I_O = 0.2A / 0.4A$ .

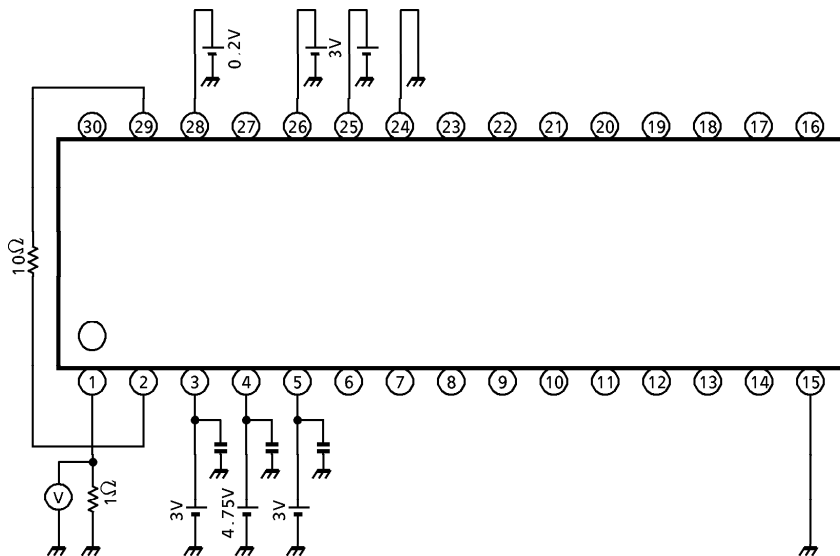
The sum of the upper / lower values of OUT1 and OUT2 is fixed at  $V_{sat} (H + L)$ .

6.  $V_{RS}$



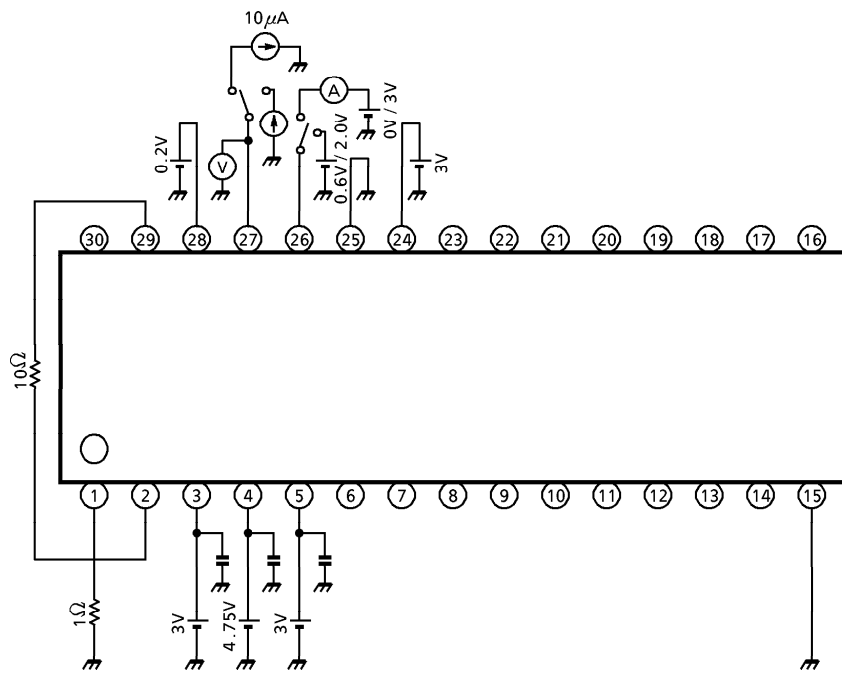
- $V_{RS}$   
Change  $V_{RS}$  and measure input current.

7.  $V_{LIMIT}$



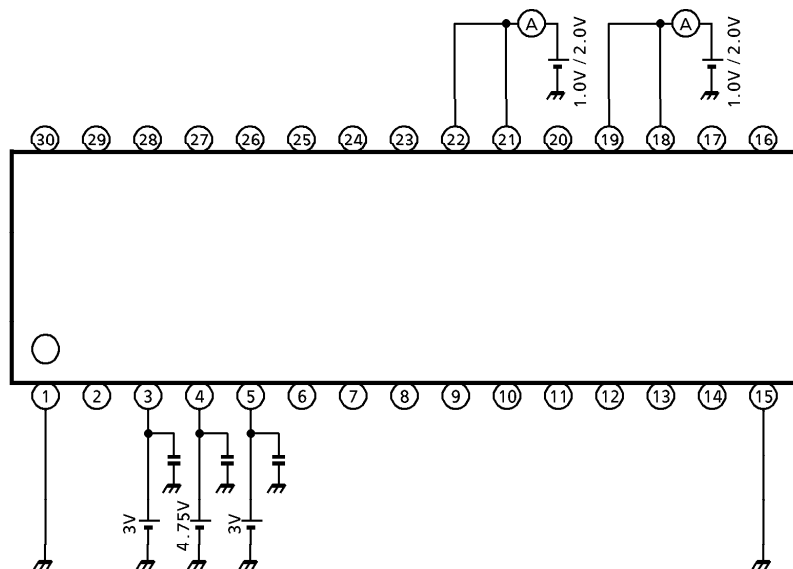
- $V_{LIMIT}$   
Input  $V_{RS} = 0.2V$  and measure  $R_F (= 1\Omega)$  generating voltage at the time of limiter amp operation.

8.  $V_{LE}(H)$ ,  $V_{LE}(L)$ ,  $I_{LC}$ ,  $I_{LCL}$ ,  $V_{LO}(H)$ ,  $V_{LO}(L)$

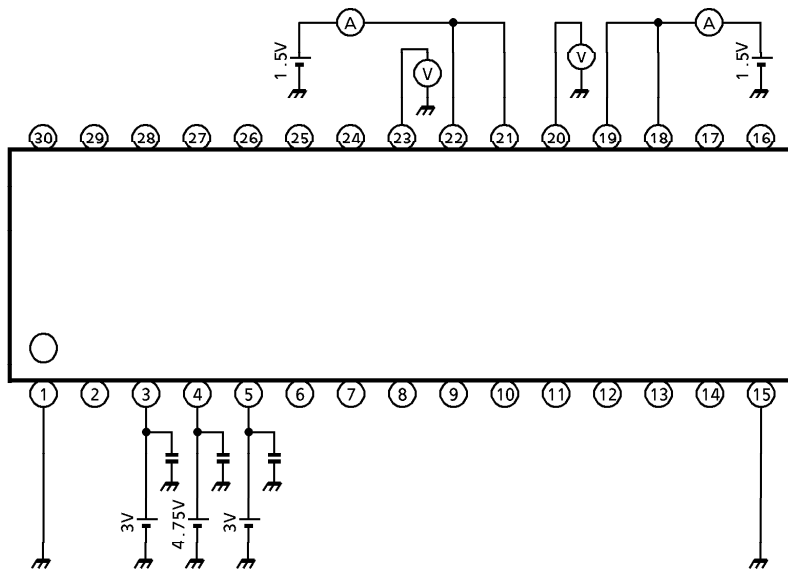


- $V_{LE}(H)$ ,  $V_{LE}(L)$   
Input  $V_{LE} = 2.0V / 0.6V$  in a limiter amp operating state and check the LIMIT OUT terminal voltage.
- $I_{LC}$   
 $V_{LE} = 3.0V$
- $I_{LCL}$   
 $V_{LE} = 0V$
- $V_{LO}(H)$ ,  $V_{LO}(L)$   
Input  $V_{LE} = 0.6V / 2.0V$  in a limiter amp operating state and measure the LIMIT OUT terminal voltage when  $I_O = 10\mu A$ .

9.  $V_{CMRFG}$



10. I<sub>FG</sub>, V<sub>OFFG</sub>



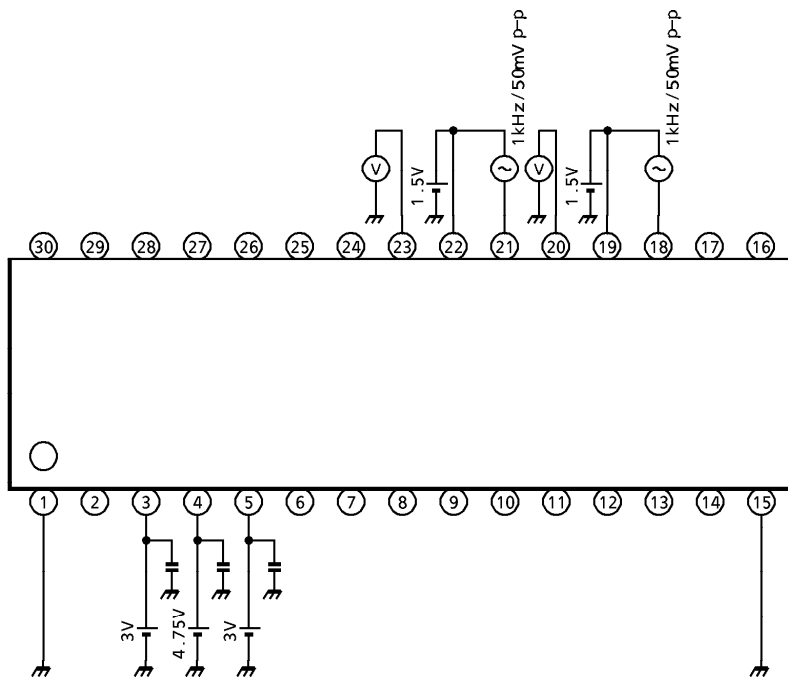
- I<sub>FG</sub>  
Measure the input current (I<sub>FG'</sub>) when V<sub>CMRFG</sub> = 1.5V, and calculate the following formula :

$$I_{FG} = \frac{1}{2} \times I_{FG'}$$

- V<sub>OFFG</sub>  
Measure the R<sub>LO</sub> pin output voltage when V<sub>CMRFG</sub> = 1.5V, and calculate the following formula :

$$V_{OFFG} = V_{RLO} - 1.5$$

11. GV<sub>FG</sub>

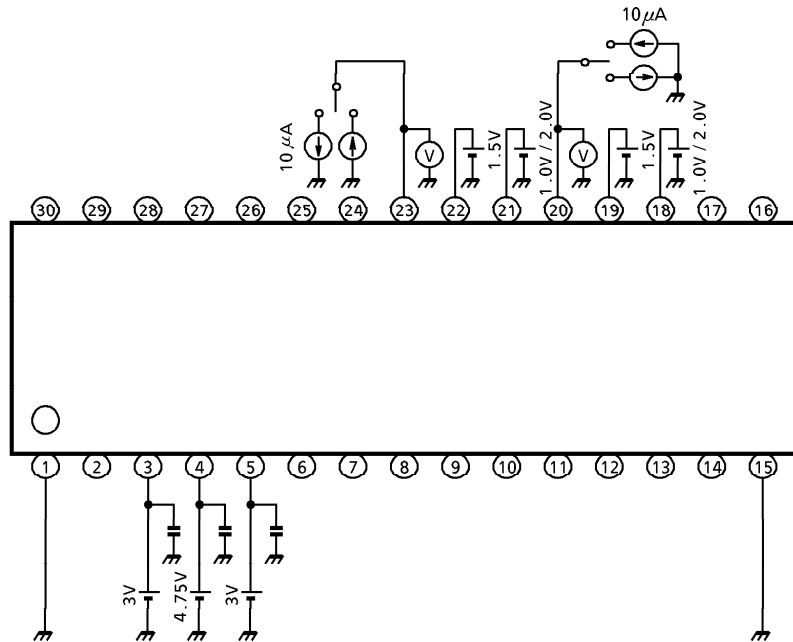


- GV<sub>FG</sub>  
V<sub>RLP</sub> = 1.5V, input signals

f<sub>FG</sub> = 1kHz, V<sub>FG</sub> = 50mV<sub>p-p</sub> between R<sub>LP</sub> and R<sub>LM</sub>, and measure V<sub>RLO</sub> in this case.

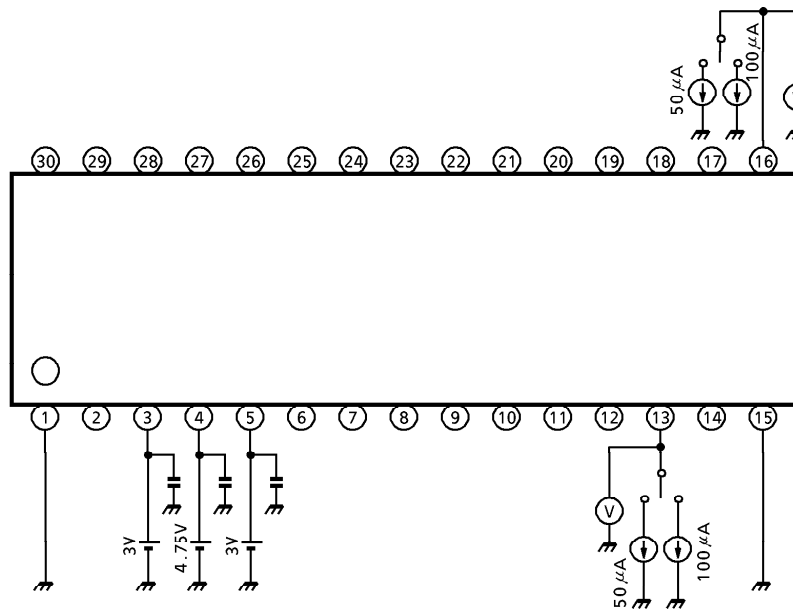
$$GV_{FG} = 20 \log \frac{V_{RLO}}{0.05} \text{ [dB]}$$

12.  $V_{sat-FG} (H)$ ,  $V_{sat-FG} (L)$



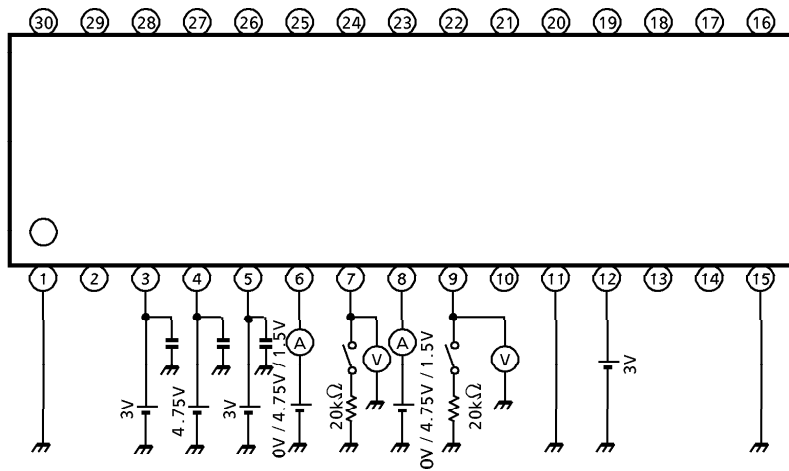
- $V_{sat-FG} (H)$   
Input  $V_{RLP} = 1.5V$ ,  
 $V_{RLM} = 1.0V$ , measure the  
 $R_{LO}$  pin voltage when  
 $I_O = 10\mu A$  (source current),  
and calculate the following  
formula :  
$$V_{sat-FG} (H) = 3.0 - V_{RLO} [V]$$
- $V_{sat-FG} (L)$   
Input  $V_{RLP} = 1.5V$ ,  
 $V_{RLM} = 2.0V$  and measure the  
 $R_{LO}$  pin voltage when  
 $I_O = 10\mu A$  (sink current).

13.  $R_{IN}$



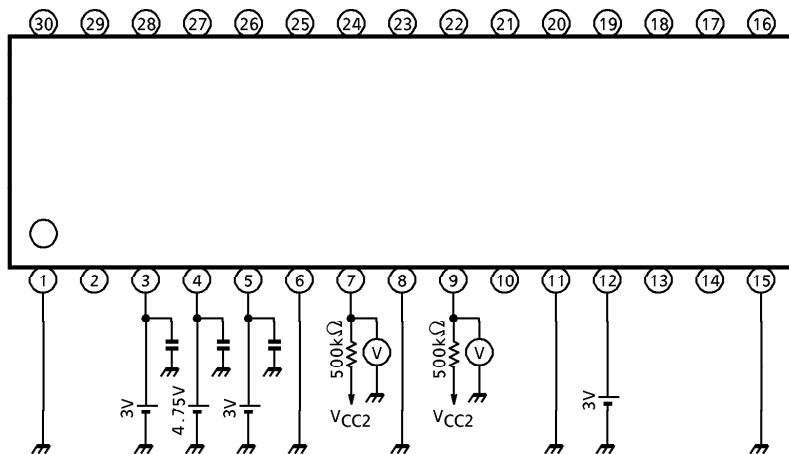
- $R_{IN}$   
Measure the  $V_{TOPIN}$ ,  $V_{ENDIN}$   
at the time  $50\mu A / 100\mu A$   
current flows from  $TOPIN /$   
 $ENDIN$  pin, and calculate the  
following formula :  
$$R_{IN} = \frac{V (50\mu A) - V (100\mu A) - 0.007}{50\mu A} [\Omega]$$
- \* The 7mV in the formula  
represents the  $V_{BE}$  change of  
the internal  $T_r$ . at the time  
of  $50\mu A / 100\mu A$ .

14.  $V_{CMRB}$ ,  $I_B$ ,  $V_{OB} (H)$

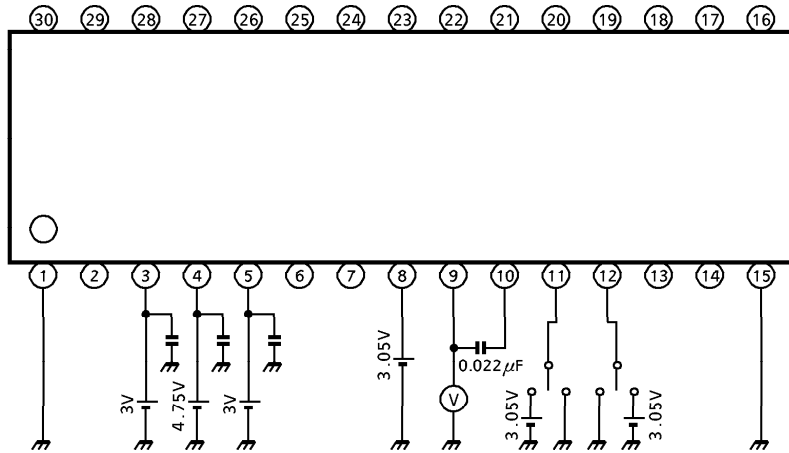


- $V_{CMRB}$   
Input  $V_{BIN} = 0V / 4.75V$  and measure BOUT pin voltage.
- $I_B$   
 $V_{BIN} = 1.5V$
- $V_{OB} (H)$   
Input  $V_{BIN} = 4.75V$  and connect  $20k\Omega$  (against GND) to BOUT pin.

15.  $V_{OB} (L)$

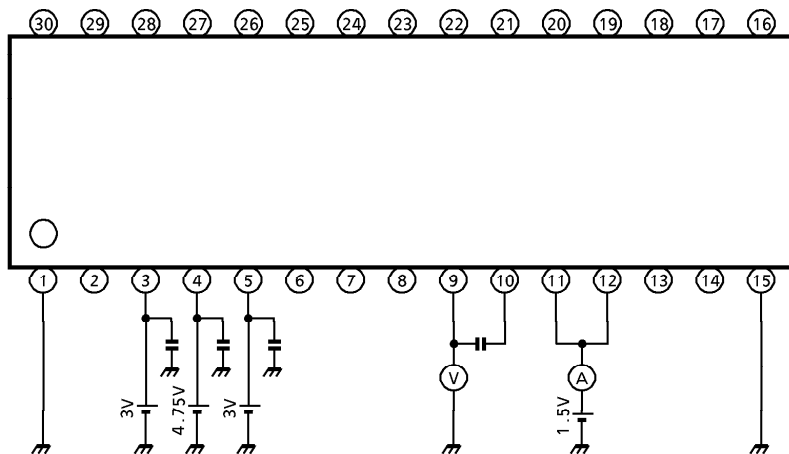


16.  $V_{CMRBL}$

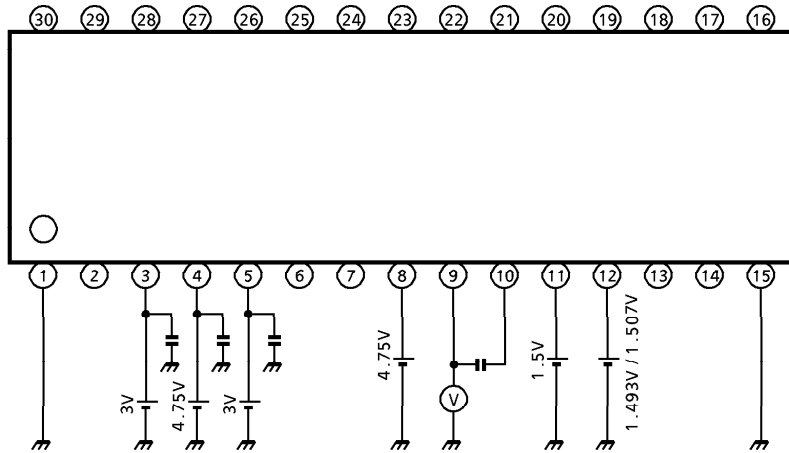


- $V_{CMRBL}$   
 Check BOUT2 pin : L when  $V_{RFB} = 3.05V, V_{RSB} = 0V$ .  
 Check BOUT2 pin : L when  $V_{RFB} = 0V, V_{RSB} = 3.05$ .

17.  $I_{BL}$



18. V<sub>OFBL</sub>

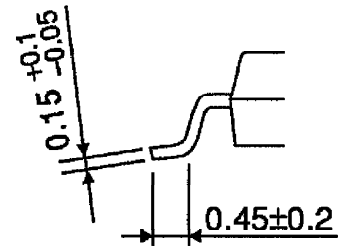
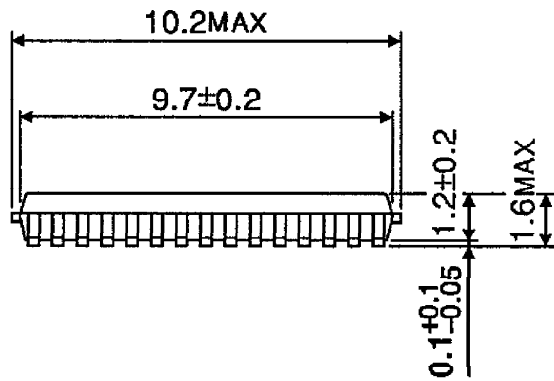
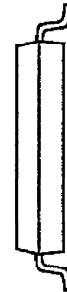
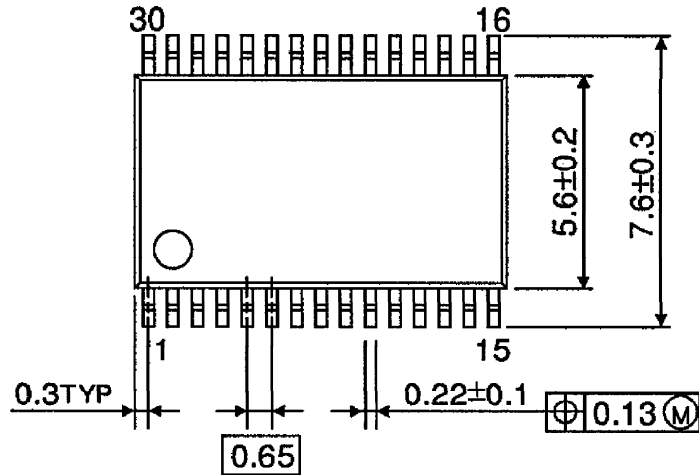


- V<sub>OFBL</sub>  
 Input V<sub>RSB</sub> = 1.5V,  
 V<sub>RFB</sub> = 1.5V ± 7mV, and check  
 the switching of BOUT2 pin  
 output function.  
 BOUT2 : H when  
 V<sub>RFB</sub> = 1.493V.  
 BOUT2 : L when  
 V<sub>RFB</sub> = 1.507V.



OUTLINE DRAWING  
SSOP30-P-300-0.65

Unit : mm



Weight : 0.17g (Typ.)