STL80N4LLF3

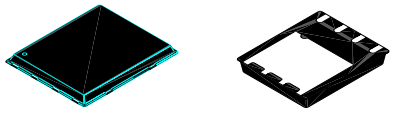
N-channel 40V - 0.0042Ω - 80A - PowerFLAT™ (6x5) STripFET™ Power MOSFET for DC-DC conversion

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STL80N4LLF3	40V	<0.005Ω	20A (1)

1. When mounted on FR-4 board of 1 inch², 2oz Cu, t<10 sec

- Improved die-to-footprint ratio
- Very low profile package (1mm Max)
- Very low thermal resistance
- Conduction losses reduced
- Switching losses reduced

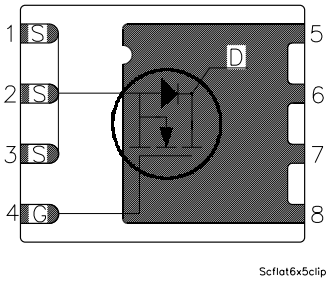


PowerFLAT™(6x5)

Description

This series of product utilizes the latest advanced design rules of ST's proprietary STripFET™ Technology. The resulting Transistor is optimized for low on-Resistance and minimal gate charge. The chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STL80N4LLF3	L80N4LLF3	PowerFLAT™ (6x5)	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	40	V
V_{GS}	Gate- source voltage	±16	V
V_{GS} (1)	Gate- source voltage	±18	V
I_D (2)	Drain current (continuous) at T_C = 25°C	80	A
I_D (2)	Drain current (continuous) at T_C = 100°C	50	A
I_D (3)	Drain current (continuous) at T_C = 25°C	20	A
I_{DM} (4)	Drain current (pulsed)	80	A
P_{TOT} (2)	Total dissipation at T_C = 25°C	80	W
P_{TOT} (3)	Total dissipation at T_C = 25°C	4	W
	Derating factor (3)	0.03	W/°C
T_{stg} T_j	Storage temperature Operating junction temperature	-55 to 150	°C

1. Guaranteed for test time ≤ 15ms
2. The value is rated according Rthj-c
3. When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec
4. Pulse width limited by safe operating area

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-c	Thermal resistance junction-case max	1.56	°C/W
Rthj-pcb (1)	Thermal operating junction-pcb max	31.2	°C/W

1. When mounted on FR-4 board of 1 inch², 2oz Cu, t<10 sec

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	40			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating@125 °C				10 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 10 A V_{GS} = 4.5V, I_D =10 A		0.0042 0.005	0.005 0.007	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2530 574 29		pF pF pF
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20mV open drain	1	3	5	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 32V, I_D = 20 A, V_{GS} = 4.5V *(see Figure 13)*		21.5 6.9 8.2	28	nC nC nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_r	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 20V, I_D = 10A, R_G= 4.7Ω V_{GS} = 10V *(see Figure 15)*		17 25 62 9		ns ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				20 80	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 20 A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 20A,V_{DD} = 20V di/dt = 100A/µs T_j = 150°C*(see Figure 14)*		43 64 3		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

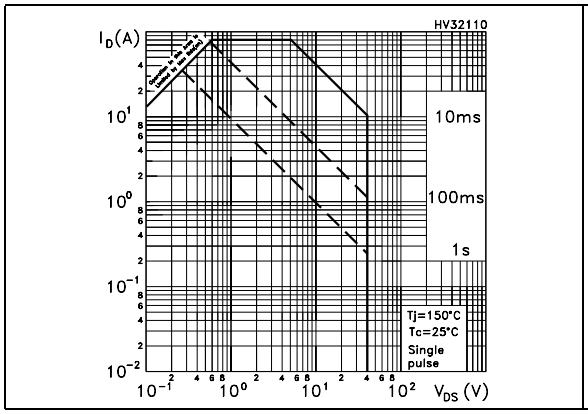


Figure 2. Thermal impedance

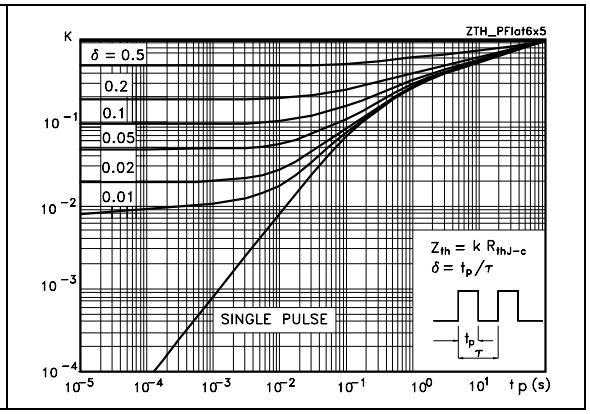


Figure 3. Output characterisics

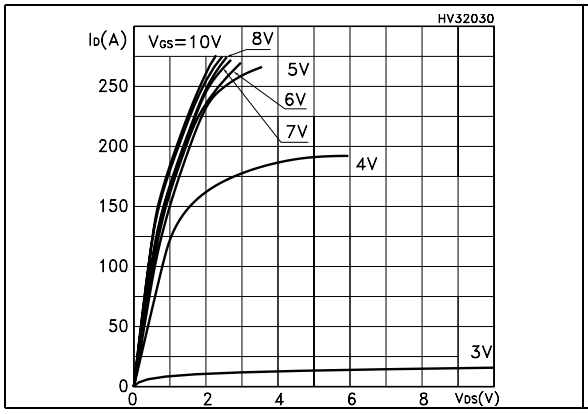


Figure 4. Transfer characteristics

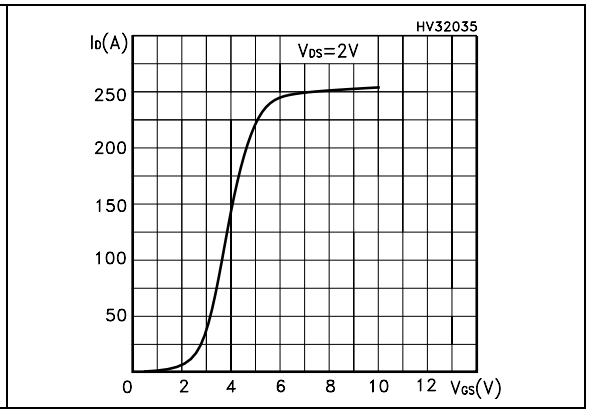


Figure 5. Normalized B_{VDSS} vs temperature

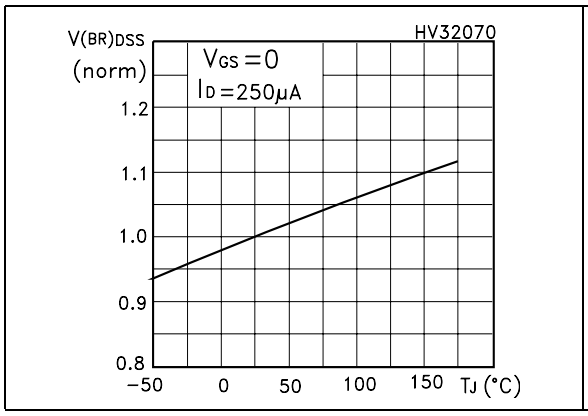


Figure 6. Static drain-source on resistance

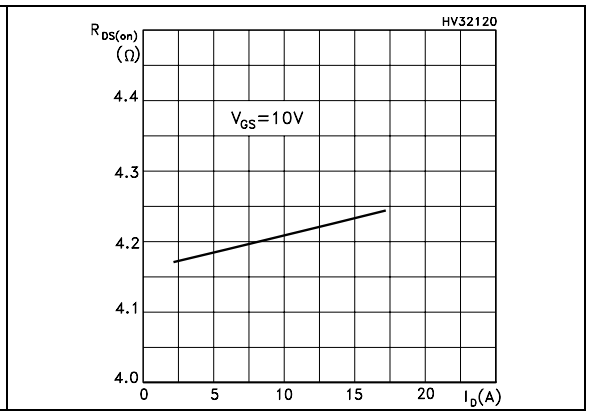


Figure 7. Gate charge vs gate-source voltage

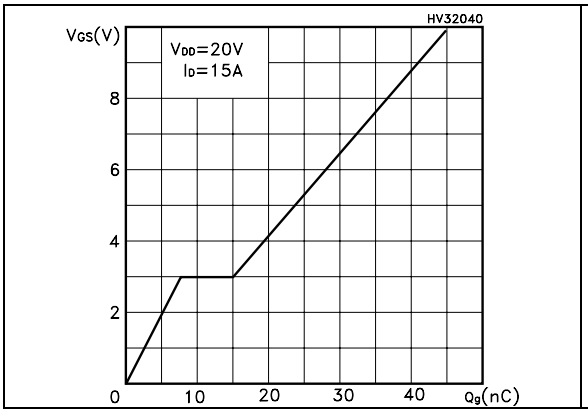


Figure 8. Capacitance variations

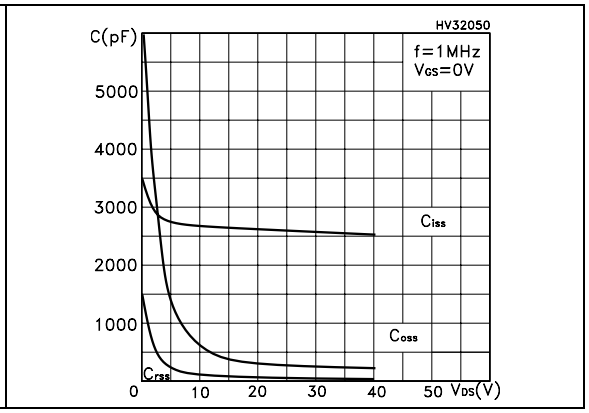


Figure 9. Normalized gate threshold voltage vs temperature

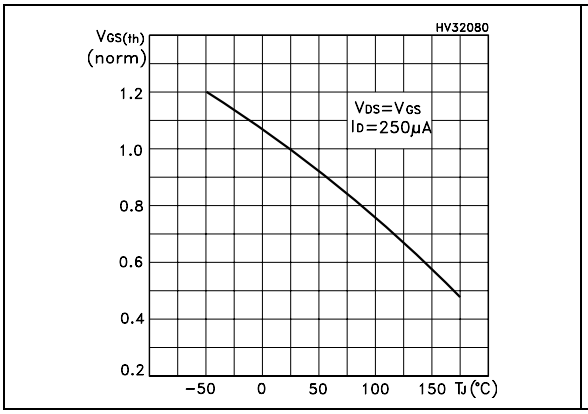


Figure 10. Normalized on resistance vs temperature

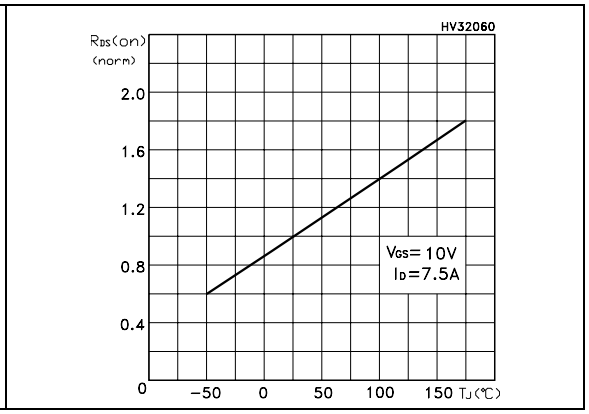
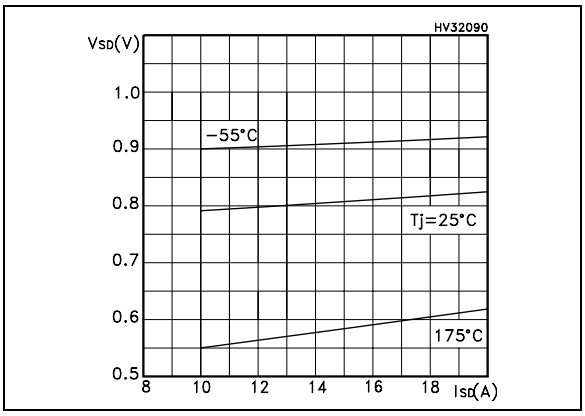


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

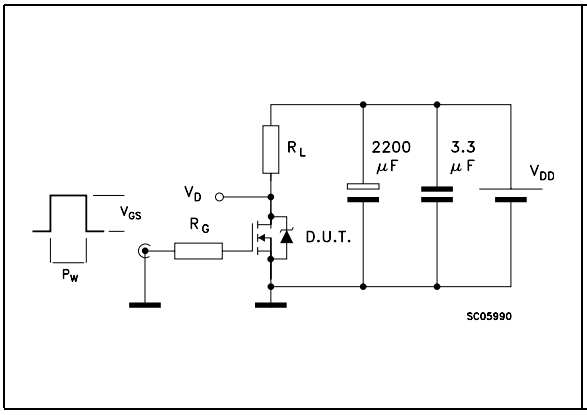


Figure 13. Gate charge test circuit

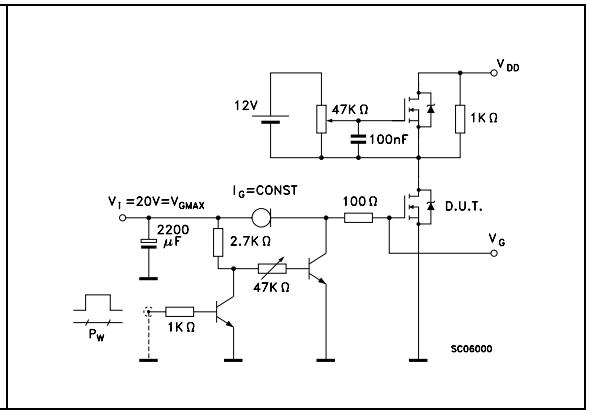


Figure 14. Test circuit for inductive load switching and diode recovery times

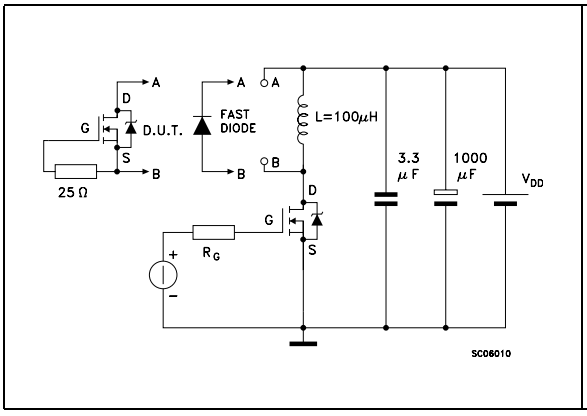


Figure 15. Unclamped inductive load test circuit

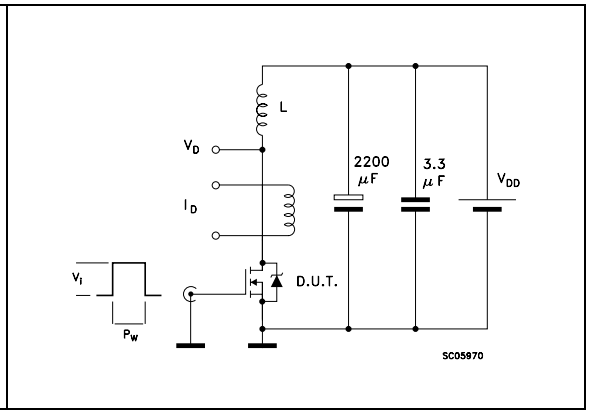


Figure 16. Unclamped inductive waveform

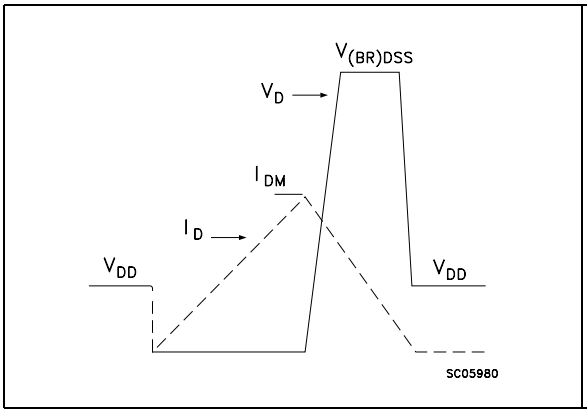
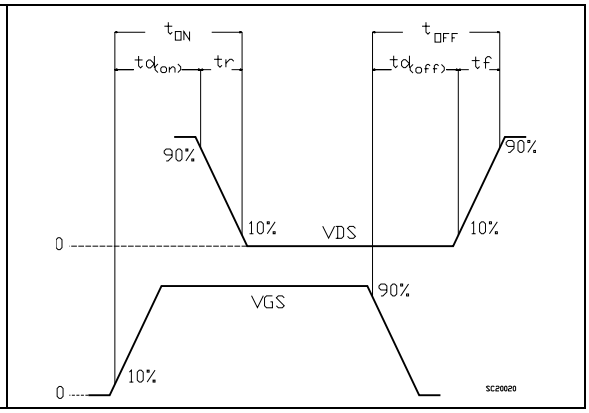


Figure 17. Switching time waveform

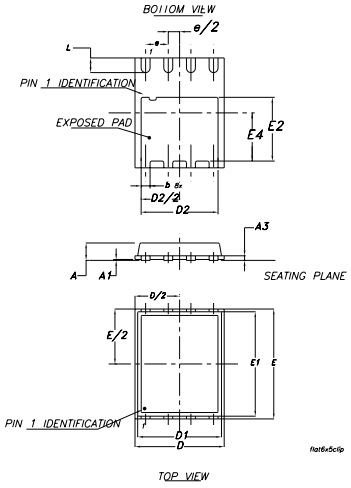


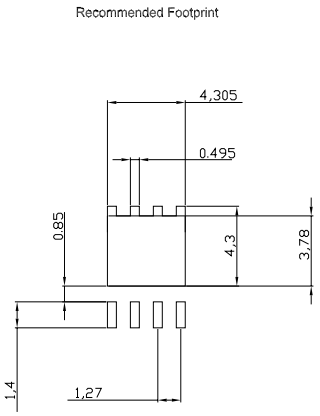
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035





Note: all dimentions are in mm.

5 Revision history

Table 7. Revision history

Date	Revision	Changes
13-May-2005	1	First release.
20-Jun-2005	2	Updated mechanical data
22-Jun-2005	3	New R_G value on *Table 6*
04-Jan-2006	4	New footprint
06-Jun-2006	5	Complete version
04-Sep-2006	6	New template, no content change
22-Nov-2006	7	Corrected part number

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