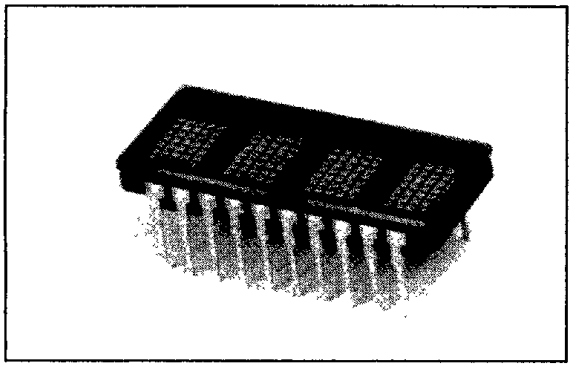
SIEMENS

# HIGH EFFICIENCY RED MPD 2545
# GREEN MPD 2547
# YELLOW MPD 2548

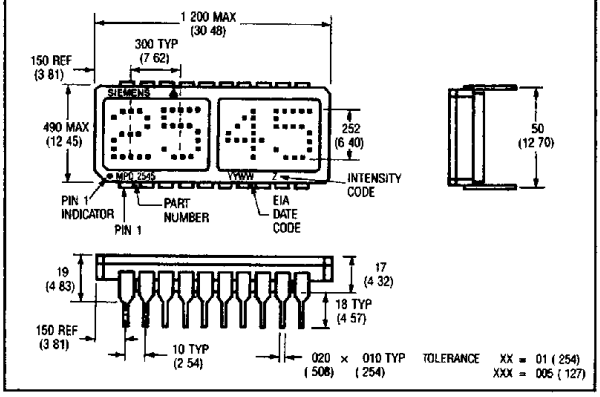
T-41-37

## .25″ 4-Character, 5×7 Dot Matrix, X-Y Stackable, HI-REL/Military Alphanumeric Programmable Display™ with Built-In CMOS Control Functions

Intelligent Display Devices



Package Dimensions in Inches (mm)




### FEATURES

- **Four .25″Dot Matrix Characters In Hermetic Package**
- **Conforms to MIL-D-87157 Quality Level A Test Table**
- **Built-in Memory, Decoders, Multiplexer and Drivers**
- **Viewing Angle, X Axis ±40°, Y Axis ±75°**
- **96-Character ASCII Format (Both Upper and Lower Case Characters)**
- **Rugged Ceramic Package, Hermetic Sealed Flat Glass Window**
- **Wide Temperature Operating Range for High Reliability Industrial and Military Use, −55°C to +100°C**
- **8-Bit Bidirectional Data BUS**
- **READ/WRITE Capability**
- **Built-In Character Generator ROM**
- **TTL Compatible**
- **Easily Cascaded for Multidisplay Operation**
- **Less CPU Time Required**
- **Software Controlled Features:**
  - **Programmable Highlight Attribute (Blinking, Non-Blinking)**
  - **Asynchronous Memory Clear Function**
  - **Lamp Test**
  - **Display Blank Function**
  - **Single or Multiple Character Blinking Function**
  - **Three Programmabale Brightness Levels**

**Important:** Refer to Appnote 18, "Using and Handling Intelligent Displays" Since this is a CMOS device, normal precautions should be taken to avoid static damage.

### GENERAL DESCRIPTION

The MPD 2545 (high efficiency red/orange), MPD 2547 (green), and MPD 2548 (yellow) are four-digit High Reliability dot matrix Programmable Displays that are aimed at satisfying the most demanding Military display requirements. They are designed for use in extremely harsh environments where only the most reliable product is acceptable. These devices are processed to meet the requirements of HI-REL/Military applications The devices are constructed in a hermetic package using four 25-inch-high 5 × 7 dot matrix displays The devices incorporate the latest in CMOS technology which is the heart of the device intelligence. The CMOS controller chip is controlled by a user-supplied eight-bit data word on the bidirectional BUS The ASCII data and attribute data are word driven. This approach allows the MPD 2545/2547/2548 to interface using the same techniques as a microprocessor peripheral

### APPLICATIONS

- **Military Control Panels**
- **Night Viewing Applications (Red Light)**
- **Cockpit Monitors**
- **Night Vision Goggle Viewable Displays (Green)**
- **Portable and Vehicle Technology**
- **Industrial Controllers**

### Maximum Ratings

| | |
|---|---|
| DC Supply | −0 5 V to +6.0 Vdc |
| Input Voltage Relative to GND (all inputs) | −0 5 V to $V_{CC}$ +0.5 Vdc |
| Operating Temperature | −55°C to +100°C |
| Storage Temperature | −55°C to +150°C |
| Thermal Resistance ($\theta_{JC}$) | 30°C/W |

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## OPTICAL CHARACTERISTICS

### High Efficiency Red MPD 2545

| Description | Symbol | Min. | Typ.(4) | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Luminous Intensity per LED(1, 3) (Character Average) | $I_{Vave}$ | 75 | 150 | | µcd | $V_{CC}$ = 5.0 V, # sign "ON" on all digits at full brightness, $T_{amb}$ = 25°C |
| Peak Wavelength | $\lambda_{PEAK}$ | | 635 | | nm | |
| Dominant Wavelength(2) | $\lambda_D$ | | 630 | | nm | |

### High Efficiency Green MPD 2547

| Description | Symbol | Min. | Typ.(4) | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Luminous Intensity per LED(1, 3) (Character Average) | $I_{Vave}$ | 75 | 150 | | µcd | $V_{CC}$ = 5.0 V, # sign "ON" on all digits at full brightness, $T_{amb}$ = 25°C |
| Peak Wavelength | $\lambda_{PEAK}$ | | 565 | | nm | |
| Dominant Wavelength(2) | $\lambda_D$ | | 570 | | nm | |

### Yellow MPD 2548

| Description | Symbol | Min. | Typ.(4) | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Luminous Intensity per LED(1, 3) (Character Average) | $I_{Vave}$ | 75 | 150 | | µcd | $V_{CC}$ = 5.0 V, # sign "ON" on all digits at full brightness, $T_{amb}$ = 25°C |
| Peak Wavelength | $\lambda_{PEAK}$ | | 585 | | nm | |
| Dominant Wavelength(2) | $\lambda_D$ | | 590 | | nm | |

**Notes:**
1 The displays are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package
2 Dominant wavelength $\lambda_D$, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device
3 The luminous sterance of the LED may be calculated using the following relationships
$L_V$ (cd/m²) = $I_V$ (Candela)/A (Meter)²
$L_V$ (Footlamberts) = π$I_V$ (Candela)/A (Foot)²
A = 8.4×10⁻⁷ ft², 78×10⁻⁶ m²
4 All typical values specified at $V_{CC}$ = 5.0 V and $T_{amb}$ = 25°C unless otherwise noted

## DC CHARACTERISTICS

| Parameter | −55°C | | | +25°C | | | +100°C | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $I_{CC}$ Blank (All Inputs Low) | | 4 | 10 | | 2.0 | 5.0 | | 1 | 2.5 | mA | $V_{CC}$ = 5 V |
| $I_{CC}$ 80 dots/unit (100% Brightness) | | 220 | 250 | | 160 | 190 | | 125 | 160 | mA | $V_{CC}$ = 5 V |
| $V_{IL}$ (all inputs) | | | 0.8 | | | 0.8 | | | 0.8 | V | $V_{CC}$ = 5 V ±0.5 V |
| $V_{IH}$ (all inputs) | 2.0 | | | 2.0 | | | 2.0 | | | V | $V_{CC}$ = 5 V ±0.5 V |
| $I_{IL}$ (all inputs) | | 70 | 120 | | 60 | 100 | | 50 | 80 | µA | $V_{IN}$ = 0.8 V $V_{CC}$ = 5.0 V |

## SWITCHING SPECIFICATIONS (@$V_{CC}$ = 4.5 V)

**WRITE CYCLE TIMING**

| Parameter | Description | Specification (ns) | | |
|---|---|---|---|---|
| | | −55°C | +25°C | +100°C |
| $T_{WD}$ | Delay time for write pulse after control signals and data (min.) | 25 | 50 | 75 |
| $T_{DH}$ | Data hold after write pulse (min.) | 25 | 50 | 75 |
| $T_{WR}$ | Write pulse width | 50 | 100 | 150 |
| $T_{WC}$ | Total write cycle time (min.) | 100 | 200 | 300 |

Notes 1 TRD=TRC−TAD−(TACC−TDD)
2 TWR=TWC−(TWD+TDH)

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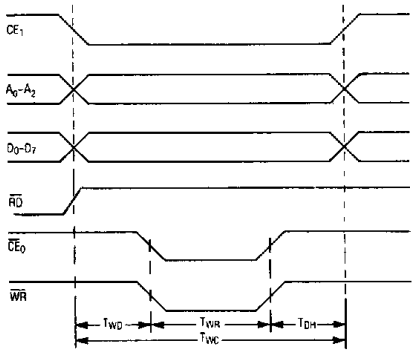
**SWITCHING SPECIFICATIONS** ($@V_{CC}$ = 4.5 V) (Continued)

| READ CYCLE TIMING | | | | |
|---|---|---|---|---|
| | | Specification (ns) | | |
| **Parameter** | **Description** | **–55°C** | **+25°C** | **+100°C** |
| $T_{AD}$ | Address set up delay after CE (min.) | 0 | 0 | 10 |
| $T_{ACC}$ | Access time for data valid after address (max ) | 100 | 175 | 200 |
| $T_{DD}$ | Delay time for data valid after read pulse (max ) | 100 | 150 | 175 |
| $T_{DH}$ | Data valid after end of read pulse (min ) | 0 | 0 | 0 |
| $T_{RD}$ | Read Pulse (min.) | 150 | 175 | 200 |
| $T_{RC}$ | Total read cycle time (min ) | 150 | 200 | 235 |

Notes 1 TRD = TRC – TAD – (TACC – TDD)
2 TWR = TWC – (TWD + TDH)

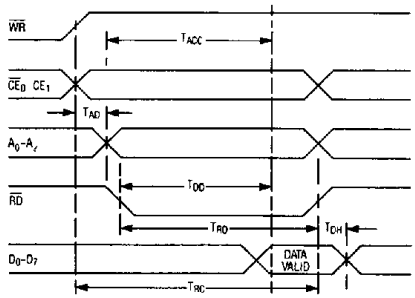
**TIMING CHARACTERISTICS** $@V_{CC}$ = 4 5 V

**DATA "WRITE" CYCLE**



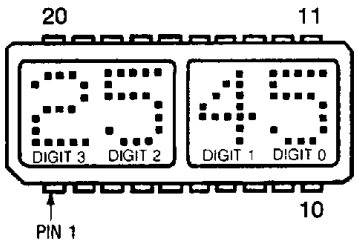

Note $T_{RD} = T_{RC} - T_{AD} - (T_{ACC} - T_{DD})$

**DATA "READ" CYCLE**




**TIMING MEASUREMENT LEVELS**


**TOP VIEW**




**PIN ASSIGNMENTS**

| PINOUT | | | |
|---|---|---|---|
| **Pin** | **Function** | **Pin** | **Function** |
| 1 $\overline{RD}$ | READ | 11 $\overline{WR}$ | WRITE |
| 2 CLK I/O | CLOCK I/O | 12 D7 | DATA MSB |
| 3 CLKSEL | CLOCK SELECT | 13 D6 | DATA |
| 4 $\overline{RST}$ | RESET | 14 D5 | DATA |
| 5 CE1 | CHIP ENABLE | 15 D4 | DATA |
| 6 $\overline{CE0}$ | CHIP ENABLE | 16 D3 | DATA |
| 7 A2 | ADDRESS MSB | 17 D2 | DATA |
| 8 A1 | ADDRESS | 18 D1 | DATA |
| 9 A0 | ADDRESS LSB | 19 D0 | DATA LSB |
| 10 GND | | 20 $V_{CC}$ | |

**PIN DEFINITIONS**

Pin

1 $\overline{RD}$ — Active low, will enable a processor to read all registers in the MPD 2545/7/8

2 CLK I/O — If CLK SEL (pin 3) is low, then expect an external clock source into this pin If CLK SEL is high, then this pin will be the master or source for all other devices which have CLK SEL low

3 CLK SEL — CLocK SELect, determines the action of pin 2. CLK I/O, see the section on Cascading for an example.

4 $\overline{RST}$ — Reset Must be held low until $V_{CC}$ > 4.5 volts. Reset is used only to synchronize blinking and will not clear the display

5 CE1 — Chip enable (active high).

6 $\overline{CE0}$ — Chip enable (active low)

7. A2 — Address input (MSB).

8 A1 — Address input.

9 A0 — Address input (LSB)

10 GND — Ground.

11 $\overline{WR}$ — Write. Active Low. If the device is selected, a low on the write input loads the data into memory.

12 D7 — Data Bus bit 7 (MSB)

13 D6 — Data Bus bit 6.

14 D5 — Data Bus bit 5.

15. D4 — Data Bus bit 4.

16. D3 — Data Bus bit 3.

17. D2 — Data Bus bit 2.

18. D1 — Data Bus bit 1

19 D0 — Data Bus bit 0 (LSB)

20. $V_{CC}$ — Plus 5 volts power pin

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**DATA INPUT COMMANDS**

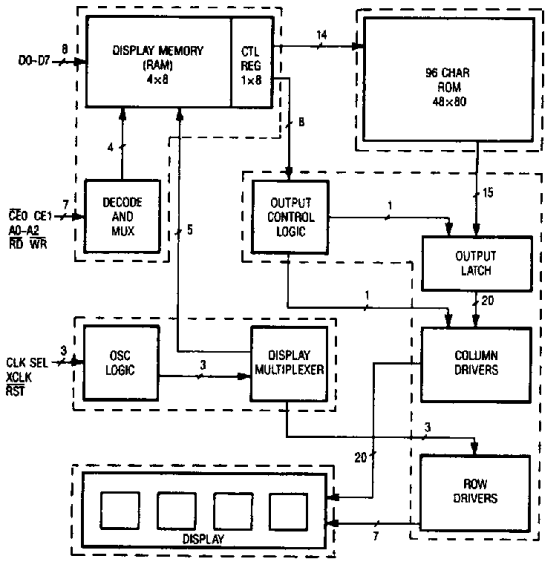
| $\overline{CE0}$ | CE1 | $\overline{RD}$ | $\overline{WR}$ | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | OPERATION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | No Change |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | Read Digit 0 Data To Bus |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | X | 0 | 1 | 0 | 0 | 1 | 0 | 0 | ($) Written To Digit 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | X | 1 | 0 | 1 | 0 | 1 | 1 | 1 | (W) Written to Digit 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | X | 1 | 1 | 0 | 0 | 1 | 1 | 0 | (f) Written To Digit 2 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | X | 0 | 1 | 1 | 0 | 0 | 1 | 1 | (3) Written to Digit 3 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | X | X | X | X | X | X | X | Char Written To Digit 0 And Cursor Enabled |

**MODE SELECTION**

| $\overline{CE0}$ | CE1 | $\overline{RD}$ | $\overline{WR}$ | OPERATION |
|---|---|---|---|---|
| 0 | 1 | 0 | 0 | Illegal |
| 1 | X | X | X | No Change |
| X | 0 | X | X | No Change |
| X | X | 1 | 1 | No Change |

NOTE 0 = Low Logic Level 1 = High Logic Level X = Don t Care

## BLOCK DIAGRAM




## FUNCTIONAL DESCRIPTION

The MPD 2545/7/8 block diagram includes 5 major blocks and internal registers (indicated by dotted lines)

**Display Memory** consists of a 5×8 bit RAM block Each of the four 8-bit words holds the 7-bit ASCII data (bits D0–D6). The fifth 8-bit memory word is used as a control word register. A detailed description of the control register and its functions can be found under the heading Control Word. Each 8-bit word is addressable and can be read from or written to

The **Control Logic** dictates all of the features of the display device and is discussed in the Control Word section of this data sheet

The **Character Generator** converts the 7-bit ASCII data into the proper dot pattern for the 96 characters shown in the character set chart

The **Clock Source** can originate either from the internal oscillator clock or from an external source—usually from the output of another MPD 2545/7/8 in a multiple module display

The **Display Multiplexer** controls all display output to the digit drivers so no additional logic is required for a display system.

The **Column Drivers** are connected directly to the display.

The **Display** has four digits. Each of the four digits is comprised of 35 LEDs in a 5×7 dot array which makes up the alphanumeric characters.

The intensity of the display can be varied by the Control Word in steps of 0% (Blank), 25%, 50%, and full brightness.

## MICROPROCESSOR INTERFACE

The interface to the microprocessor is through the address lines (A0–A2), the data bus (D0–D7), two chip select lines ($\overline{CE0}$, CE1), and read ($\overline{RD}$) and write ($\overline{WR}$) lines

To derive the appropriate enable signal, the $\overline{WR}$ and $\overline{RD}$ lines should be "NANDED" into the CE1 input. The $\overline{CE0}$ should be held low when executing a read, or write operation

The read and write lines are both active low During a valid read the data input lines (D0–D7) become outputs A valid write will enable the data as input lines

## INPUT BUFFERING

If a cable length of 6 inches or more is used, all inputs to the display should be buffered with a tri-state non-inverting buffer mounted as close to the display as conveniently possible Recommended buffers are 74LS245 for the data lines and 74LS244 for the control lines

## PROGRAMMING THE MPD 2545/7/8

There are five registers within the MPD 2545/7/8 Four of these registers are used to hold the ASCII code of the four display characters. The fifth register is the Control Word, which is used to blink, blank, clear or dim the entire display, or to change the presentation (attributes) of individual characters.

## ADDRESSING

The addresses within the display device are shown below Digit 0 is the rightmost digit of the display, while digit 3 is on the left Although there is only one Control Word, it is duplicated at the four address locations 0–3 Data can be read from any of these locations When one of these locations is written to, all of them will change together

| Address | Contents |
|---|---|
| 0 | Control Word |
| 1 | Control Word (Duplicate) |
| 2 | Control Word (Duplicate) |
| 3 | Control Word (Duplicate) |
| 4 | Digit 0 (rightmost) |
| 5 | Digit 1 |
| 6 | Digit 2 |
| 7 | Digit 3 (leftmost) |

Bit D7 of any of the display digit locations is used to allow an attribute to be assigned to that digit The attributes are discussed in the next section If bit D7 is set to a one, that character will be displayed using the attribute If bit D7 is cleared, the character will display normally

## CONTROL WORD

When address bit A2 is taken low, the Control Word is accessed. The same Control Word appears in all four of the lower address spaces of the display. Through the Control Word, the display can be cleared, the lamps can be tested, display brightness can be selected, and attributes can be set for any characters which have been loaded with their most significant bit (D7) set high.

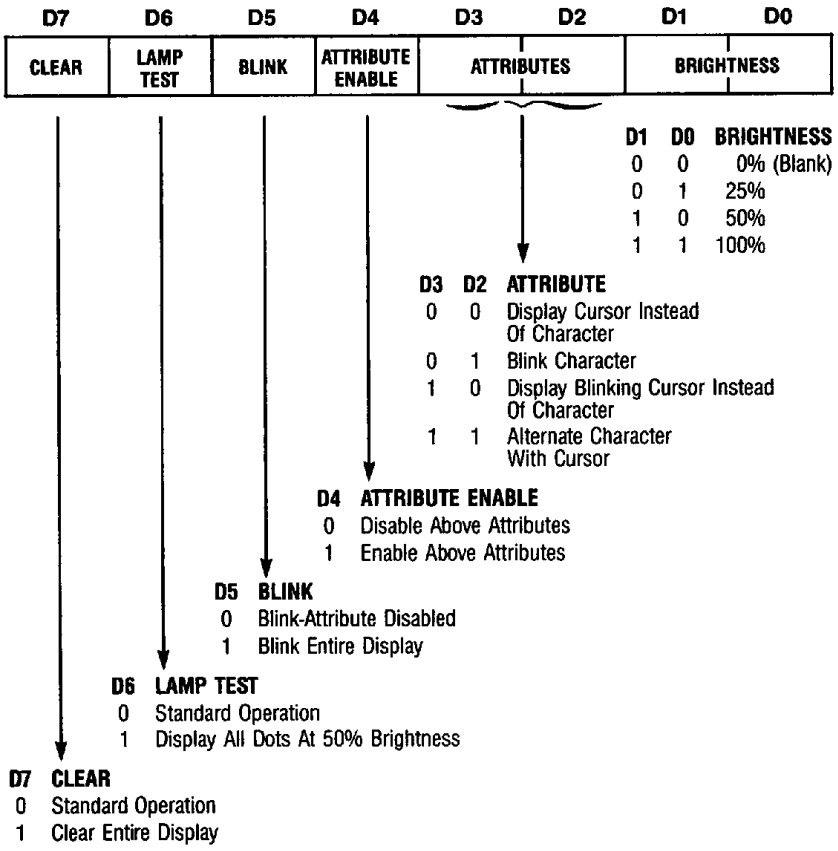
**Brightness (D0, D1):** The state of the lower two bits of the Control Word are used to set the brightness of the entire display, from 0% to 100% The table below shows the correspondence of these bits to the brightness

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | X | X | X | X | 0 | 0 | Blank |
| 0 | 0 | X | X | X | X | 0 | 1 | 25% brightness |
| 0 | 0 | X | X | X | X | 1 | 0 | 50% brightness |
| 0 | 0 | X | X | X | X | 1 | 1 | Full brightness |

X = don't care

**Attributes (D2-D4):** Bits D2, D3, and D4 control the visual attributes (i.e., blinking, alternate) of those display digits which have been written with bit D7 set high. In order to use any of the four attributes, the Cursor Enable bit (D4 in the Control Word) must be set. When the Cursor Enable bit is

### CONTROL WORD FORMAT

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set, and bit D7 in a character location is set, the character will take on one of the following display attributes.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | X | X | B | B | Disable highlight attribute |
| 0 | 0 | 0 | 1 | 0 | 0 | B | B | Display cursor* instead of character |
| 0 | 0 | 0 | 1 | 0 | 1 | B | B | Blink single character |
| 0 | 0 | 0 | 1 | 1 | 0 | B | B | Display blinking cursor* instead of character |
| 0 | 0 | 0 | 1 | 1 | 1 | B | B | Alternate character with cursor* |

*"Cursor" refers to a condition when all dots in a single character space are lit to half brightness.
X = don't care
B = depends on the selected brightness

Attributes are non-destructive. If a character with bit D7 set is replaced by a cursor (Control Word bit D4 is set, and D3=D2=0) the character will remain in memory and can be revealed again by clearing D4 in the Control Word

**Blink (D5):** The entire display can be caused to blink at a rate of approximately 2Hz by setting bit D5 in the Control Word. This blinking is independent of the state of D7 in all character locations

In order to synchronize the blink rate in a bank of these devices, it is necessary to tie all devices' clocks and resets together as described in a later section of this data sheet

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | X | X | X | B | B | Blinking display |

**Lamp Test (D6):** When the Lamp Test bit is set, all dots in the entire display are lit at half brightness. When this bit is cleared, the display returns to the characters that were showing before the lamp test.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | X | X | X | X | X | Lamp test |

**Clear Data (7):** When D7 is set in the Control Word all character and Control Word memory bits are reset to zero This causes total erasure of the display, and returns all digits to a non-blink, the preset brightness, non-cursor status.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | X | X | % | % | Clear |

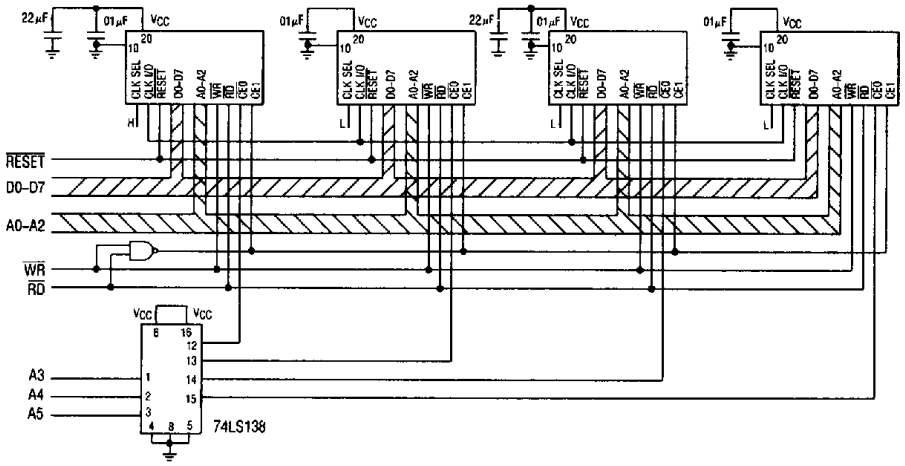
## CASCADING

Cascading the MPD 2545/7/8 is a simple operation. The requirements for cascading are 1) decoding the correct address to determine the chip select for each additional device, 2) assuring that all devices are reset simultaneously, and 3) selecting one display as the clock source and setting all others to accept clock input (the reason for cascading the clock is to synchronize the flashing of multiple displays) One display as a source is capable of driving six other MPD 2545/7/8s. If more displays are required, a buffer will be necessary The source display must have pin 3 tied high to output clock signals. All other displays must have pin 3 tied low

## VOLTAGE TRANSIENTS

It has become common practice to provide 0.01 µf bypass capacitors liberally in digital systems. Like other CMOS circuitry, the Intelligent Display controller chip has very low power consumption and the usual 0.01 µf would be adequate were it not for the LEDs. The module itself can, in some conditions, use up to 100 mA (multiplexed). In order to prevent power supply transients, capacitors with low inductance and high capacitance at high frequencies are required This suggests a solid tantalum or ceramic disc for high frequency bypass. For larger displays, distribute the bypass capacitors evenly, keeping capacitors as close to the power pins as possible. We recommend a 10 µf and 0.01 µf for every Intelligent Display to decouple the displays themselves, at the display.

### CASCADING THE MPD 2545/7/8



## HOW TO LOAD INFORMATION INTO THE MPD 2545/7/8

Information loaded into the MPD 2545/7/8 can be either ASCII data or Control Word data. The following procedure (see also typical loading sequence) will demonstrate a typical loading sequence and the resulting visual display The word STOP is used in all of the following examples

**SET BRIGHTNESS**

**Step 1** Set the brightness level of the entire display to your preference (example: 100%)

**LOAD FOUR CHARACTERS**

**Step 2** Load an "S" in the left-hand digit.

**Step 3** Load a "T" in the next digit.

**Step 4** Load an "O" in the next digit.

**Step 5** Load a "P" in the right-hand digit.

If you loaded the information correctly, the MPD 2545 should now show the word "STOP."

**BLINK A SINGLE CHARACTER**

**Step 6** Into the digit, second from the right, load the hex code "CF," which is the code for an "O" with the D7 bit added as a control bit.

NOTE. the "O" is the only digit which has the control bit (D7) added to normal ASCII data.

**Step 7** Load enable blinking character into the control word register.

The MPD 2545 should now display "STOP" with a flashing "O."

**ADD ANOTHER BLINKING CHARACTER**

**Step 8** Into the left hand digit, load the hex code "D3" which is for an "S" with the D7 bit added as a control bit.

The MPD 2545 should display "STOP" with a flashing "O" and a flashing "S."

**ALTERNATE CHARACTER/CURSOR ENABLE**

**Step 9** Load enable alternate character/cursor into the control word register.

The MPD 2545 should now display "STOP" with the "O" and the "S" alternating between the letter and a cursor (all dots lit).

**INITIATE FOUR-CHARACTER BLINKING**

(Regardless of Control Bit setting)

**Step 10** Load enable display blinking.

The MPD 2545 should now display the entire word "STOP" blinking.

## ELECTRICAL AND MECHANICAL CONSIDERATIONS

The CMOS IC of the MPD 2545/7/8 is designed to provide resistance to both Electrostatic and Discharge Damage and Latch Up due to voltage or current surges Several precautions are strongly recommended for the user, to avoid overstressing these built-in safeguards.

### ESD PROTECTION

Users of the MPD 2545/7/8 should be careful to handle the devices consistent with Standard ESD protection procedures. Operators should wear appropriate wrist, ankle or feet ground straps and avoid clothing that collects static charges Work surfaces, tools and transport carriers that come into contract with unshielded devices or assemblies should also be appropriately grounded

### LATCH UP PROTECTION

Latch up is a condition that occurs in CMOS ICs after the input protection diodes have been broken down. These diodes can be reversed through several means

$V_{IN} < GND$, $V_{IN} > V_{CC} + 0.5$ V, or through excessive currents begin forced on the inputs. When these situations exist, the IC may develop the response of an SCR and begin conducting as much as one amp through the $V_{CC}$ pin. This destructive condition will persist (latched) until device failure or the device is turned off

The Voltage Transient Suppression Techniques and buffer interfaces for longer cable runs help considerably to prevent latch conditions from occuring Additionally, the following Power Up and Power Down sequence should be observed.

### POWER UP SEQUENCE

1. Float all active signals by tri-stating the inputs to the displays.
2. Apply $V_{CC}$ and GND to the display
3. Apply active signals to the displays by enabling all input signals per application.

### POWER DOWN SEQUENCE

1. Float all active signals by tri-stating the inputs to the display.
2. Turn off the power to the display

## TYPICAL LOADING SEQUENCE

| | $\overline{CE0}$ | CE1 | $\overline{RD}$ | $\overline{WR}$ | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DISPLAY |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | L | H | H | L | L | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| 2 | L | H | H | L | H | H | H | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | S |
| 3 | L | H | H | L | H | H | L | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | ST |
| 4 | L | H | H | L | H | L | H | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | STO |
| 5 | L | H | H | L | H | L | L | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | STOP |
| 6 | L | H | H | L | H | L | H | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | STOP |
| 7 | L | H | H | L | L | X | X | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | STO*P |
| 8 | L | H | H | L | H | H | H | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | S*TO*P |
| 9 | L | H | H | L | L | X | X | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | S†TO†P |
| 10 | L | H | H | L | L | X | X | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | S*T*O*P* |

*Blinking Character
† Character alternating with cursor (all dots lit)

CHARACTER SET

| | D0 | L | H | L | H | L | H | L | H | L | H | L | H | L | H | L | H |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D1 | L | L | H | H | L | L | H | H | L | L | H | H | L | L | H | H |
| | D2 | L | L | L | L | H | H | H | H | L | L | L | L | H | H | H | H |
| | D3 | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H |
| D6 | D5 | D4 | HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| L | L | L | 0 | THESE CODES DISPLAY BLANK | | | | | | | | | | | | | | | |
| L | L | H | 1 | | | | | | | | | | | | | | | | |
| L | H | L | 2 | | ! | " | # | $ | % | & | ' | ( | ) | * | + | , | - | . | / |
| L | H | H | 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : | ; | < | = | > | ? |
| H | L | L | 4 | @ | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O |
| H | L | H | 5 | P | Q | R | S | T | U | V | W | X | Y | Z | [ | \ | ] | ^ | _ |
| H | H | L | 6 | ` | a | b | c | d | e | f | g | h | i | j | k | l | m | n | o |
| H | H | H | 7 | p | q | r | s | t | u | v | w | x | y | z | { | \| | } | ~ | |

Notes 1 A2 must be held high for ASCII data
2 Bit D7 = 1 enables attributes for the assigned digit

## GENERAL QUALITY ASSURANCE LEVELS

The parts are tested in conformance with Quality Level A of MIL-D-87157 for hermetically sealed LED displays with 100% screening. The product is tested to Tables I, II, IIIa and IVa.

**Table I. Quality Level A of MIL-D-87157**

| Test Screen | Method | Conditions |
|---|---|---|
| 1. Precap Visual | 2072 MIL-STD-750 | |
| 2. High Temperature Storage | 1032 MIL-STD-750 | $T_{amb}$ = 125 °C, Time = 24 hours |
| 3. Temperature Cycling | 1051 MIL-STD-750 | Condition B, 10 Cycles, 15 min. Dwell |
| 4. Constant Acceleration | 2006 MIL-STD-750 | 5,000 G's at $Y_1$ Orientation |
| 5. Fine Leak | 1071 MIL-STD-750 | Condition G or H |
| 6. Gross Leak | 1071 MIL-STD-750 | Condition C |
| 7. Interim Electrical/Optical Tests | | Limits and conditions are per the Electrical/Optical Characteristics. The $I_{OH}$ and $I_{OL}$ tests are the inverse of $V_{OH}$ and $V_{OL}$ specified in the Electrical Characteristics $T_{amb}$ = 25 °C |
| 8 Burn-In(1) | 1015 MIL-STD-883 | Condition B at $V_{CC}$ = 5.5 V, $T_{amb}$ = 100 °C. t = 160 hours |
| 9. Final Electrical Test | | Same as Step 7 |
| 10. External Visual | 2009 MIL-STD-883 | |

**Note:**
1 MIL-STD 883 test method applies

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**Table II. Group A Electrical Tests – MIL-D-87157**

| Subgroup/Test | Parameters | LTPD |
|---|---|---|
| Subgroup 1<br>DC Electrical Tests at 25°C | Limits and conditions are per the Electrical/Optical Characteristics. The $I_{OH}$ and $I_{OL}$ tests are the inverse of $V_{OH}$ and $V_{OL}$ specified in the Electrical Characteristics. | 5 |
| Subgroup 2<br>Selected DC Electrical Tests at High Temperatures | | 7 |
| Subgroup 3<br>Selected DC Electrical Tests at Low Temperatures | | 7 |
| Subgroup 4, 5 and 6 Not Applicable | | |
| Subgroup 7<br>Optical and Functional Tests at 25°C | Satisfied by Subgroup 1 | 5 |
| Subgroup 8<br>External Visual | | 7 |

**Table IIIa. Group B, Class A and B of MIL-D-87157**

| Subgroup/Test | MIL-STD-750 Method | Conditions | Sample Size |
|---|---|---|---|
| Subgroup 1<br>Resistance to Solvents | 1022 | | 4 Devices/0 Failures |
| Internal Visual and Mechanical(3) | 2014 | | 1 Device/0 Failures |
| Subgroup 2(1 2)<br>Solderability | 2026 | $T_{amb}$ = 245°C for 5 seconds | LTPD = 15 |
| Subgroup 3<br>Thermal Shock (Temp Cycle) | 1051 | Condition B, 10 Cycles, 15 min Dwell | LTPD = 15 |
| Moisture Resistance | 1021 | | |
| Fine Leak | 1071 | Condition G or H | |
| Gross Leak | 1071 | Condition C | |
| Electrical/Optical Endpoints | | Limits and conditions are per the Electrical/Optical Characteristics The $I_{OH}$ and $I_{OL}$ tests are the inverse of $V_{OH}$ and $V_{OL}$ specified in the Electrical Characteristics $T_{amb}$ = 25°C | |
| Subgroup 4(1)<br>Operating Life Test (340 hours) | 1027 | $T_{amb}$ = 100°C @ $V_{CC}$ = 5 5 V | LTPD = 10 |
| Electrical/Optical Endpoints | | Same as Subgroup 3 | |
| Subgroup 5<br>Non-Operating (Storage) Life Test (340 hours) | 1032 | $T_{amb}$ = + 125°C | LTPD = 10 |
| Electrical/Optical Endpoints | | Same as Subgroup 3 | |

**Notes:**
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required
3. MIL-STD-883 test methods apply
4. Visual requirements shall be as specified in MIL STD-883 Methods 1010 or 1011

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**Table IVa. Group C, Class A and B of MIL-D-87157**

| Subgroup/Test | MIL-STD-750 Method | Conditions | Sample Size |
|---|---|---|---|
| Subgroup 1<br>Physical Dimensions | 2066 | | 2 Devices/0 Failures |
| Subgroup 2(2 6)<br>Lead Integrity | 2004 | Condition B2 | LTPD = 15 |
| Fine Leak | 1071 | Condition G or H | |
| Gross Leak | 1071 | Condition C | |
| Subgroup 3<br>Shock | 2016 | 1500G, Time = 0 5 ms, 5 Blows in Each Orientation X1, Y1, Y2 | LTPD = 15 |
| Vibration, Variable Frequency | 2056 | | |
| Constant Acceleration | 2006 | 5,000G at Y1 Orientation | |
| External Visual(4) | 1001 or 1011 | | |
| Electrical/Optical Endpoints | | Limits and conditions are per the Electrical/Optical Characteristics The $I_{OH}$ and $I_{OL}$ tests are the inverse of $V_{OH}$ and $V_{OL}$ specified in the Electrical Characteristics $T_{amb} = 25°C$. | |
| Subgroup 4(1 3)<br>Salt Atmosphere | 1041 | | LTPD = 15 |
| External Visual(4) | 1010 or 1011 | | LTPD = 20 (C = 0) |
| Subgroup 5<br>Bond Strength(5) | 2037 | Condition A | |
| Subgroup 6<br>Operating Life Test(7) | 1026 | $T_{amb} = 100°C$ @ $V_{CC} = 5.5$ V | $\lambda = 10$ |
| Electrical/Optical Endpoints(7) | 1026 | Same as Subgroup 3 | |

**Notes:**

1 Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used
2 The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required
3 Solderability samples shall not be used
4 Visual requirements shall be as specified in MIL-STD 883, Methods 1010 or 1011
5 Displays may be selected prior to seal
6 MIL STD-883 test method applies
7 Test method or conditions in accordance with detail specification

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