Multicell Battery Stack Monitor

FEATURES

- Measures up to 12 Li-Ion Cells in Series (60V Max)
- Stackable Architecture Enables >1000V Systems
- 0.25% Maximum Total Measurement Error
- 13ms to Measure All Cells in a System
- Cell Balancing:
  - On-Chip Passive Cell Balancing Switches
  - Provision for Off-Chip Passive Balancing
- Two Thermistor Inputs Plus On-Board Temperature Sensor
- 1MHz Daisy-Chainable Serial Interface
- High EMI Immunity
- Delta Sigma Converter with Built-In Noise Filter
- Open Wire Connection Fault Detection
- Low Power Modes
- 44-Lead SSOP Package

APPLICATIONS

- Electric and Hybrid Electric Vehicles
- High Power Portable Equipment
- Backup Battery Systems
- High Voltage Data Acquisition Systems

DESCRIPTION

The LTC®6802-1 is a complete battery monitoring IC that includes a 12-bit ADC, a precision voltage reference, a high voltage input multiplexer and a serial interface. Each LTC6802-1 can measure up to 12 series connected battery cells with an input common mode voltage up to 60V. In addition, multiple LTC6802-1 devices can be placed in series to monitor the voltage of each cell in a long battery string. The unique level-shifting serial interface allows the serial ports of these devices to be daisy-chained without optocouplers or isolators.

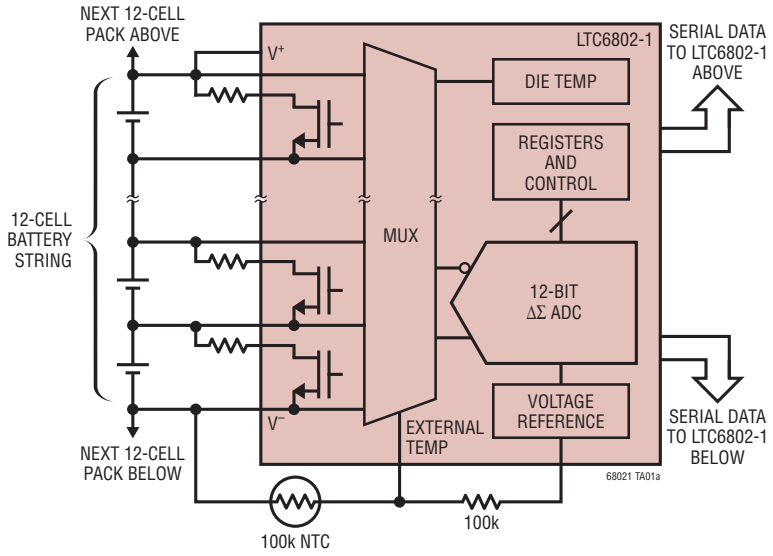
When multiple LTC6802-1 devices are connected in series they can operate simultaneously, permitting all cell voltages in the stack to be measured within 13ms.

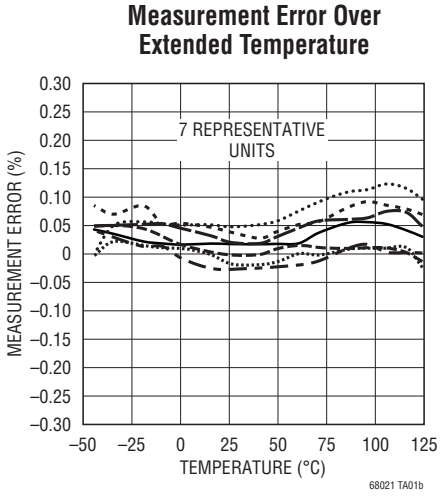
To minimize power, the LTC6802-1 offers a measure mode, which simply monitors each cell for overvoltage and undervoltage conditions. A standby mode is also provided.

Each cell input has an associated MOSFET switch for discharging overcharged cells.

For large battery stack applications requiring individually addressable serial communications, see the LTC6802-2.

TYPICAL APPLICATION





ABSOLUTE MAXIMUM RATINGS

(Note 1)

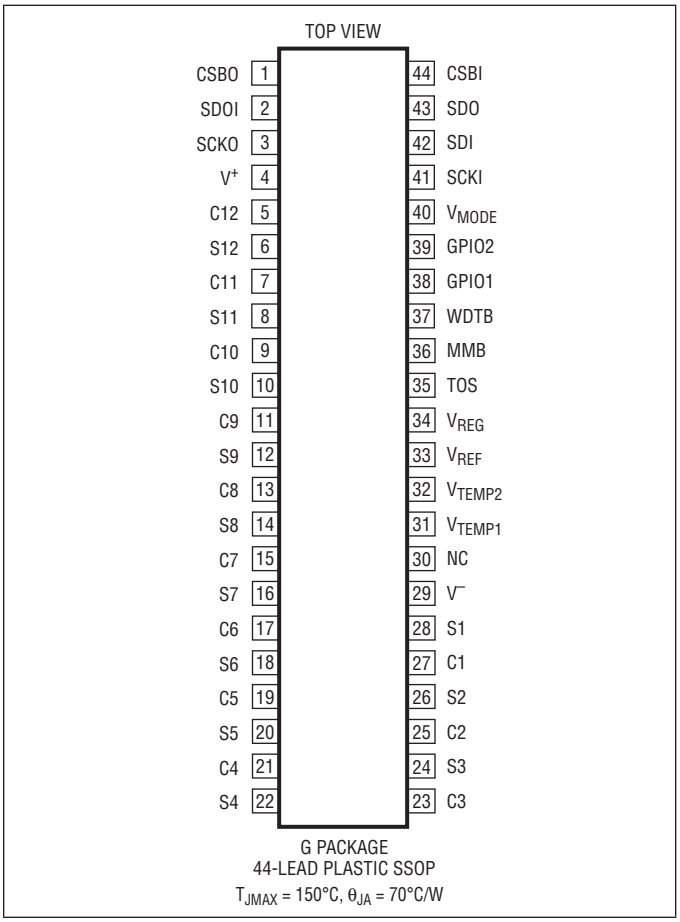
Total Supply Voltage (V^+ to V^-) 60V
Input Voltage (Relative to V^-)
- C1 ..... –0.3V to 9V
- C12 ..... V^+ – 0.6V to V^+ + 0.3V
- Cn (Note 5) ..... –0.3V to min (9 • n, 60V)
- Sn (Note 5) ..... –0.3V to min (9 • n, 60V)
- CSBO, SCKO, SDOI ..... V^+ – 0.6V to V^+ + 0.3V
- All other pins ..... –0.3V to 7V

Voltage Between Inputs
- Cn to Cn-1 ..... –0.3V to 9V
- Sn to Cn-1 ..... –0.3V to 9V
- C12 to C8 ..... –0.3V to 25V
- C8 to C4 ..... –0.3V to 25V
- C4 to V^- ..... –0.3V to 25V

Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

*n = 1 to 12

PIN CONFIGURATION



G PACKAGE
44-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6802IG-1#PBF	LTC6802IG-1#TRPBF	LTC6802G-1	44-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 43.2V, V^- = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Specifications							
V_{ACC}	Measurement Resolution	Quantization of the ADC	●		1.5		mV/Bit
	ADC Offset Voltage	(Note 2)	●	–0.5		0.5	mV
	ADC Gain Error	(Note 2)		–0.12		0.12	%
			●	–0.22		0.22	%
V_{ERR}	Total Measurement Error	(Note 4)					
		V_{CELL} = 0V			0.8		mV
		V_{CELL} = 2.3V		–2.8		2.8	mV
		V_{CELL} = 2.3V	●	–5.1		5.1	mV
		V_{CELL} = 3.6V		–4.3		4.3	mV
		V_{CELL} = 3.6V	●	–7.9		7.9	mV
		V_{CELL} = 4.2V		–5		5	mV
		V_{CELL} = 4.2V	●	–9.2		9.2	mV
		V_{CELL} = 4.6V			±8		mV
		V_{TEMP} = 2.3V	●	–5.1		5.1	mV
		V_{TEMP} = 3.6V	●	–7.9		7.9	mV
		V_{TEMP} = 4.2V	●	–9.2		9.2	mV
V_{CELL}	Cell Voltage Range	Full Scale Voltage Range			5		V
V_{CM}	Common Mode Voltage Range Measured Relative to V^-	Range of Inputs CN for <0.25% Gain Error, N = 3 to 11	●	3.7		5 • N	V
		Range of Input C3 for <1% Gain Error	●	1.8		15	V
		Range of Input C2 for <0.25% Gain Error	●	1.2		10	V
		Range of Input C1 for <0.25% Gain Error	●	0		5	V
	Overvoltage (OV) Detection Level	Programmed for 4.2V	●	4.182	4.200	4.218	V
	Undervoltage (UV) Detection Level	Programmed for 2.3V	●	2.290	2.300	2.310	V
	Die Temperature Measurement Error	Error in Measurement at 125°C			3		°C
V_{REF}	Reference Pin Voltage	R_{LOAD} = 100k to V^-		3.020	3.065	3.110	V
			●	3.015	3.065	3.115	V
	Reference Voltage Temperature Coefficient				8		ppm/°C
	Reference Voltage Thermal Hysteresis	25°C to 85°C and 25°C to –40°C			100		ppm
	Reference Voltage Long Term Drift				60		ppm/$\sqrt{khr}$
V_{REG}	Regulator Pin Voltage	10 < V^+ < 50, No Load	●	4.5	5.0	5.5	V
		I_{LOAD} = 4mA	●	4.1	4.8		V
	Regulator Pin Short Circuit Current Limit		●	5	8		mA
V_S	Supply Voltage, V^+ Relative to V^-	V_{ERR} Specifications Met	●	10		50	V
		Timing Specifications Met	●	4		50	V
I_B	Input Bias Current	In/Out of Pins C1 Thru C12					
		When Measuring Cells	●	–10		10	µA
		When Not Measuring Cells			1		nA
I_S	Supply Current, Active	Current Into the V^+ Pin when Measuring Voltages			0.8	1.1	mA
		with the ADC	●			1.2	mA
I_M	Supply Current, Monitor Mode	Average Current Into the V^+ Pin While Monitoring for UV and OV Conditions					
		Continuous Monitoring (CDC = 2)			800		µA
		Monitor Every 130ms (CDC = 5)			225		µA
		Monitor Every 500ms (CDC = 6)			150		µA
		Monitor Every 2s (CDC = 7)			100		µA
I_{QS}	Supply Current, Idle	Current into the V^+ Pin When Idle		35	60	80	µA
		All Serial Port Pins at Logic '1'	●	30		85	µA
I_{CS}	Supply Current, Serial I/O	All Serial Port Pins at Logic '0' V_{MODE} = 0, This Current is Added to I_S or I_{QS}	●	3		4.5	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 43.2V, V^- = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Discharge Switch On-Resistance	V_{CELL} > 3V (Note 3)	●		10	20	Ω
	Temperature Range		●	–40		85	°C
	Thermal Shutdown Temperature				145		°C
	Thermal Shutdown Hysteresis				5		°C
Voltage Mode Timing Specifications							
t_{CYCLE}	Measurement Cycle Time	Time Required to Measure 11 or 12 Cells Time Required to Measure Up to 10 Cells Time Required to Measure 1 Cell	● ● 	11 9.2 1	13 11 1.2	16 13.5 1.5	ms ms ms
t_1	SDI Valid to SCKI Rising Setup		●	10			ns
t_2	SDI Valid to SCKI Rising Hold		●	250			ns
t_3	SCKI Low		●	400			ns
t_4	SCKI High		●	400			ns
t_5	CSBI Pulse Width		●	400			ns
t_6	SCKI Rising to CSBI Rising		●	100			ns
t_7	CSBI Falling to SCKI Rising		●	100			ns
t_8	SCKI Falling to SDO Valid		●			250	ns
	Clock Frequency		●			1	MHz
	Watchdog Timer Time Out Period		●	1		2.5	s
Timing Specifications							
t_{PD1}	CSBI to CSBO	C_{CSBO} = 150pF	●			600	ns
t_{PD2}	SCKI to SCKO	C_{SCKO} = 150pF	●			300	ns
t_{PD3}	SDI to SDOI Write Delay	C_{SDOI} = 150pF	●			300	ns
t_{PD4}	SDOI to SDI Read Delay	C_{SDO} = 150pF	●			300	ns
Voltage Mode Digital I/O Specifications							
V_{IH}	Digital Input Voltage High	Pins SCKI, SDI, and CSBI	●	2			V
V_{IL}	Digital Input Voltage Low	Pins SCKI, SDI, and CSBI	●			0.8	V
V_{OL}	Digital Output Voltage Low	Pin SDO; Sinking 500µA	●			0.3	V
Current Mode Digital I/O Specifications							
I_{IH1}	Digital Input Current High	Pins CSBI, SCKI, and SDI (Write)	●			10	µA
I_{IL1}	Digital Input Current Low	Pins CSBI, SCKI, and SDI (Write)	●	1000			µA
I_{IH2}	Digital Input Current High	Pin SDOI (Read)	●			–1000	µA
I_{IL2}	Digital Input Current Low	Pin SDOI (Read)	●	–10			µA
I_{OH1}	Digital Output Current High	Pins CSBO, SCKO, and SDOI (Write)	●		3	10	µA
I_{OL1}	Digital Output Current Low	Pins CSBO, SCKO, and SDOI (Write)	●	1000	1200	1650	µA
I_{OH2}	Digital Output Current High	Pin SDI (Read)	●	–1650	–1200	–1000	µA
I_{OL2}	Digital Output Current Low	Pin SDI (Read)	●	–10	–3	0	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The ADC specifications are guaranteed by the Total Measurement Error (V_{ERR}) specification.

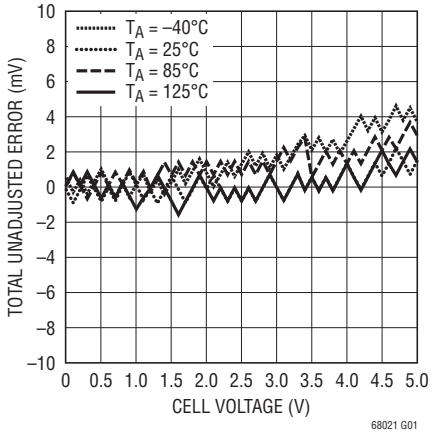
Note 3: Due to the contact resistance of the production tester, this specification is tested to relaxed limits. The 20Ω limit is guaranteed by design.

Note 4: V_{CELL} refers to the voltage applied across the following pin combinations: Cn to Cn-1 for n = 2 to 12, C1 to V^-. V_{TEMP} refers to the voltage applied from V_{TEMP1} or V_{TEMP2} to V^-.

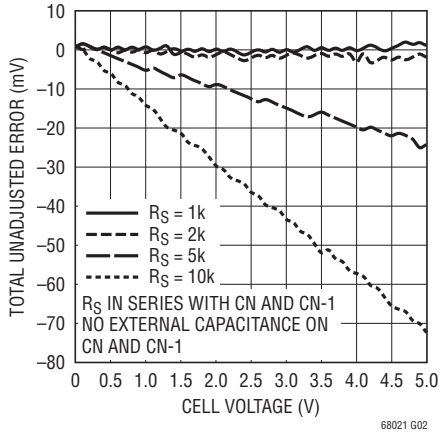
Note 5: These absolute maximum ratings apply provided that the voltage between inputs do not exceed their absolute maximum ratings.

TYPICAL PERFORMANCE CHARACTERISTICS

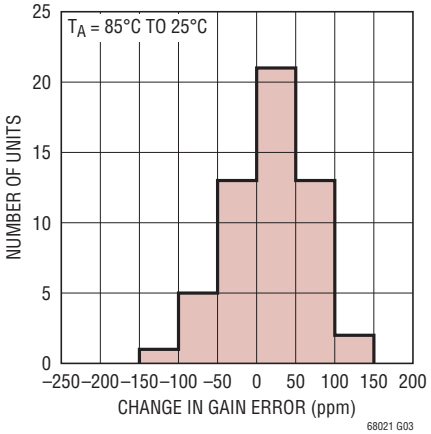
Cell Measurement Total Unadjusted Error



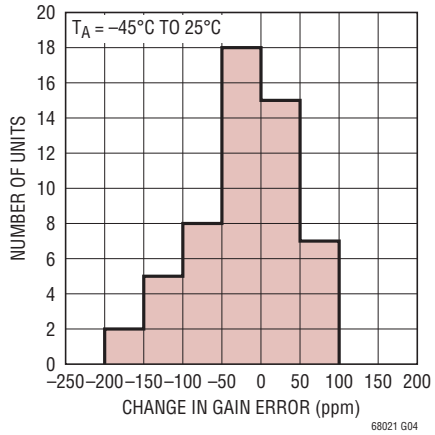
Cell Measurement Total Unadjusted Error vs Input Resistance



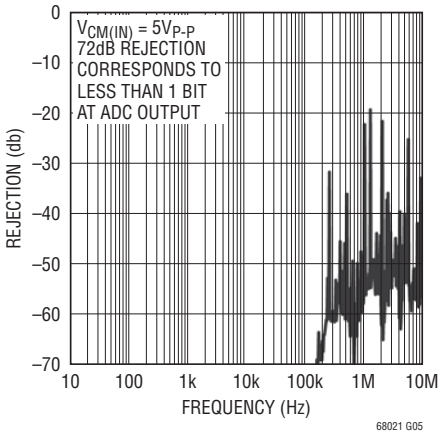
Measurement Gain Error Hysteresis



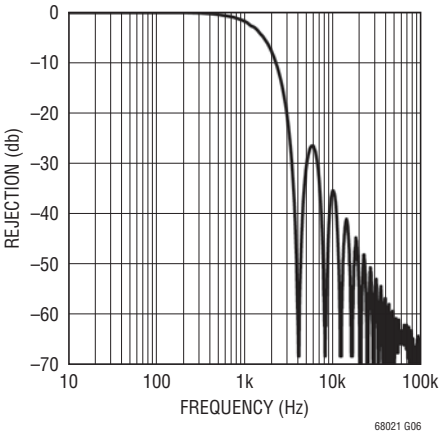
Measurement Gain Error Hysteresis



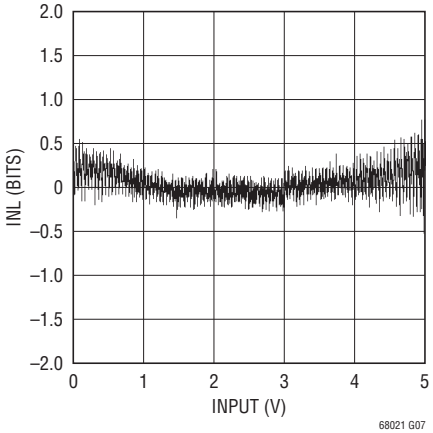
Cell Measurement Common Mode Rejection



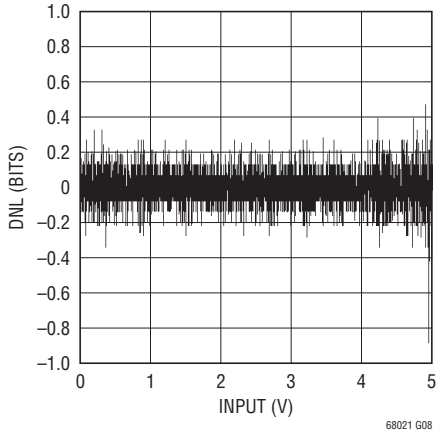
ADC Normal Mode Rejection vs Frequency



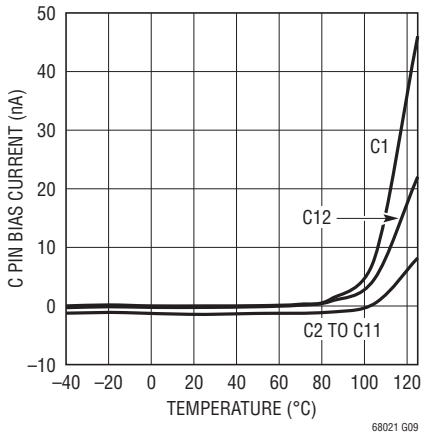
ADC INL



ADC DNL

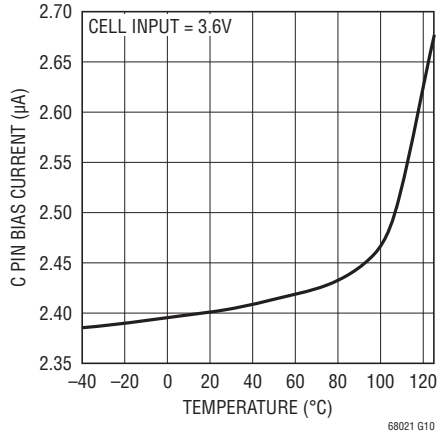


Cell Input Bias Current in Standby

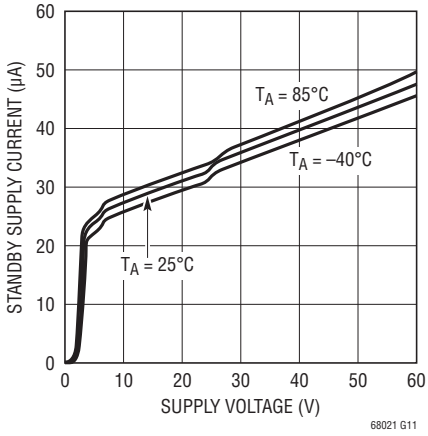


TYPICAL PERFORMANCE CHARACTERISTICS

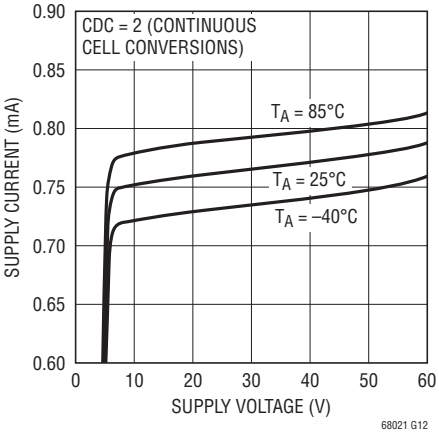
Cell Input Bias Current During Conversion



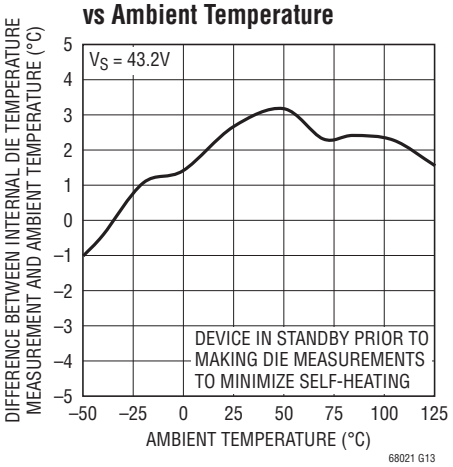
Supply Current vs Supply Voltage Standby



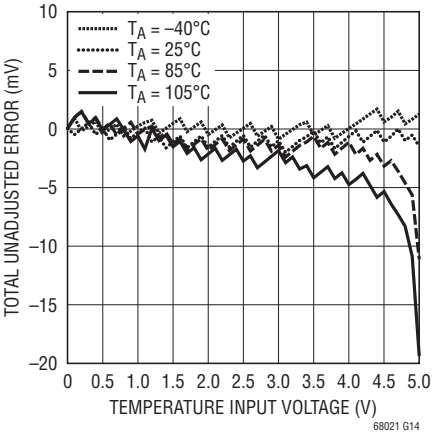
Supply Current vs Supply Voltage in CDC = 2



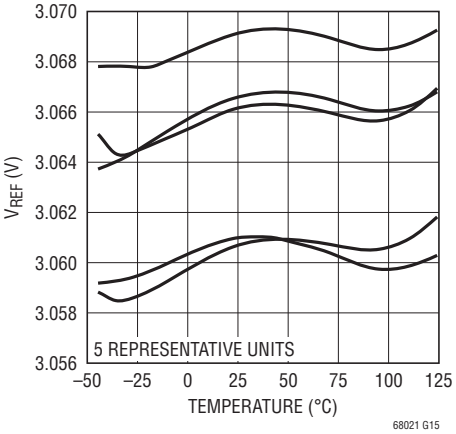
Internal Die Temperature Measurement vs Ambient Temperature



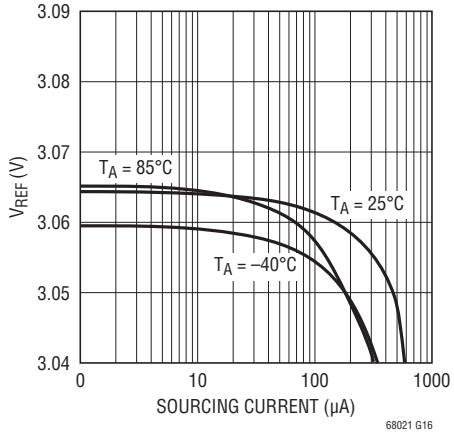
External Temperature Measurement Total Unadjusted Error vs Input



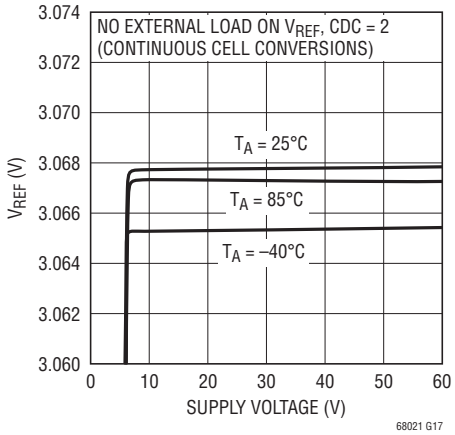
V_{REF} Output Voltage vs Temperature



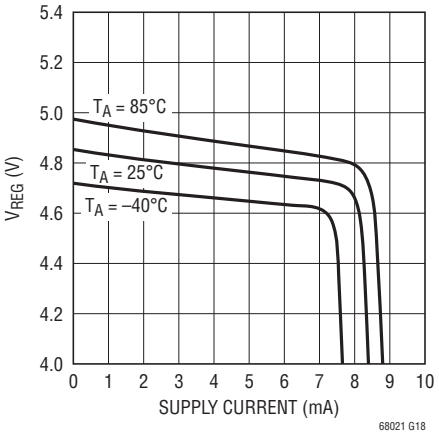
V_{REF} Load Regulation



V_{REF} Line Regulation

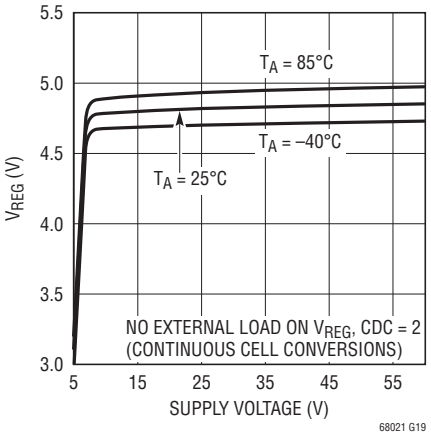


V_{REG} Load Regulation

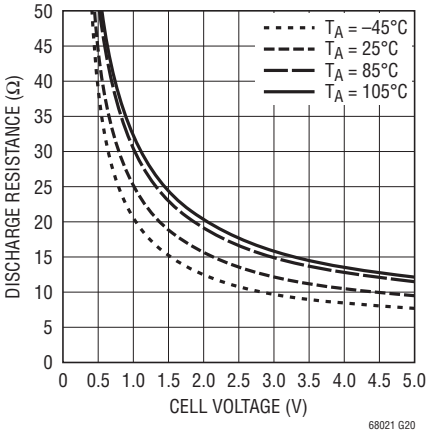


TYPICAL PERFORMANCE CHARACTERISTICS

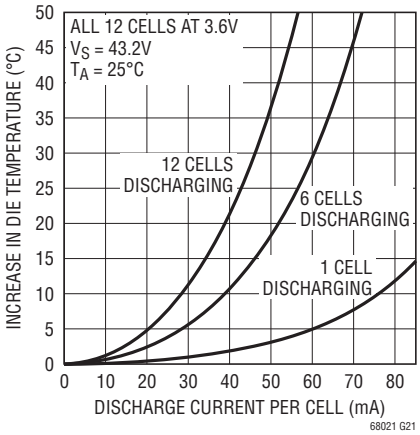
V_{REG} Line Regulation



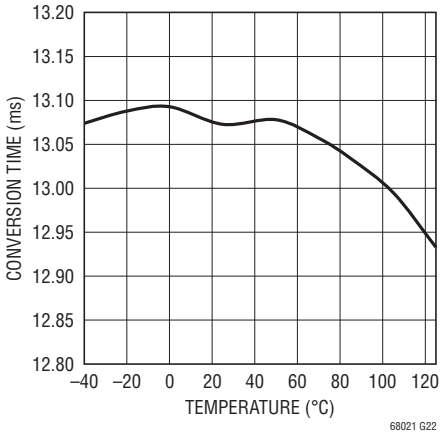
Internal Discharge Resistance vs Cell Voltage



Die Temperature Increase vs Discharge Current in Internal FET



Cell Conversion Time



PIN FUNCTIONS

CSBO (Pin 1): Chip Select Output (Active Low). CSBO is a buffered version of the chip select input, CSBI. CSBO drives the next IC in the daisy chain. See Serial Port in the Applications Information section.

SDOI (Pin 2): Serial Data I/O Pin. SDOI transfers data to and from the next IC in the daisy chain. See Serial Port in the Applications Information section.

SCKO (Pin 3): Serial Clock Output. SCKO is a buffered version of SCKI. SCKO drives the next IC in the daisy chain. See Serial Port in the Applications Information section.

V^+ (Pin 4): Tie pin 4 to the most positive potential in the battery stack. Typically V^+ is the same potential as C12.

C12, C11, C10, C9, C8, C7, C6, C5, C4, C3, C2, C1 (Pins 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27): C1 through C12 are the inputs for monitoring battery cell voltages. Up to 12 cells can be monitored. The lowest potential is tied to pin V^-. The next lowest potential is tied to C1 and so forth. See the figures in the Applications Information section for more details on connecting batteries to the LTC6802-1.

The LTC6802-1 can monitor a series connection of up to 12 cells. Each cell in a series connection must have a common mode voltage that is greater than or equal to the cells below it.

S12, S11, S10, S9, S8, S7, S6, S5, S4, S3, S2, S1 (Pins 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28): S1 though S12 pins are used to balance battery cells. If one cell in a series becomes over charged, an S output can be used to discharge the cell. Each S output has an internal N-channel MOSFET for discharging. See the Block Diagram. The NMOS has a maximum on resistance of 20Ω. An external resistor should be connected in series with the NMOS to dissipate heat outside of the LTC6802-1 package. When using the internal MOSFETs to discharge cells, the die temperature should be monitored. See Power Dissipation and Thermal Shutdown in the Applications Information section.

The S pins also feature an internal 10k pull-up resistor. This allows the S pins to be used to drive the gates of external P-channel MOSFETs for higher discharge capability.

V^- (Pin 29): Connect V^- to the most negative potential in the series of cells.

NC (Pin 30): Pin 30 is internally connected to V^- through 10Ω. Pin 30 can be left unconnected or connected to pin 29 on the PCB.

V_{TEMP1}, V_{TEMP2} (Pins 31, 32): Temperature Sensor Inputs. The ADC measures the voltage on V_{TEMPx} with respect to V^- and stores the result in the TMP registers. The ADC measurements are relative to the V_{REF} pin voltage. Therefore a simple thermistor and resistor combination connected to the V_{REF} pin can be used to monitor temperature. The V_{TEMP} inputs can also be general purpose ADC inputs.

V_{REF} (Pin 33): 3.075V Voltage Reference Output. This pin should be bypassed with a 1µF capacitor. The V_{REF} pin can drive a 100k resistive load connected to V^-. Larger loads should be buffered with an LT6003 op amp, or similar device.

V_{REG} (Pin 34): Linear Voltage Regulator Output. This pin should be bypassed with a 1µF capacitor. The V_{REG} pin is capable of supplying up to 4mA to an external load. The V_{REG} pin does not sink current.

TOS (Pin 35): Top of Stack Input. Tie TOS to V_{REG} when the LTC6802-1 is the top device in a daisy chain. Tie TOS to V^- when the LTC6802-1 is any other device in a daisy chain. When TOS is tied to V_{REG}, the LTC6802-1 ignores the SDOI input. When TOS is tied to V^-, the LTC6802-1 expects data to be passed to and from the SDOI pin.

MMB (Pin 36): Monitor Mode (Active Low) Input. When MMB is low (same potential as V^-), the LTC6802-1 goes into monitor mode. See Modes of Operation in the Applications Information section.

WDTB (Pin 37): Watchdog Timer Output (Active Low). If there is no activity on the SCKI pin for 2.5 seconds, the WDTB output is asserted. The WDTB pin is an open drain NMOS output. When asserted it pulls the output down to V^- and resets the configuration register to its default state. See Watchdog Timer Circuit in the Applications Information section.

PIN FUNCTIONS

GPIO1, GPIO2 (Pins 38, 39): General Purpose Input/Output. The operation of these pins depends on the state of the MMB pin.

When MMB is high, the pins behave as traditional GPIOs. By writing a "0" to a GPIO configuration register bit, the open drain output is activated and the pin is pulled to V^-. By writing a logic "1" to the configuration register bit, the corresponding GPIO pin is high impedance. An external resistor is needed to pull the pin up to V_{REG}.

By reading the configuration register locations GPIO1 and GPIO2, the state of the pins can be determined. For example, if a "0" is written to register bit GPIO1, a "0" is always read back because the output NMOSFET pulls pin 38 to V^-. If a "1" is written to register bit GPIO1, the pin becomes high impedance. Either a "1" or a "0" is read back, depending on the voltage present at pin 38. The GPIOs makes it possible to turn on/off circuitry around the LTC6802-1, or read logic values from a circuit around the LTC6802-1.

When the MMB pin is low, the GPIO pins and the WDTB pin are treated as inputs that set the number of cells to be monitored. See Monitor Mode in the Applications Information section.

V_{MODE} (Pin 40): Voltage Mode Input. When V_{MODE} is tied to V_{REG}, the SCKI, SDI, SDO, and CSBI pins are configured as voltage inputs and outputs. This means these pins accept standard TTL logic levels. Connect V_{MODE} to V_{REG} when the LTC6802-1 is the bottom device in a daisy chain.

When V_{MODE} is connected to V^-, the SCKI, SDI, and CSBI pins are configured as current inputs and outputs, and SDO is unused. Connect V_{MODE} to V^- when the LTC6802-1 is being driven by another LTC6802-1 in a daisy chain.

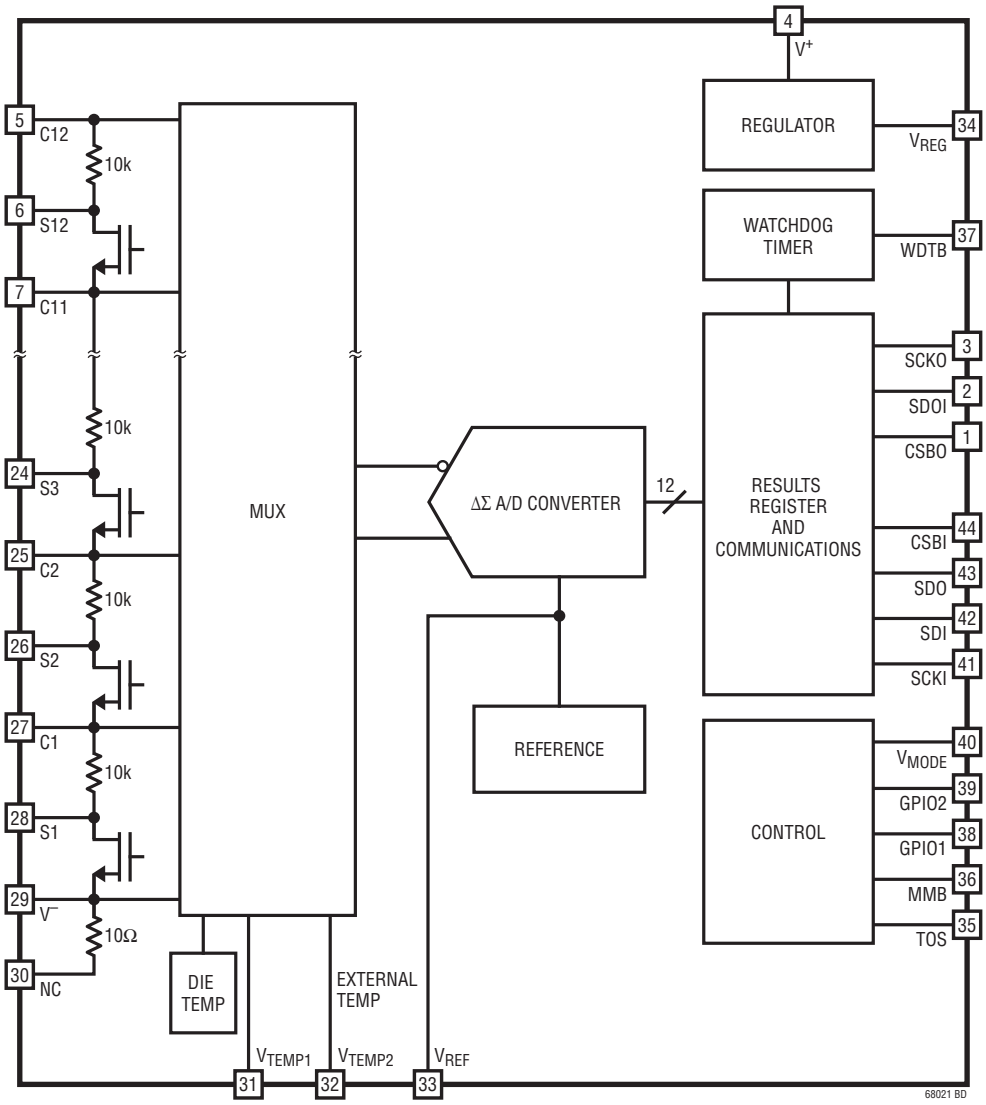
SCKI (Pin 41): Serial Clock Input. The SCKI pin interfaces to any logic gate (TTL levels) if V_{MODE} is tied to V_{REG}. SCKI must be driven by the SCKO pin of another LTC6802-1 if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

SDI (Pin 42): Serial Data Input. The SDI pin interfaces to any logic gate (TTL levels) if V_{MODE} is tied to V_{REG}. SDI must be driven by the SDOI pin of another LTC6802-1 if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

SDO (Pin 43): Serial Data Output. The SDO pin is an NMOS open drain output if V_{MODE} is tied to V_{REG}. SDO is not used if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

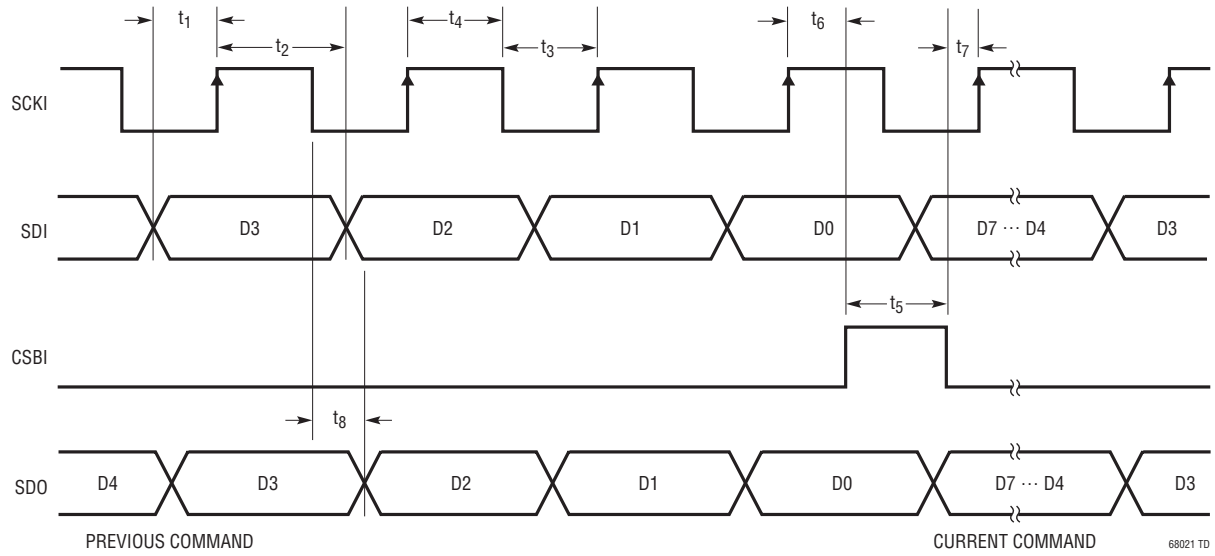
CSBI (Pin 44): Chip Select (Active Low) Input. The CSBI pin interfaces to any logic gate (TTL levels) if V_{MODE} is tied to V_{REG}. CSBI must be driven by the CSBO pin of another LTC6802-1 if V_{MODE} is tied to V^-. See Serial Port in the Applications Information section.

BLOCK DIAGRAM



TIMING DIAGRAM

Timing Diagram of the Serial Interface



OPERATION

THEORY OF OPERATION

The LTC6802-1 is a data acquisition IC capable of measuring the voltage of 12 series connected battery cells. An input multiplexer connects the batteries to a 12-bit delta-sigma analog to digital converter (ADC). An internal 10ppm voltage reference combined with the ADC give the LTC6802-1 its outstanding measurement accuracy. The inherent benefits of the delta-sigma ADC versus other types of ADCs (e.g. successive approximation) are explained in Advantages of Delta-Sigma ADCs in the Applications Information section.

Communication between the LTC6802-1 and a host processor is handled by a SPI compatible serial interface. As shown in Figure 1, the LTC6802-1's can pass data up and down a stack of devices using simple diodes for isolation. This operation is described in Serial Port in the Applications Information section.

The LTC6802-1 also contains circuitry to balance cell voltages. Internal MOSFETs can be used to discharge cells. These internal MOSFETs can also be used to control external balancing circuits. Figure 1 illustrates cell balancing by internal discharge. Figure 4 shows the S pin controlling an external balancing circuit. It is important to note that the LTC6802-1 makes no decisions about turning on/off the internal MOSFETs. This is completely controlled by the host processor. The host processor writes values to a configuration register inside the LTC6802-1 to control the switches. The watchdog timer on the LTC6802-1 will turn off the discharge switches if communication with the host processor is interrupted.

OPEN CONNECTION DETECTION

When a cell input (C pin) is open, it affects two cell measurements. Figure 2 shows an open connection to C3, in an application without external filtering between the C pins and the cells. During normal ADC conversions (that is, using the STCVAD command), the LTC6802 will give near zero readings for B3 and B4 when C3 is open. The zero reading for B3 occurs because during the measurement of B3, the ADC input resistance will pull C3 to the C2 potential. Similarly, during the measurement of B4, the ADC input resistance pulls C3 to the C4 potential.

OPERATION

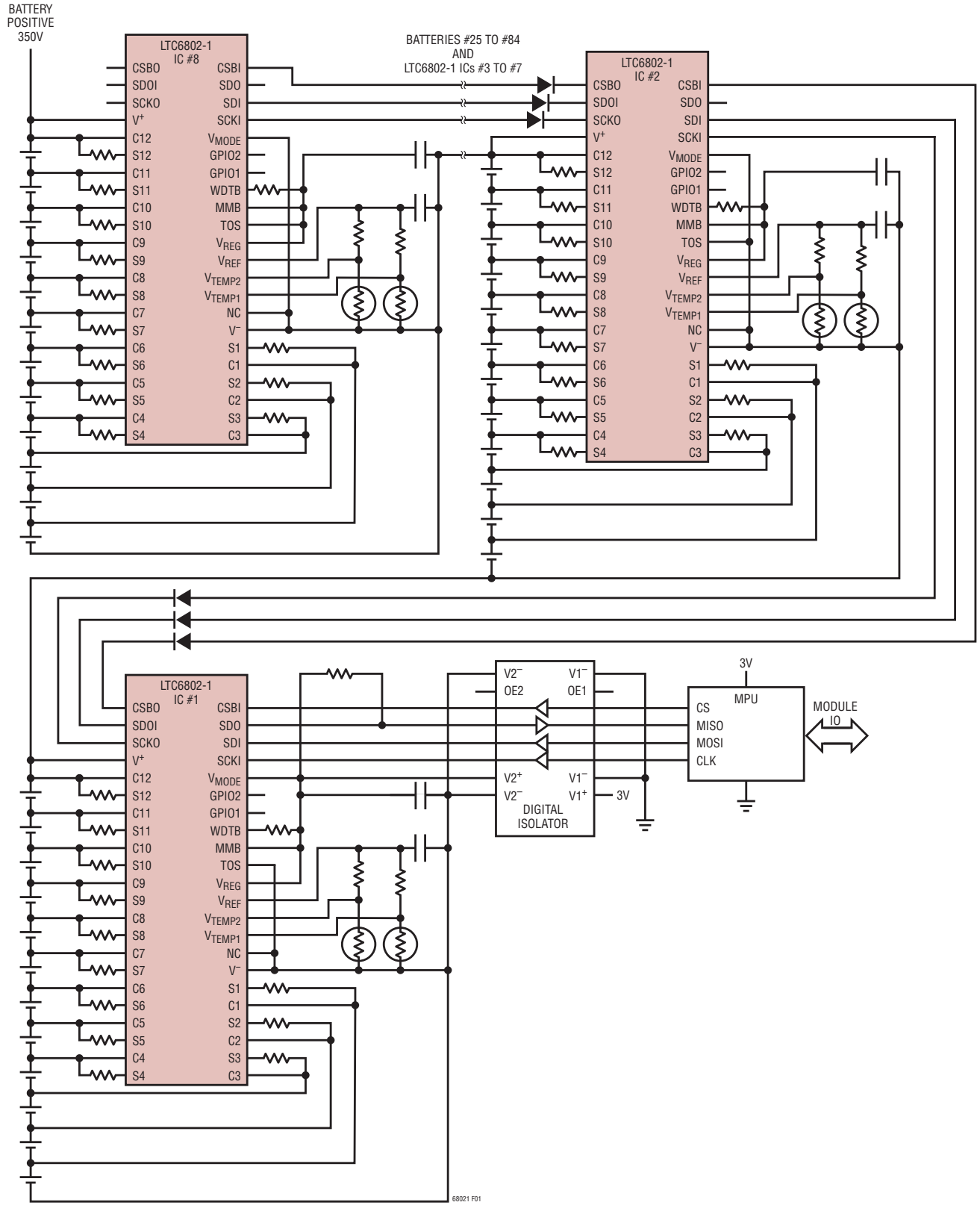


Figure 1. 96-Cell Battery Stack, Daisy Chain Interface. This is a Simplified Schematic Showing the Basic Multi-IC Architecture

OPERATION

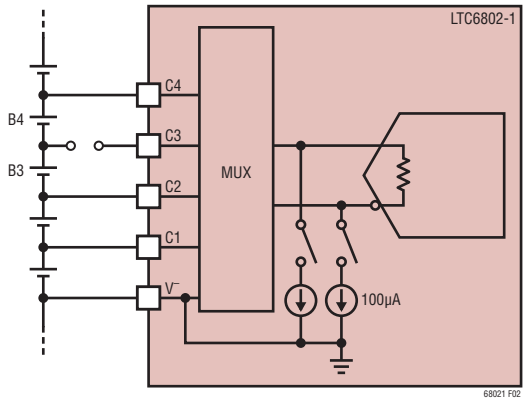


Figure 2. Open Connection

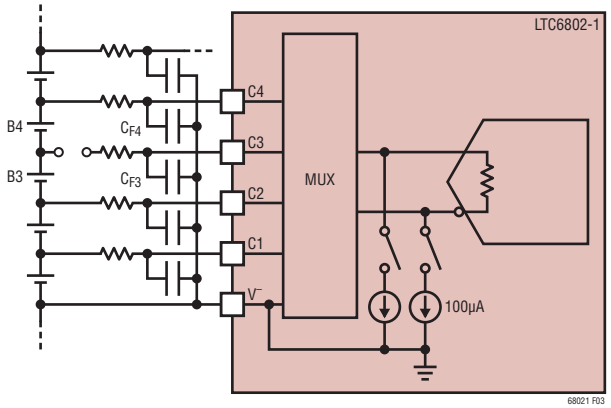


Figure 3. Open Connection with RC Filtering

Figure 3 shows an open connection at the same point in the cell stack as Figure 2, but this time there is an external filter network still connected to C3. Depending on the value of the capacitor remaining on C3, a normal measurement of B3 and B4 may not give near-zero readings, since the C3 pin is not truly open. In fact, with a large external capacitance on C3, the C3 voltage will be charged midway between C2 and C4 after several cycles of measuring cells B3 and B4. Thus the measurements for B3 and B4 may indicate a valid cell voltage when in fact the exact state of B3 and B4 is unknown.

To reliably detect an open connection, the command STOWAD is provided. With this command, two 100µA current sources are connected to the ADC inputs and turned on during all cell conversions. Referring again to Figure 3, with the STOWAD command, the C3 pin will be pulled down by the 100µA current source during the B3 cell measurement AND during the B4 cell measurement. This will tend to decrease the B3 measurement result and increase the B4 measurement result relative to the normal STCVAD command. The biggest change is observed in the B4 measurement when C3 is open. So, the best method to detect an open wire at input C3 is to look for an increase in the measurement of the cell connected between inputs C3 and C4 (cell B4).

Thus the following algorithm can be used to detect an open connection to cell pin CN:

(1) Issue a STCVAD command (ADC convert without 100µA current sources).

(2) Issue a RDCV command and store all cell measurements into array CELLA(N).

(3) Issue a STOWAD command (ADC convert with 100µA current sources).

(4) Issue a RDCV command and store all cell measurements into array CELLB(N).

(5) For each value of N from 1 to 11:

If CELLB(N+1) – CELLA(N+1) ≥ +200mV, then CN is open, otherwise it is not open.

The +200mV threshold is chosen to provide tolerance for errors in the measurement with the 100µA current source connected. Even without an open connection there is always some difference between a cell measured with and without the 100µA current source because of the IR drop across the finite resistance of the MUX switches. On the other hand, with capacitors larger than 0.1µF remaining on an otherwise open C pin, the 100µA current source may not be enough to move the open C pin 200mV with a single STOWAD command. If the STOWAD command is repeated several times, the large external capacitor will discharge enough to create a 200mV change in cell readings. To detect an open connection with larger than 0.1µF capacitance still on the pin, one must repeat step (3) above a number of times before proceeding to step (4).

The algorithm above determines if the CN pin is open based on measurements of the N+1 Cell. For example, in a 12-cell system, the algorithm finds opens on pins C1

OPERATION

through C11 by looking at the measurements of cells B2 through B12. Therefore the algorithm cannot be used to determine if the topmost C pin is open. Fortunately, an open wire from the battery to the top C pin usually means the V^+ pin is also floating. When this happens, the readings for the top battery cell will always be 0V, indicating a failure. If the top C pin is open yet V^+ is still connected, then the best way to detect an open connection to the top C pin is by comparing the sum of all cell measurements using the STCVAD command to an auxiliary measurement of the sum of all the cells, using a method similar to that shown in Figure 18. A significantly lower result for the calculated sum of all 12 cells suggests an open connection to the top C pin, provided it was already determined that no other C pin is open.

DISCHARGING DURING CELL MEASUREMENTS

The primary cell voltage A/D measurement commands (STCVAD and STOWAD) automatically turn off a cell's discharge switch while its voltage is being measured. The discharge switches for the cell above and the cell below will also be turned off during the measurement. For example, discharge switches S4, S5, and S6 will be disabled while cell 5 is being measured.

In some systems it may be desirable to allow discharging to continue during cell voltage measurements. The cell voltage A/D conversion commands STCVDC and STOWDC allow any enabled discharge switches to remain on during cell voltage measurements. This feature allows the system to perform a self-test to verify the discharge functionality and multiplexer operation.

All discharge switches are automatically disabled during OV and UV comparison measurements.

A/D CONVERTER DIGITAL SELF TEST

Two self test commands can be used to verify the functionality of the digital portions of the ADC. The self tests also verify the cell voltage registers and temperature monitoring registers. During these self tests a test signal is applied to the ADC. If the circuitry is working properly all cell voltage and temperature registers will contain identical codes. For Self Test 1 the registers will contain 0x555. For Self Test 2, the registers will contain 0xAAA. The time required for the self test function is the same as required to measure all cell voltages or all temperature sensors. Perform the self test function with CDC[2:0] set to 1 in the configuration register.

USING THE S PINS AS DIGITAL OUTPUTS OR GATE DRIVERS

The S outputs include an internal 10k pull-up resistor. Therefore the S pins will behave as a digital output when loaded with a high impedance, e.g. the gate of an external MOSFET. For applications requiring high battery discharge currents, connect a discrete PMOS switch device and suitable discharge resistor to the cell, and the gate terminal to the S output pin, as illustrated in Figure 4.

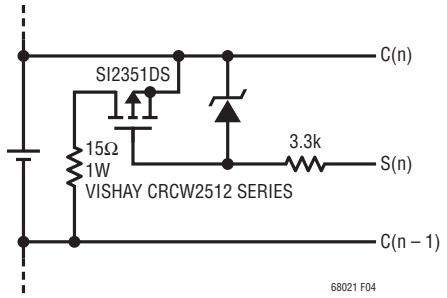


Figure 4. External Discharge FET Connection (One Cell Shown)

OPERATION

POWER DISSIPATION AND THERMAL SHUTDOWN

The MOSFETs connected to the pins S1 through S12 can be used to discharge battery cells. An external resistor should be used to limit the power dissipated by the MOSFETs. The maximum power dissipation in the MOSFETs is limited by the amount of heat that can be tolerated by the LTC6802-1. Excessive heat results in elevated die temperatures. The electrical characteristics are guaranteed for die temperatures up to 85°C. Little or no degradation will be observed in the measurement accuracy for die temperatures up to 105°C. Damage may occur near 150°C, therefore the recommended maximum die temperature is 125°C.

To protect the LTC6802-1 from damage due to overheating, a thermal shutdown circuit is included. Overheating of the device can occur when dissipating significant power in the cell discharge switches or when communicating frequently to the device using the current-mode serial interface. The problem is exacerbated when operating with a large voltage between V^+ and V^- or when the thermal conductivity of the system is poor.

If the temperature detected on the device goes above approximately 145°C, the configuration registers will be reset to default states, turning off all discharge switches and disabling A/D conversions. When a thermal shutdown has occurred, the THSD bit in the temperature register group will go high. The bit is cleared by performing a read of the temperature registers (RDTMP command).

Since thermal shutdown interrupts normal operation, the internal temperature monitor should be used to determine when the device temperature is approaching unacceptable levels.

APPLICATIONS INFORMATION

USING THE LTC6802-1 WITH LESS THAN 12 CELLS

The LTC6802-1 can typically be used with as few as four cells. The minimum number of cells is governed by the supply voltage requirements of the LTC6802-1. The sum of the cell voltages must be 10V to guarantee that all electrical specifications are met.

Figure 5 shows an example of the LTC6802-1 when used to monitor seven cells. The lowest C inputs connect to the seven cells and the upper C inputs connect to V^+. Other configurations, e.g. 9 cells, would be configured in the same way: the lowest C inputs connected to the battery cells and the unused C inputs connected to V^+. The unused inputs will result in a reading of 0V for those channels.

The ADC can also be commanded to measure a stack of cells by making 10 or 12 measurements, depending on the state of the CELL10 bit in the control register. Data from all 10 or 12 measurements must be down loaded when reading the conversion results. The ADC can be commanded to measure any individual cell voltage.

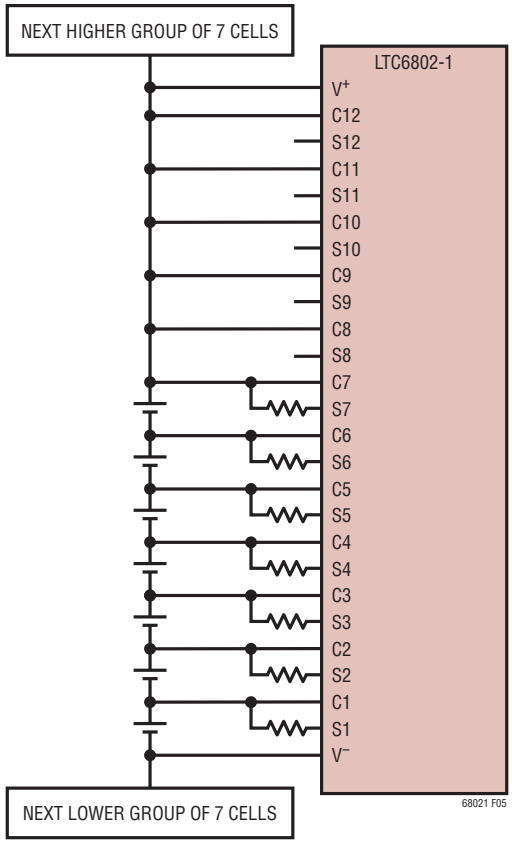


Figure 5. Monitoring 7 Cells with the LTC6802-1

USING THE GENERAL PURPOSE INPUTS/OUTPUTS (GPIO1, GPIO2)

The LTC6802-1 has two general purpose digital inputs/outputs. By writing a GPIO configuration register bit to a logic low, the open drain output can be activated. The GPIOs give the user the ability to turn on/off circuitry around the LTC6802-1. One example might be a circuit to verify the operation of the system.

When a GPIO configuration bit is written to a logic high, the corresponding GPIO pin may be used as an input. The read back value of that bit will be the logic level that appears at the GPIO pin.

When the MMB pin is low, the GPIO pins and the WDTB pin are treated as inputs that set the number of cells to be monitored. See the Monitor Mode section.

WATCHDOG TIMER CIRCUIT

The LTC6802-1 includes a watchdog timer circuit. If no activity is detected on the SCKI pin for 2.5 seconds, the WDTB open drain output is asserted low. The WDTB pin remains low until an edge is detected on the SCKI pin.

When the watchdog timer circuit times out, the configuration bits are reset to their default (power-up) state.

In the power-up state, the S outputs are off. Therefore, the watchdog timer provides a means to turn off cell discharging should communications to the MPU be interrupted. The IC is in the minimum power standby mode after a time out. Note that externally pulling the WDTB pin low will not reset the configuration bits.

The watchdog timer operation is disabled when MMB is low.

When reading the configuration register, byte CFG0 bit 7 will reflect the state of the WDTB pin.

REVISION CODE

The temperature register group contains a 3-bit revision code. If software detection of device revision is necessary, then contact the factory for details. Otherwise, the code can be ignored. In all cases, however, the values of all bits must be used when calculating the packet error code (PEC) CRC byte on data reads.

APPLICATIONS INFORMATION

MODES OF OPERATION

The LTC6802-1 has three modes of operation: standby, measure and monitor. Standby mode is a power saving state where all circuits except the serial interface are turned off. In measure mode, the LTC6802-1 is used to measure cell voltages and store the results in memory. Measure mode will also monitor each cell voltage for overvoltage (OV) and undervoltage (UV) conditions. In monitor mode, the device will only monitor cells for UV and OV conditions. A signal is output on the SDO pin to indicate the UV/OV status. The serial interface is disabled in monitor mode.

Standby Mode

The LTC6802-1 defaults (powers up) to standby mode. Standby mode is the lowest possible supply current state. All circuits are turned off except the serial interface and the voltage regulator. For the lowest possible standby current consumption all SPI logic inputs should be set to a logic 1 level. The LTC6802-1 can be programmed for standby mode by setting the comparator duty cycle configuration bits, CDC[2:0], to 0. If the part is put into standby mode while ADC measurements are in progress, the measurements will be interrupted and the cell voltage registers will be in an indeterminate state. To exit standby mode, the CDC bits must be written to a value other than 0.

Measure Mode

LTC6802-1 is in measure mode when the CDC bits are programmed with a value from 1 to 7. The IC monitors each cell voltage and produces an interrupt signal on the SDO pin indicating all cell voltages are within the UV and OV limits. There are two methods for indicating the UV/OV interrupt status: toggle polling (using a 1kHz output signal) and level polling (using a high or low output signal). The polling methods are described in the Serial Port section.

The UV/OV limits are set by the VUV and VOV values in the configuration registers. When a cell voltage exceeds the UV/OV limits a bit is set in the flag register. The UV and OV flag status for each cell can be determined using the *Read Flag Register Group*.

If fewer than 12 cells are connected to the LTC6802-1 then it is necessary to mask the unused input channels. The MCxI bits in the configuration registers are used to mask channels. If the CELL10 bit is high, then the inputs for cells 11 and 12 are automatically masked.

The LTC6802-1 can monitor UV and OV conditions continuously. Alternatively, the duty cycle of the UV and OV comparisons can be reduced or turned off to lower the overall power consumption. The CDC bits are used to control the duty cycle.

To initiate cell voltage measurements while in measure mode, *a Start A/D Conversion and Poll Status* command must be sent. After the command has been sent, the LTC6802-1 will send the A/D converter status using either the toggle polling or the level polling method, as described in the Serial Port section. If the CELL10 bit is high, then only the bottom 10 cell voltages will be measured, thereby reducing power consumption and measurement time. By default the CELL10 bit is low, enabling measurement of all 12 cell voltages. During cell voltage measurement commands, UV and OV flag conditions, reflected in the flag register group, are also updated. When the measurements are complete, the part will go back to monitoring UV and OV conditions at the rate designated by the CDC bits.

Monitor Mode

The LTC6802-1 can be used as a simple monitoring circuit with no serial interface by pulling the MMB pin low. When in this mode, the interrupt status is indicated on the SDO pin using the toggle polling mode described in the Serial Port section. Unlike serial port polling commands, however, the toggling is independent of the state of the CSBI pin. See Figure 6.

When the MMB pin is low, all the device configuration values are reset to the default states shown in Table 12. When MMB is held low the VUV, VOV, and CDC register values are ignored. Instead VUV and VOV use factory-programmed setings. CDC is set to state 5. The number of cells to be monitored is set by the logic levels on the WDTB and GPIO pins, as shown in Table 1.

APPLICATIONS INFORMATION

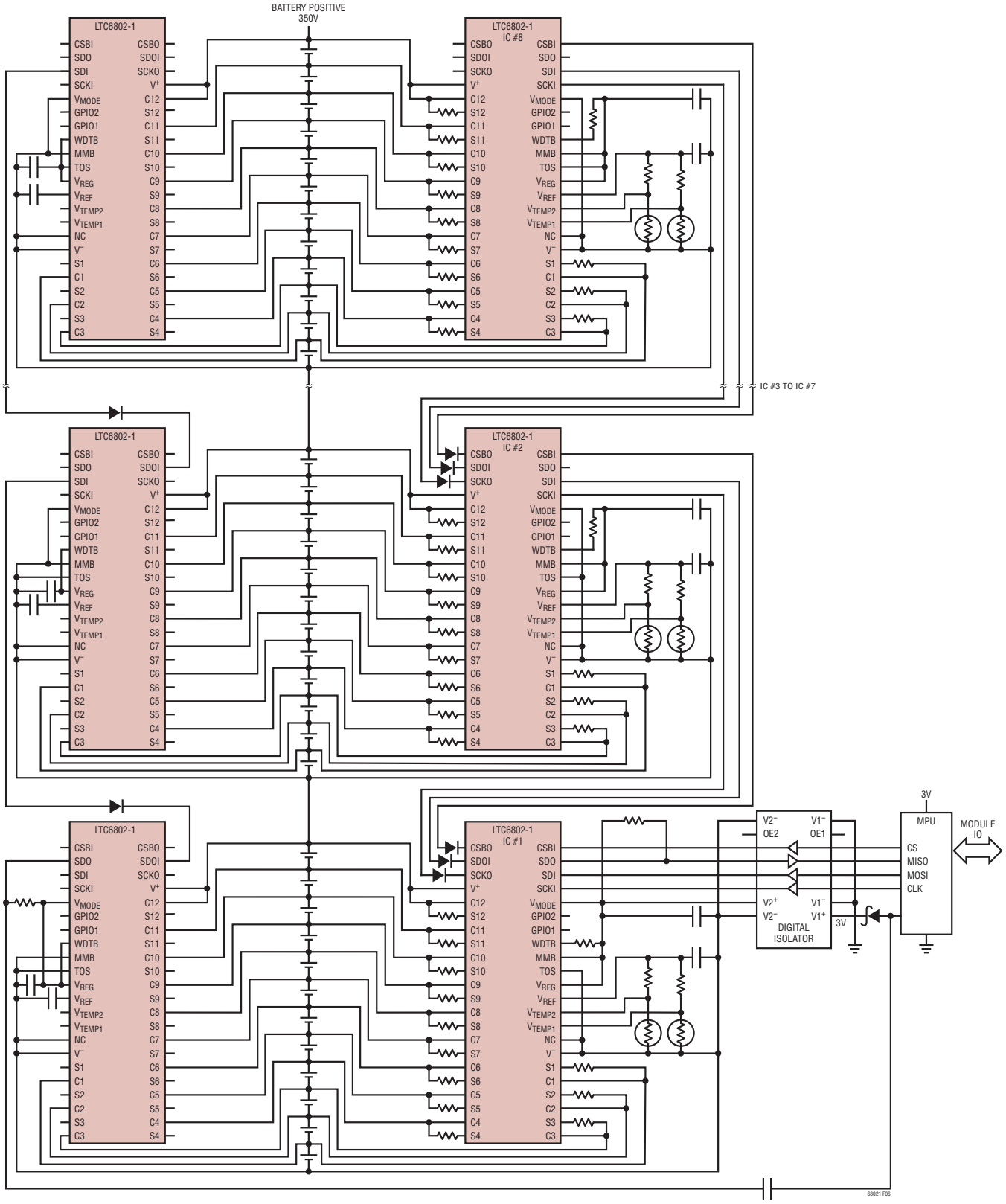


Figure 6. Redundant Monitoring Circuit. This is a Simplified Schematic to Show the General Architecture

APPLICATIONS INFORMATION

Table 1. Monitor Mode Cell Selection

WDTB	GPIO2	GPIO1	CELL INPUTS MONITORED
0	0	0	Cells 1 to 5
0	0	1	Cells 1 to 6
0	1	0	Cells 1 to 7
0	1	1	Cells 1 to 8
1	0	0	Cells 1 to 9
1	0	1	Cells 1 to 10
1	1	0	Cells 1 to 11
1	1	1	Cells 1 to 12

If MMB is low then brought high, all device configuration values are reset to the default states including the VUV, VOV, and CDC configuration bits.

SERIAL PORT

Overview

The LTC6802-1 has an SPI bus compatible serial port. Several devices can be daisy chained in series.

There are two sets of serial port pins, designated as low side and high side. The low side and high side ports enable devices to be daisy chained even when they operate at different power supply potentials. In a typical configuration, the positive power supply of the first, bottom device is connected to the negative power supply of the second, top device, as shown in Figure 1. When devices are stacked in this manner, they can be daisy chained by connecting the high side port of the bottom device to the low side port of the top device. With this arrangement, the master writes to or reads from the cascaded devices as if they formed one long shift register. The LTC6802-1 translates the voltage level of the signals between the low side and high side ports to pass data up and down the battery stack.

Physical Layer

On the LTC6802-1, seven pins comprise the low side and high side ports. The low side pins are CSBI, SCKI, SDI, and SDO. The high side pins are CSBO, SCKO and SDOI. CSBI and SCKI are always inputs, driven by the master or by the next lower device in a stack. CSBO and SCKO are always outputs that can drive the next higher device in a stack. SDI is a data input when writing to a stack of devices. For devices not at the bottom of a stack, SDI is a data output when reading from the stack. SDOI is a data output when writing to and a data input when reading from a stack of devices. SDO is an open drain output that is only used on the bottom device of a stack, where it may be tied with SDI, if desired, to form a single, bi-directional port. The SDO pin on the bottom device of a stack requires a pull-up resistor. For devices up in the stack, SDO should be tied to the local V^- or left floating.

To communicate between daisy-chained devices, the high side port pins of a lower device (CSBO, SCKO, and SDOI) must be connected through PN junction diodes to the respective low side port pins of the next higher device (CSBI, SCKI, and SDI). In this configuration, the devices communicate using current rather than voltage. To signal a logic high from the lower device to the higher device, the lower device sinks a smaller current from the higher device pin. To signal a logic low, the lower device sinks a larger current. Likewise, to signal a logic high from the higher device to the lower device, the higher device sources a larger current to the lower device pin. To signal a logic low, the higher device sources a smaller current. See Figure 7.

Standby current consumed in the current mode serial interface is minimized when CSBI, SCKI, and SDI are all high.

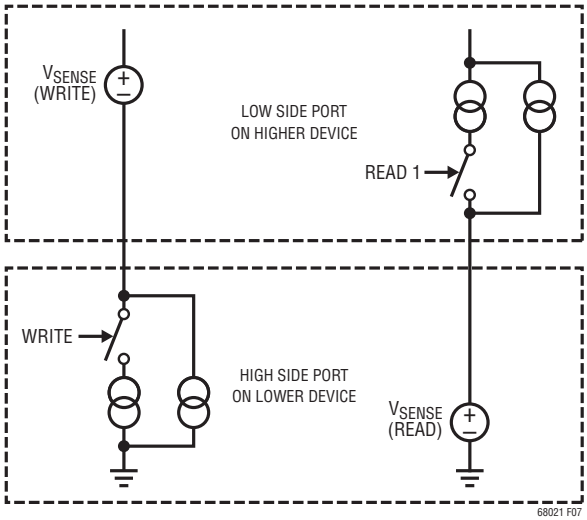


Figure 7. Current Mode Interface

APPLICATIONS INFORMATION

The voltage mode pin (V_{MODE}) determines whether the low side serial port is configured as voltage mode or current mode. For the bottom device in a daisy-chain stack, this pin must be pulled high (tied to V_{REG}). The other devices in the daisy chain must have this pin pulled low (tied to V^-) to designate current mode communication. To designate the top-of-stack device for polling commands, the TOS pin on the top device of a daisy chain must be tied high. The other devices in the stack must have TOS tied low. See Figure 1.

Data Link Layer

Clock Phase And Polarity: The LTC6802-1 SPI-compatible interface is configured to operate in a system using CPHA=1 and CPOL=1. Consequently, data on SDI must be stable during the rising edge of SCKI.

Data Transfers: Every byte consists of 8 bits. Bytes are transferred with the most significant bit (MSB) first. On a write, the data value on SDI is latched into the device on the rising edge of SCKI (Figure 8). Similarly, on a read, the data value output on SDO is valid during the rising edge of SCKI and transitions on the falling edge of SCKI (Figure 9).

CSBI must remain low for the entire duration of a command sequence, including between a command byte and subsequent data. On a write command, data is latched in on the rising edge of CSBI.

After a polling command has been entered, the SDO output will immediately be driven by the polling state, with the SCKI input ignored (Figure 10). See the Toggle Polling and Level Polling sections.

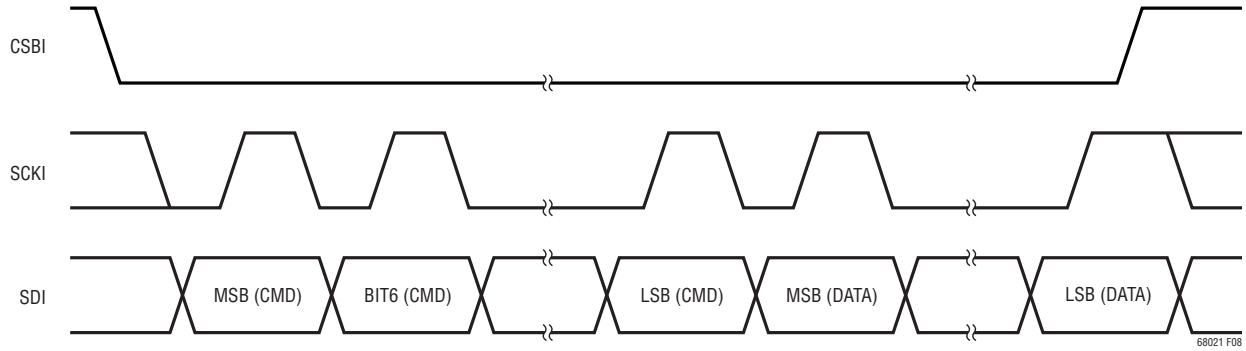


Figure 8. Transmission Format (Write)

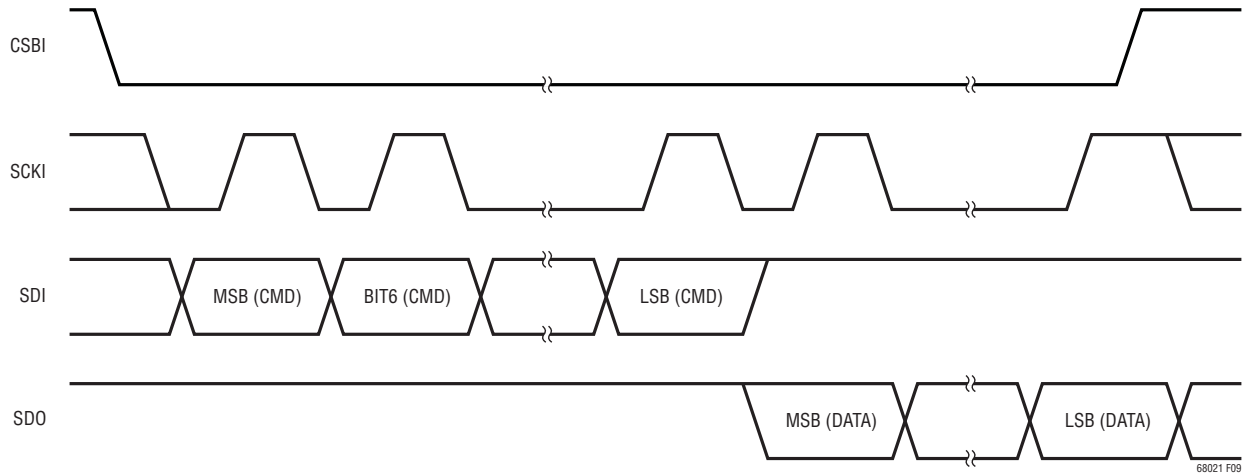


Figure 9. Transmission Format (Read)

APPLICATIONS INFORMATION

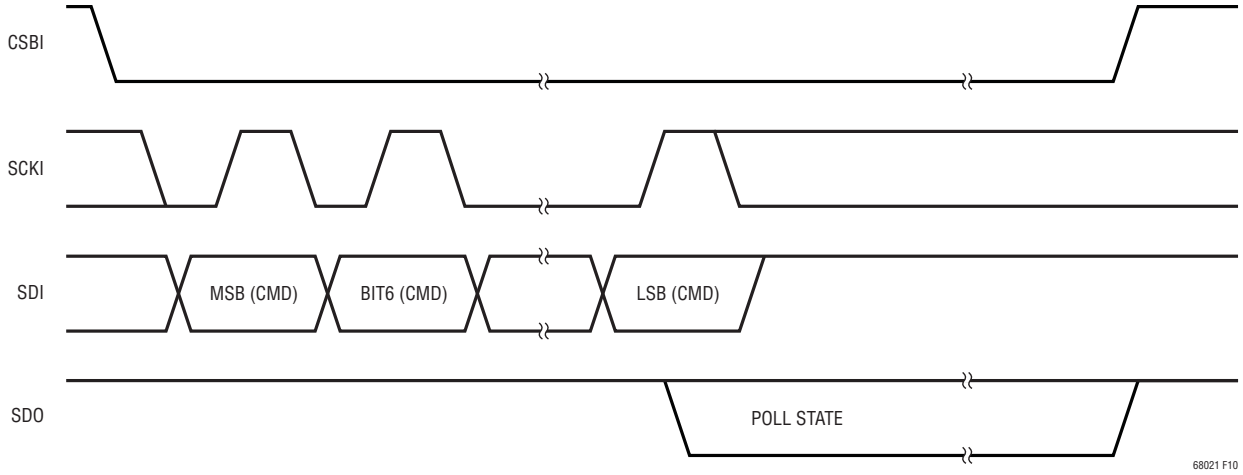


Figure 10. Transmission Format (Poll)

Network Layer

Broadcast Commands: A broadcast command is one to which all devices on the bus will respond. See the Bus Protocols and Commands sections.

In daisy chained configurations, all devices in the chain receive the command bytes simultaneously. For example, to initiate A/D conversions in a stack of devices, a single STCVAD command byte is sent, and all devices will start conversions at the same time. For read and write commands, a single command byte is sent, and then the stacked devices effectively turn into a cascaded shift register, in which data is shifted through each device to the next higher (on a write) or the next lower (on a read) device in the stack. See the Serial Command Examples section.

PEC Byte: The Packet Error Code (PEC) byte is a CRC value calculated for all of the bits in a register group in the order they are read, using the following characteristic polynomial:

$$x^8 + x^2 + x + 1$$

On a read command, after sending the last byte of a register group, the device will shift out the calculated PEC, MSB first. For daisy-chained devices, after the PEC is read from the first device, the data from any daisy-chained devices will follow in the same order. For example, when reading the flag registers from two stacked devices (bottom device A and top device B), the data will be output in the following order:

FLGR0(A), FLGR1(A), FLGR2(A), PEC(A), FLGR0(B), FLGR1(B), FLGR2(B), PEC(B)

Toggle Polling: Toggle polling allows a robust determination both of device states and of the integrity of the connections between the devices in a stack. Toggle polling is enabled when the LVLPL bit is low. After entering a polling command, the data out line will be driven by the slave devices based on their status. When polling for the A/D converter status, data out will be low when any device is busy performing an A/D conversion and will toggle at 1kHz when no device is busy. Similarly, when polling for interrupt status, the output will be low when any device has an interrupt condition and will toggle at 1kHz when none has an interrupt condition.

Toggle Polling—Daisy-Chained Broadcast Polling: The SDO pin (bottom device) or SDI pin (stacked devices) will be low if a device is busy/in interrupt. If it is not busy/not in interrupt, the device will pass the signal from the SDOI input to data out (if not the top-of-stack device) or toggle the data out line at 1kHz (if the top-of-stack device).

The master pulls CSBI high to exit polling.

Level polling: Level polling is enabled when the LVLPL bit is high. After entering a polling command, the data out line will be driven by the slave devices based on their status. When polling for the A/D converter status, data

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out will be low when any device is busy performing an A/D conversion and will be high when no device is busy. Similarly, when polling for interrupt status, the output will be low when any device has an interrupt condition and will be high when none has an interrupt condition.

Level polling—Daisy-Chained Broadcast Polling: The SDO pin (bottom device) or SDI pin (stacked devices) will be low if a device is busy/in interrupt. If it is not busy/not in interrupt, the device will pass the level from the SDOI input to data out (if not the top-of-stack device) or hold the data out line high (if the top-of-stack device). Therefore, if any device in the chain is busy or in interrupt, the SDO signal at the bottom of the stack will be low. If all devices are not busy/not in interrupt, the SDO signal at the bottom of the stack will be high.

The master pulls CSBI high to exit polling.

Polling Methods: For A/D conversions, three methods can be used to determine A/D completion. First, a controller can start an A/D conversion and wait for the specified conversion time to pass before reading the results. The second method is to hold CSBI low after an A/D start command has been sent. The A/D conversion status will be output on SDO. A problem with the second method is that the controller is not free to do other serial communication while waiting for A/D conversions to complete. The third method overcomes this limitation. The controller can send an A/D start command, perform other tasks, and then send a Poll A/D Converter Status (PLADC) command to determine the status of the A/D conversions.

For OV/UV interrupt status, the Poll Interrupt Status (PLINT) command can be used to quickly determine whether any cell in a stack is in an overvoltage or undervoltage condition.

Bus Protocols

There are 3 different protocol formats, depicted in Table 3 through Table 5. Table 2 is the key for reading the protocol diagrams.

Table 2. Protocol Key

PEC		Packet error code (CRC-8)			Master-to-slave
N		Number of bits			Slave-to-master
…		Continuation of protocol			Complete byte of data

Table 3. Broadcast Poll Command

8	
Command	Poll Data

Table 4. Broadcast Read

8	*8*		*8*	*8*	*8*		*8*
Command	Data Byte Low	…	Data Byte High	PEC	Shift Byte 1	…	Shift Byte N

Table 5. Broadcast Write

8	*8*		*8*	*8*		*8*
Command	Data Byte Low	…	Data Byte High	Shift Byte 1	…	Shift Byte N

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Commands

Table 6. Command Codes

Write Configuration Register Group	WRCFG	0x01
Read Configuration Register Group	RDCFG	0x02
Read Cell Voltage Register Group	RDCV	0x04
Read Flag Register Group	RDFLG	0x06
Read Temperature Register Group	RDTMP	0x08
Start Cell Voltage A/D Conversions and Poll Status	STCVAD	0x10 (all cell voltage inputs) 0x11 (cell 1 only) 0x12 (cell 2 only) … 0x1A (cell 10 only) 0x1B (cell 11 only, if CELL10 bit=0) 0x1C (cell 12 only, if CELL10 bit=0) 0x1D (unused) 0x1E (cell self test 1; all CV=0x555) 0x1F (cell self test 2; all CV=0xAAA)
Start Open Wire A/D Conversions and Poll Status	STOWAD	0x20 (all cell voltage inputs) 0x21 (cell 1 only) 0x22 (cell 2 only) … 0x2A (cell 10 only) 0x2B (cell 11 only, if CELL10 bit=0) 0x2C (cell 12 only, if CELL10 bit=0) 0x2D (unused) 0x2E (cell self test 1; all CV=0x555) 0x2F (cell self test 2; all CV=0xAAA)
Start Temperature A/D Conversions and Poll Status	STTMPAD	0x30 (all temperature inputs) 0x31 (external temp 1 only) 0x32 (external temp 2 only) 0x33 (internal temp only) 0x34—0x3D (unused) 0x3E (temp self test 1; all TMP=0x555) 0x3F (temp self test 2; all TMP=0xAAA)
Poll A/D Converter Status	PLADC	0x40
Poll Interrupt Status	PLINT	0x50
Start Cell Voltage A/D Conversions and Poll Status, with Discharge Permitted	STCVDC	0x60 (all cell voltage inputs) 0x61 (cell 1 only) 0x62 (cell 2 only) … 0x6A (cell 10 only) 0x6B (cell 11 only, if CELL10 bit=0) 0x6C (cell 12 only, if CELL10 bit=0) 0x6D (unused) 0x6E (cell self test 1; all CV=0x555) 0x6F (cell self test 2; all CV=0xAAA)
Start Open Wire A/D Conversions and Poll Status, with Discharge Permitted	STOWDC	0x70 (all cell voltage inputs) 0x71 (cell 1 only) 0x72 (cell 2 only) … 0x7A (cell 10 only) 0x7B (cell 11 only, if CELL10 bit=0) 0x7C (cell 12 only, if CELL10 bit=0) 0x7D (unused) 0x7E (cell self test 1; all CV=0x555) 0x7F (cell self test 2; all CV=0xAAA)

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Memory Map

Table 7 through Table 12 show the memory map for the LTC6802-1. Table 12 gives bit descriptions.

Table 7. Configuration (CFG) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGR0	RD/WR	WDT	GPIO2	GPIO1	LVLPL	CELL10	CDC[2]	CDC[1]	CDC[0]
CFGR1	RD/WR	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGR2	RD/WR	MC4I	MC3I	MC2I	MC1I	DCC12	DCC11	DCC10	DCC9
CFGR3	RD/WR	MC12I	MC11I	MC10I	MC9I	MC8I	MC7I	MC6I	MC5I
CFGR4	RD/WR	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGR5	RD/WR	VOV[7]	VOV[6]	VOV[5]	VOV[4]	VOV[3]	VOV[2]	VOV[1]	VOV[0]

Table 8. Cell Voltage (CV) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVR00	RD	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
CVR01	RD	C2V[3]	C2V[2]	C2V[1]	C2V[0]	C1V[11]	C1V[10]	C1V[9]	C1V[8]
CVR02	RD	C2V[11]	C2V[10]	C2V[9]	C2V[8]	C2V[7]	C2V[6]	C2V[5]	C2V[4]
CVR03	RD	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
CVR04	RD	C4V[3]	C4V[2]	C4V[1]	C4V[0]	C3V[11]	C3V[10]	C3V[9]	C3V[8]
CVR05	RD	C4V[11]	C4V[10]	C4V[9]	C4V[8]	C4V[7]	C4V[6]	C4V[5]	C4V[4]
CVR06	RD	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]
CVR07	RD	C6V[3]	C6V[2]	C6V[1]	C6V[0]	C5V[11]	C5V[10]	C5V[9]	C5V[8]
CVR08	RD	C6V[11]	C6V[10]	C6V[9]	C6V[8]	C6V[7]	C6V[6]	C6V[5]	C6V[4]
CVR09	RD	C7V[7]	C7V[6]	C7V[5]	C7V[4]	C7V[3]	C7V[2]	C7V[1]	C7V[0]
CVR10	RD	C8V[3]	C8V[2]	C8V[1]	C8V[0]	C7V[11]	C7V[10]	C7V[9]	C7V[8]
CVR11	RD	C8V[11]	C8V[10]	C8V[9]	C8V[8]	C8V[7]	C8V[6]	C8V[5]	C8V[4]
CVR12	RD	C9V[7]	C9V[6]	C9V[5]	C9V[4]	C9V[3]	C9V[2]	C9V[1]	C9V[0]
CVR13	RD	C10V[3]	C10V[2]	C10V[1]	C10V[0]	C9V[11]	C9V[10]	C9V[9]	C9V[8]
CVR14	RD	C10V[11]	C10V[10]	C10V[9]	C10V[8]	C10V[7]	C10V[6]	C10V[5]	C10V[4]
CVR15*	RD	C11V[7]	C11V[6]	C11V[5]	C11V[4]	C11V[3]	C11V[2]	C11V[1]	C11V[0]
CVR16*	RD	C12V[3]	C12V[2]	C12V[1]	C12V[0]	C11V[11]	C11V[10]	C11V[9]	C11V[8]
CVR17*	RD	C12V[11]	C12V[10]	C12V[9]	C12V[8]	C12V[7]	C12V[6]	C12V[5]	C12V[4]

*Registers CVR15, CVR16, and CVR17 can only be read if the CELL10 bit in register CFGR0 is low

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Table 9. Flag (FLG) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLGR0	RD	C4OV	C4UV	C3OV	C3UV	C2OV	C2UV	C1OV	C1UV
FLGR1	RD	C8OV	C8UV	C7OV	C7UV	C6OV	C6UV	C5OV	C5UV
FLGR2	RD	C12OV*	C12UV*	C11OV*	C11UV*	C10OV	C10UV	C9OV	C9UV

* Bits C11UV, C12UV, C11OV, and C12OV are always low if the CELL10 bit in register CFGR0 is high

Table 10. Temperature (TMP) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMPR0	RD	ETMP1[7]	ETMP1[6]	ETMP1[5]	ETMP1[4]	ETMP1[3]	ETMP1[2]	ETMP1[1]	ETMP1[0]
TMPR1	RD	ETMP2[3]	ETMP2[2]	ETMP2[1]	ETMP2[0]	ETMP1[11]	ETMP1[10]	ETMP1[9]	ETMP1[8]
TMPR2	RD	ETMP2[11]	ETMP2[10]	ETMP2[9]	ETMP2[8]	ETMP2[7]	ETMP2[6]	ETMP2[5]	ETMP2[4]
TMPR3	RD	ITMP[7]	ITMP[6]	ITMP[5]	ITMP[4]	ITMP[3]	ITMP[2]	ITMP[1]	ITMP[0]
TMPR4	RD	REV[2]	REV[1]	REV[0]	THSD	ITMP[11]	ITMP[10]	ITMP[9]	ITMP[8]

Table 11. Packet Error Code (PEC)

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PEC	RD	PEC[7]	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]

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Table 12. Memory Bit Descriptions

NAME	DESCRIPTION	VALUES			
CDC	Comparator Duty Cycle	CDC	UV/OV COMPARATOR PERIOD	V_{REF} POWERED DOWN BETWEEN MEASUREMENTS	CELL VOLTAGE MEASUREMENT TIME
		0 (default)	N/A (Comparator Off) Standby Mode	Yes	N/A
		1	N/A (Comparator Off)	No	13ms
		2	13ms	No	13ms
		3	130ms	No	13ms
		4	500ms	No	13ms
		5*	130ms	Yes	21ms
		6	500ms	Yes	21ms
		7	2000ms	Yes	21ms
		*when MMB pin is low, the CDC value is set to 5			
CELL10	10-Cell Mode	0=12-cell mode (default); 1=10-cell mode			
LVLPL	Level Polling Mode	0=toggle polling (default); 1=level polling			
GPIO1	GPIO1 Pin Control	Write: 0=GPIO1 pin pull down on; 1=GPIO1 pin pull down off (default) Read: 0=GPIO1 pin at logic '0'; 1=GPIO1 pin at logic '1'			
GPIO2	GPIO2 Pin Control	Write: 0=GPIO2 pin pull down on; 1=GPIO2 pin pull down off (default) Read: 0=GPIO2 pin at logic '0'; 1=GPIO2 pin at logic '1'			
WDT	Watchdog Timer	Read Only: 0=WDTB pin at logic '0'; 1=WDTB pin at logic '1'			
DCCx	Discharge Cell x	x=1..12 0=turn off shorting switch for cell 'x' (default); 1=turn on shorting switch			
VUV	Undervoltage Comparison Voltage*	Comparison voltage = VUV * 16 * 1.5mV (default VUV=0. When MMB pin is low a factory programmed comparison voltage is used)			
VOV	Overvoltage Comparison Voltage*	Comparison voltage = VOV * 16 * 1.5mV (default VOV=0. When MMB pin is low a factory programmed comparison voltage is used)			
MCxI	Mask Cell x Interrupts	x=1..12 0=enable interrupts for cell 'x' (default) 1=turn off interrupts and clear flags for cell 'x'			
CxV	Cell x Voltage*	x=1..12 12-bit ADC measurement value for cell 'x' cell voltage for cell 'x' = CxV * 1.5mV reads as 0xFFF while A/D conversion in progress			
CxUV	Cell x Undervoltage Flag	x=1..12 cell voltage compared to VUV comparison voltage 0=cell 'x' not flagged for under voltage condition; 1=cell 'x' flagged			
CxOV	Cell x Overvoltage Flag	x=1..12 cell voltage compared to VOV comparison voltage 0=cell 'x' not flagged for over voltage condition; 1=cell 'x' flagged			
ETMPx	External Temperature Measurement*	Temperature measurement voltage = ETMPx * 1.5mV			
THSD	Thermal Shutdown Status	0= thermal shutdown has not occurred; 1=thermal shutdown has occurred Status cleared to '0' on read of Thermal Register Group			
REV	Revision Code	Device revision code			
ITMP	Internal Temperature Measurement*	Temperature measurement voltage = ITMP * 1.5mV = 8mV * T(°K)			
PEC	Packet Error Code	CRC value for reads			

*Voltage determinations use the decimal value of the registers, 0 to 4095 for 12-bit and 0 to 255 for 8-bit registers

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SERIAL COMMAND EXAMPLES

LTC6802-1 (Daisy Chained Configuration)

Examples below use a configuration of three stacked devices: bottom (B), middle (M), and top (T)

Write Configuration Registers

1. Pull CSBI low
2. Send WRCFG command byte
3. Send CFGR0 byte for top device, then CFGR1 (T), CFGR2 (T), … CFGR5 (T)
4. Send CFGR0 byte for middle device, then CFGR1 (M), CFGR2 (M), … CFGR5 (M)
5. Send CFGR0 byte for bottom device, then CFGR1 (B), CFGR2 (B), … CFGR5 (B)
6. Pull CSBI high; data latched into all devices on rising edge of CSBI

Calculation of serial interface time for sequence above:

Number of devices in stack= N
Number of bytes in sequence = B = 1 command byte and 6 data bytes per device = 1+6*N
Serial port frequency per bit = F
Time = (1/F) * B * 8 bits/byte = (1/F) * (1+6*N) * 8
Time for 3 cell-stacks example above, with 1MHz serial port = (1/1000000) * (1+6*3)*8 = 152us

Read Cell Voltage Registers (12 Cell Mode)

1. Pull CSBI low
2. Send RDCV command byte
3. Read CVR00 byte of bottom device, then CVR01 (B), CVR02 (B), … CVR17 (B), and then PEC (B)
4. Read CVR00 byte of middle device, then CVR01 (M), CVR02 (M), … CVR17 (M), and then PEC (M)
5. Read CVR00 byte for top device, then CVR01 (T), CVR02 (T), … CVR17 (T), and then PEC (T)
6. Pull CSBI high

Calculation of serial interface time for sequence above:

Number of devices in stack= N
Number of bytes in sequence = B = 1 command byte, and 18 data bytes plus 1 PEC byte per device = 1+19*N
Serial port frequency per bit = F
Time = (1/F) * B * 8 bits/byte = (1/F) * (1+19*N) * 8
Time for 3-cell example above, with 1MHz serial port = (1/1000000) * (1+19*3)*8 =464us

Start Cell Voltage A/D Conversions and Poll Status (Toggle Polling)

1. Pull CSBI low
2. Send STCVAD command byte (all devices in stack start A/D conversions simultaneously)
3. SDO output from bottom device pulled low for approximately 12ms
4. SDO output toggles at 1kHz rate, indicating conversions complete for all devices in daisy chain
5. Pull CSBI high to exit polling

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Poll Interrupt Status (Level Polling)

1. Pull CSBI low
2. Send PLINT command byte
3. SDO output from bottom device pulled low if any device has an interrupt condition; otherwise, SDO high
4. Pull CSBI high to exit polling

FAULT PROTECTION

Overview

Care should always be taken when using high energy sources such as batteries. There are numerous ways that systems can be [mis-]configured that might affect a battery system during its useful lifespan. Table 13 shows the various situations that should be considered when planning protection circuitry. The first five scenarios are to be anticipated during production and appropriate protection is included within the LTC6802-1 device itself.

Table 13. LTC6802-1 Failure Mechanism Effect Analysis

SCENARIO	EFFECT	DESIGN MITIGATION
Cell input open-circuit (random)	Power-up sequence at IC inputs	Clamp diodes at each pin to V^+ & V^- (within IC) provide alternate power-path.
Cell input open-circuit (random)	Differential input voltage overstress	Zener diodes across each cell voltage input pair (within IC) limits stress.
Top cell input connection loss (V^+)	Power will come from highest connected cell input or via data port fault current	Clamp diodes at each pin to V^+ & V^- (within IC) provide alternate power-path. Diode conduction at data ports will impair communication with higher-potential units.
Bottom cell input connection loss (V^-)	Power will come from lowest connected cell input or via data port fault current	Clamp diodes at each pin to V^+ & V^- (within IC) provide alternate power-path. Diode conduction at data ports will impair communication with higher-potential units.
Disconnection of a harness between a group of battery cells and the IC (in a system of stacked groups)	Loss of supply connection to the IC	Clamp diodes at each pin to V^+ & V^- (within IC) provide an alternate power-path if there are other devices (which can supply power) connected to the LTC6802-1. Diode conduction at data ports will impair communication with higher-potential units.
Data link disconnection between stacked LTC6802-1 units.	Break of "daisy chain" communication (no stress to ICs). Communication will be lost to devices above the disconnection. The devices below the disconnection are still able to communicate and perform all functions, however, the polling feature is disabled.	All units above the disconnection will enter standby mode within 2 seconds of disconnect. Discharge switches are disabled in standby mode.
Cell-pack integrity, break between stacked units	Daisy-chain voltage reversal up to full stack potential during pack discharge	Use series protection diodes with top-port I/O connections (RS07J for up to 600V). Use isolated data link at bottom-most data port.
Cell-pack integrity, break between stacked units	Daisy-chain positive overstress during charging	Add redundant current path link
Cell-pack integrity, break within stacked unit	Cell input reverse overstress during discharge	Add parallel Schottky diodes across each cell for load-path redundancy. Diode and connections must handle full operating current of stack, will limit stress on IC
Cell-pack integrity, break within stacked unit	Cell input positive overstress during charge	Add SCR across each cell for charge-path redundancy. SCR and connections must handle full charging current of stack, will limit stress on IC by selection of trigger Zener

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Battery Interconnection Integrity

The FMEA scenarios that are potentially most damaging are those that involve a break in the stack of battery cells. When the battery stack has a discontinuity between groupings of cells monitored by LTC6802-1 ICs, any load will force a large reverse potential on the daisy-chain connection. This situation might occur in a modular battery system during initial installation or a service procedure. The daisy chain ports are protected from the reverse potential in this scenario by external series high-voltage diodes required in the upper-port data connections as shown in Figure 11.

During the charging phase of operation, this fault would lead to forward biasing of daisy-chain ESD clamps that would also lead to part damage. An alternative connection to carry current during this scenario will avoid this stress from being applied (Figure 11).

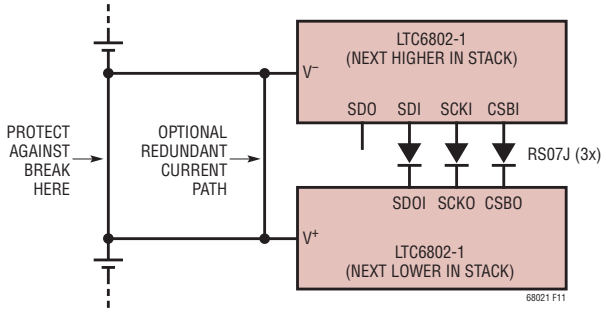

Figure 11. Reverse-Voltage Protection for the Daisy-Chain (One Link Connection Shown)

Internal Protection Diodes

Each pin of the LTC6802-1 has protection diodes to help prevent damage to the internal device structures caused by external application of voltages beyond the supply rails as shown in Figure 12.

The diodes shown are conventional silicon diodes with a forward breakdown voltage of 0.5V. The unlabeled zener diode structures have a reverse breakdown characteristic which initially breaks down at 12V then snaps back to a 7V clamping potential. The Zener diodes labeled ZCLAMP are higher voltage devices with an initial reverse breakdown of 30V snapping back to 25V. The forward voltage drop of all Zeners is 0.5V. Refer to this diagram in the event of unpredictable voltage clamping or current flow. Limiting the current flow at any pin to ±10mA will prevent damage to the IC.

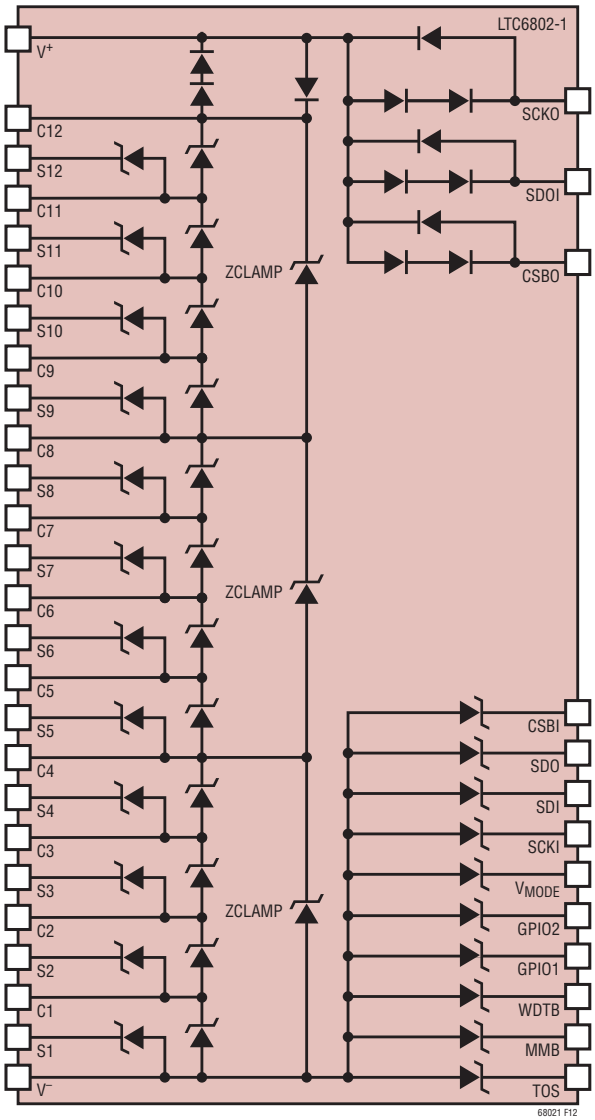

Figure 12. Internal Protection Diodes

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Cell-Voltage Filtering

The LTC6802-1 employs a sampling system to perform its analog-to-digital conversions and provides a conversion result that is essentially an average over the 0.5ms conversion window, provided there isn't noise aliasing with respect to the delta-sigma modulator rate of 512kHz. This indicates that a lowpass filter with useful attenuation at 500kHz may be beneficial. Since the delta-sigma integration bandwidth is about 1kHz, the filter corner need not be lower than this to assure accurate conversions.

Series resistors of 100Ω may be inserted in the input paths without introducing meaningful measurement error, provided only external discharge switch FETs are being used. Shunt capacitors may be added from the cell inputs to V^-, creating RC filtering as shown in Figure 13. Note that this filtering is not compatible with use of the internal discharge switches to carry current since this would induce settling errors at the time of conversion as any activated switches temporarily open to provide Kelvin mode cell sensing. As a discharge switch opens, cell wiring resistance will also form a small voltage step (recovery of the small IR drop), so keeping the frequency cutoff of the filter relatively high will allow adequate settling prior to the actual conversion. A guard time of about 60µs is provided in the ADC timing, so a 16kHz LP is optimal and offers about 30dB of noise rejection.

No resistor should be placed in series with the V^- pin. Because the supply current flows from the V^- pin, any resistance on this pin could generate a significant conversion error for CELL1.

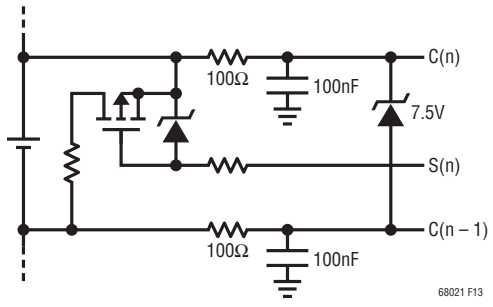

Figure 13. Adding RC Filtering to the Cell Inputs (One Cell Connection Shown)

The V^+ pin is powered from the top cell potential of the monitored cell group. A decoupling network of 20Ω/100nF is recommended.

READING EXTERNAL TEMPERATURE PROBES

Using Dedicated Inputs

The LTC6802-1 includes two channels of ADC input, V_{TEMP1} and V_{TEMP2}, that are intended to monitor thermistors (tempco about –4%/°C generally) or diodes (–2.2mV/°C typical) located within the cell array. Sensors can be powered directly from V_{REF} as shown in Figure 14 (up to 60µA total).

For sensors that require higher drive currents, a buffer op amp may be used as shown in Figure 15. Power for the sensor is actually sourced indirectly from the V_{REG} pin

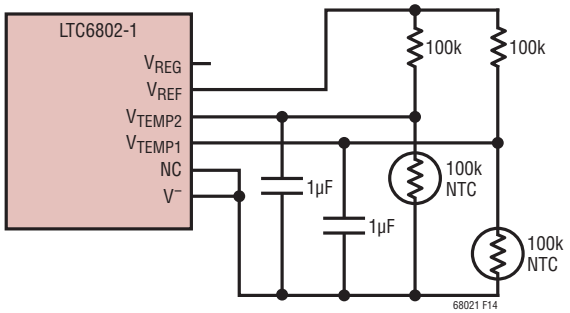

Figure 14. Driving Thermistors Directly from V_{REF}

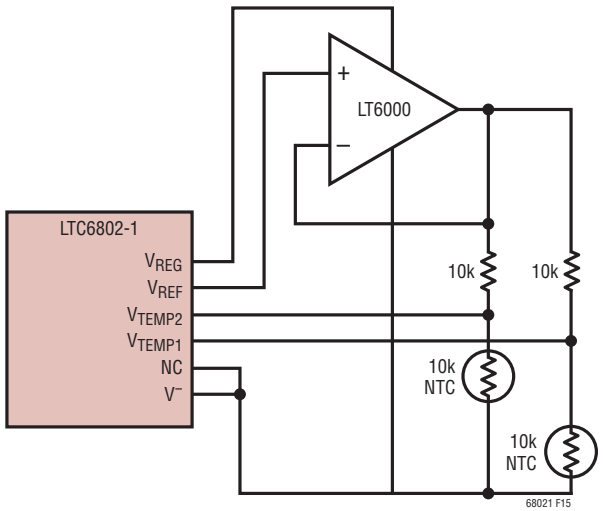

Figure 15. Buffering V_{REF} for Higher-Current Sensors

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in this case. Probe loads up to about 1mA maximum are supported in this configuration. Since V_{REF} is shutdown during the LTC6802-1 idle and shutdown modes, the thermistor drive is also shut off and thus power dissipation minimized. Since V_{REG} remains always on, the buffer op amp (LT6000 shown) is selected for its ultralow power consumption (10µA).

Expanding Probe Count

The LTC6802-1 provides general purpose I/O pins, GPIO1 and GPIO2, that may be used to control multiplexing of several temperature probes. Using just one of the GPIO pins, the sensor count can double to four as shown in Figure 16. Using both GPIO pins, up to eight sensor inputs can be supported.

Using Diodes to Monitor Temperatures in Multiple Locations

Another method of multiple sensor support is possible without the use of any GPIO pins. If the sensors are PN diodes and several used in parallel, then the hottest diode will produce the lowest forward voltage and effectively establish the input signal to the V_{TEMP} input(s). The hottest diode will therefore dominate the readout from the V_{TEMP} inputs that the diodes are connected to. In this scenario, the specific location or distribution of heat is not known, but such information may not be important in practice. Figure 17 shows the basic concept.

In any of the sensor configurations shown, a full-scale cold readout would be an indication of a failed-open sensor connection to the LTC6802-1.

ADDING CALIBRATION AND FULL-STACK MEASUREMENTS

By adding multiplexing hardware, additional signals can be digitized by the CELL1 ADC channel. One useful signal to provide is a high-accuracy voltage reference, such as from an LT1461A-4. By periodic readings of this signal, host software can provide correction of the LTC6802-1 readings to improve the accuracy over that of the internal LTC6802-1 reference, and/or validate ADC operation. Another useful signal is a measure of the total stack potential. This provides a redundant operational measurement of the cells in the event of a malfunction in the normal acquisition process, or as a faster means of monitoring the entire

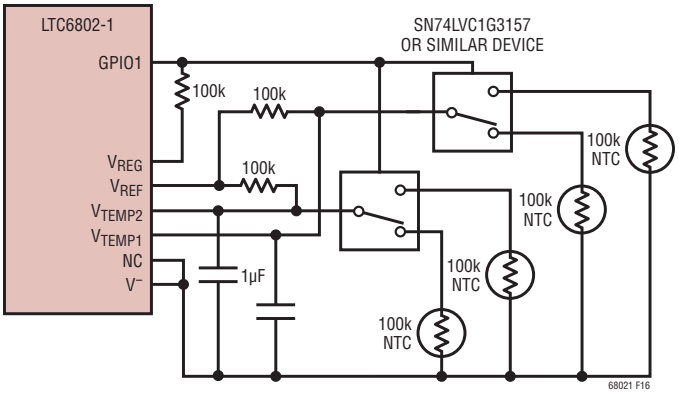


Figure 16. Expanding Sensor Count with Multiplexing

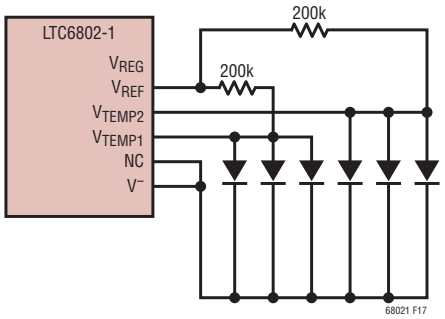


Figure 17. Using Diode Sensors as Hot-Spot Detectors

APPLICATIONS INFORMATION

stack potential. Figure 18 shows a means of providing both of these features. A resistor divider is used to provide a low-voltage representation of the full stack potential (C12 to C0 voltage) with MOSFETs that decouple the divider current under unneeded conditions. Other MOSFETs, in conjunction with an op amp having a shutdown mode, form a voltage selector that allows measurement of the normal cell1 potential (when GPIO1 is low) or a buffered MUX signal. When the MUX is active (GPIO1 is high), selection can be made between the reference (4.096V) or the full-stack voltage divider (GPOI2 set low will select the reference). During idle time when the LTC6802-1 WTB signal goes low, the external circuitry goes into a power down condition, reducing battery drain to a minimum. When not actively performing measurements, GPIO1 should be set low and GPIO2 should be set high to achieve the lowest power state for the configuration shown.

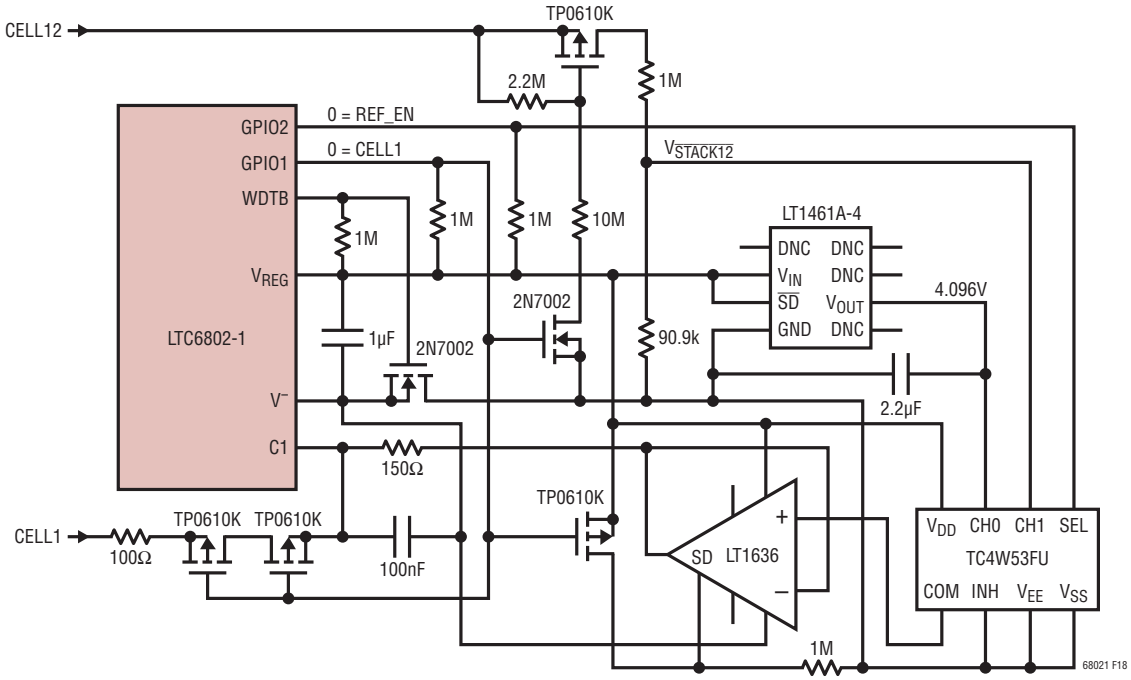


Figure 18. Providing Measurement of Calibration Reference and Full-Stack Voltage Through CELL1 Port

APPLICATIONS INFORMATION

PROVIDING HIGH-SPEED OPTO-ISOLATION OF THE SPI DATA-PORT

Isolation techniques that are capable of supporting the 1Mbps data rate of the LTC6802-1 require more power on the isolated (battery) side than can be furnished by the V_{REG} output of the LTC6802-1. To keep battery drain minimal, this means that a DC/DC function must be implemented along with a suitable data isolation circuit, such as shown in Figure 19. Here an optimal Avago 4-channel (3/1 bidirectional) opto-coupler is used, with a simple isolated supply generated by an LTC1693-2 configured as a 200kHz oscillator. The DC/DC function provides an unregulated logic voltage (~4V) to the opto-coupler isolated side, from energy provided by host-furnished 5V. This circuit provides totally galvanic isolation between the batteries and the host processor, with an insulation rating of 560V continuous, 2500V transient.

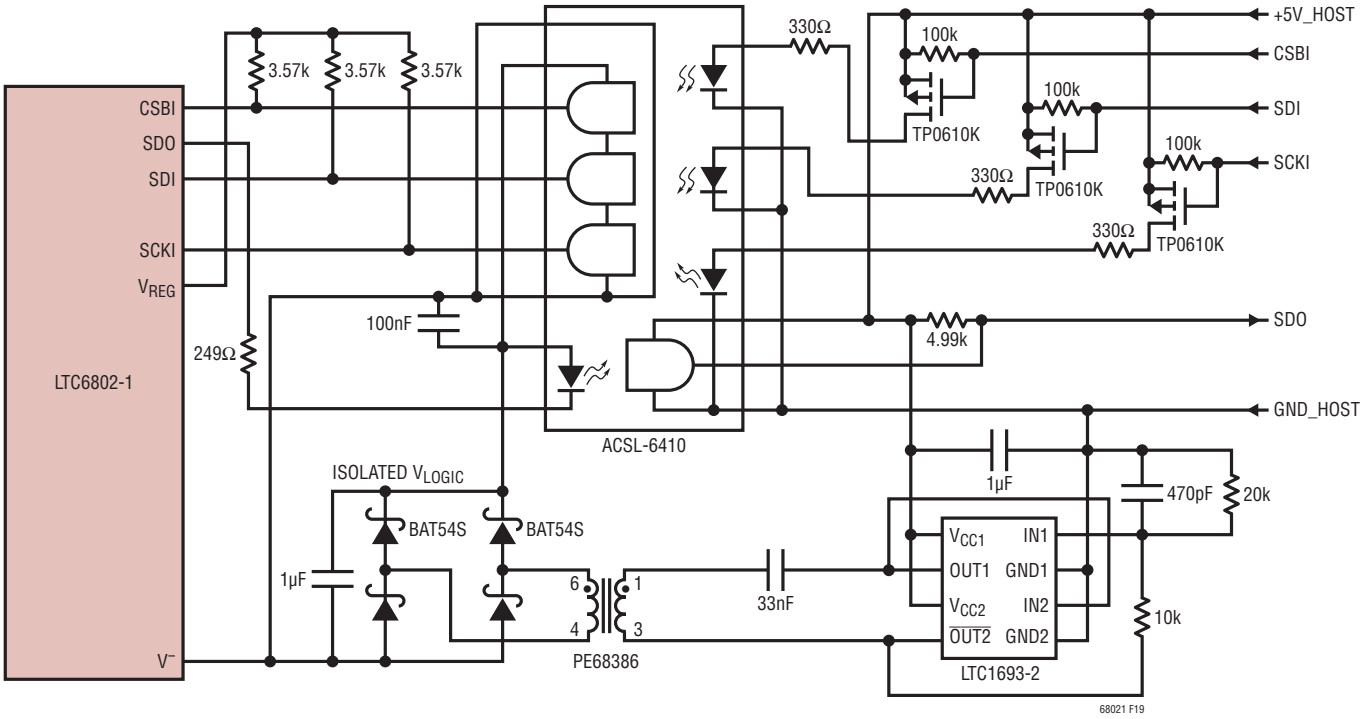


Figure 19. Providing an Isolated High-Speed Data Interface

APPLICATIONS INFORMATION

PCB LAYOUT CONSIDERATIONS

The V_{REG} and V_{REF} pins should be bypassed with a 1µF capacitor for best performance.

The LTC6802-1 is capable of operation with as much as 60V between V^+ and V^-. Care should be taken on the PCB layout to maintain physical separation of traces at different potentials. The pinout of the LTC6802-1 was chosen to facilitate this physical separation. Figure 20 shows the DC voltage on each pin with respect to V^- when twelve 3.6V battery cells are connected to the LTC6802-1. There is no more then 5.5V between any two adjacent pins. The package body is used to separate the highest voltage (43.5V) from the lowest voltage (0V).

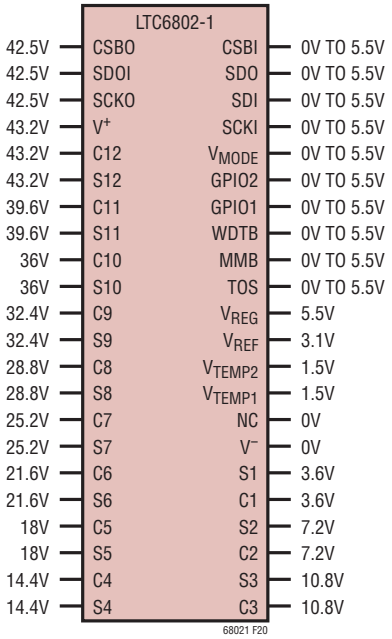


Figure 20. Typical Pin Voltages for 12 3.6V Cells

ADVANTAGES OF DELTA-SIGMA ADCS

The LTC6802-1 employs a delta sigma analog to digital converter for voltage measurement. The architecture of delta sigma converters can vary considerably, but the common characteristic is that the input is sampled many times over the course of a conversion and then filtered or averaged to produce the digital output code. In contrast, a SAR converter takes a single snapshot of the input voltage and then performs the conversion on this single sample. For measurements in a noisy environment, a delta sigma converter provides distinct advantages over a SAR converter.

While SAR converters can have high sample rates, the full-power bandwidth of a SAR converter is often greater than 1MHz, which means the converter is sensitive to noise out to this frequency. And many SAR converters have much higher bandwidths – up to 50MHz and beyond. It is possible to filter the input, but if the converter is multiplexed to measure several input channels a separate filter will be required for each channel. A low frequency filter cannot reside between a multiplexer and an ADC and achieve a high scan rate across multiple channels. Another consequence of filtering a SAR ADC is that any noise reduction gained by filtering the input cancels the benefit of having a high sample rate in the first place, since the filter will take many conversion cycles to settle.

For a given sample rate, a delta sigma converter can achieve excellent noise rejection while settling completely in a single conversion – something that a filtered SAR converter cannot do. Noise rejection is particularly important in high voltage switching controllers, where switching noise will invariably be present in the measured voltage. Other advantages of delta sigma converters are that they are inherently monotonic, meaning they have no missing codes, and they have excellent DC specifications.

APPLICATIONS INFORMATION

Converter Details

The LTC6802-1's ADC has a second order delta sigma modulator followed by a Sinc2, finite impulse response (FIR) digital filter. The front-end sample rate is 512ksps, which greatly reduces input filtering requirements. A simple 16kHz, 1 pole filter composed of a 100Ω resistor and a 0.1µF capacitor at each input will provide adequate filtering for most applications. These component values will not degrade the DC accuracy of the ADC.

Each conversion consists of two phases – an autozero phase and a measurement phase. The ADC is autozeroed at each conversion, greatly improving CMRR. The second half of the conversion is the actual measurement.

Noise Rejection

Figure 21 shows the frequency response of the ADC. The rolloff follows a Sinc2 response, with the first notch at 4kHz. Also shown is the response of a 1 pole, 850Hz filter (187µs time constant) which has the same integrated response to wideband noise as the LTC6802-1's ADC, which is about 1350Hz. This means that if wideband noise is applied to the LTC6802-1 input, the increase in noise seen at the digital output will be the same as an ADC with a wide bandwidth (such as a SAR) preceded by a perfect 1350Hz brickwall lowpass filter.

Thus if an analog filter is placed in front of a SAR converter to achieve the same noise rejection as the LTC6802-1 ADC, the SAR will have a slower response to input signals. For example, a step input applied to the input of the 850Hz filter will take 1.55ms to settle to 12 bits of precision, while the LTC6802-1 ADC settles in a single 1ms conversion cycle. This also means that very high sample rates do not provide any additional information because the analog filter limits the frequency response.

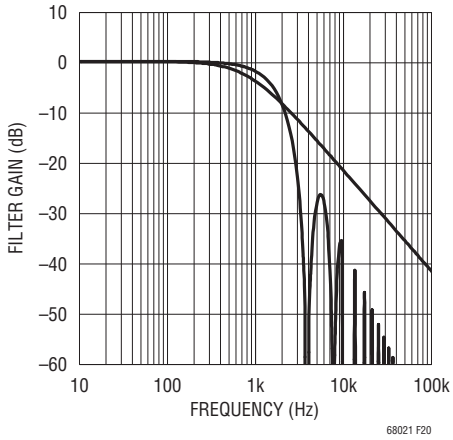


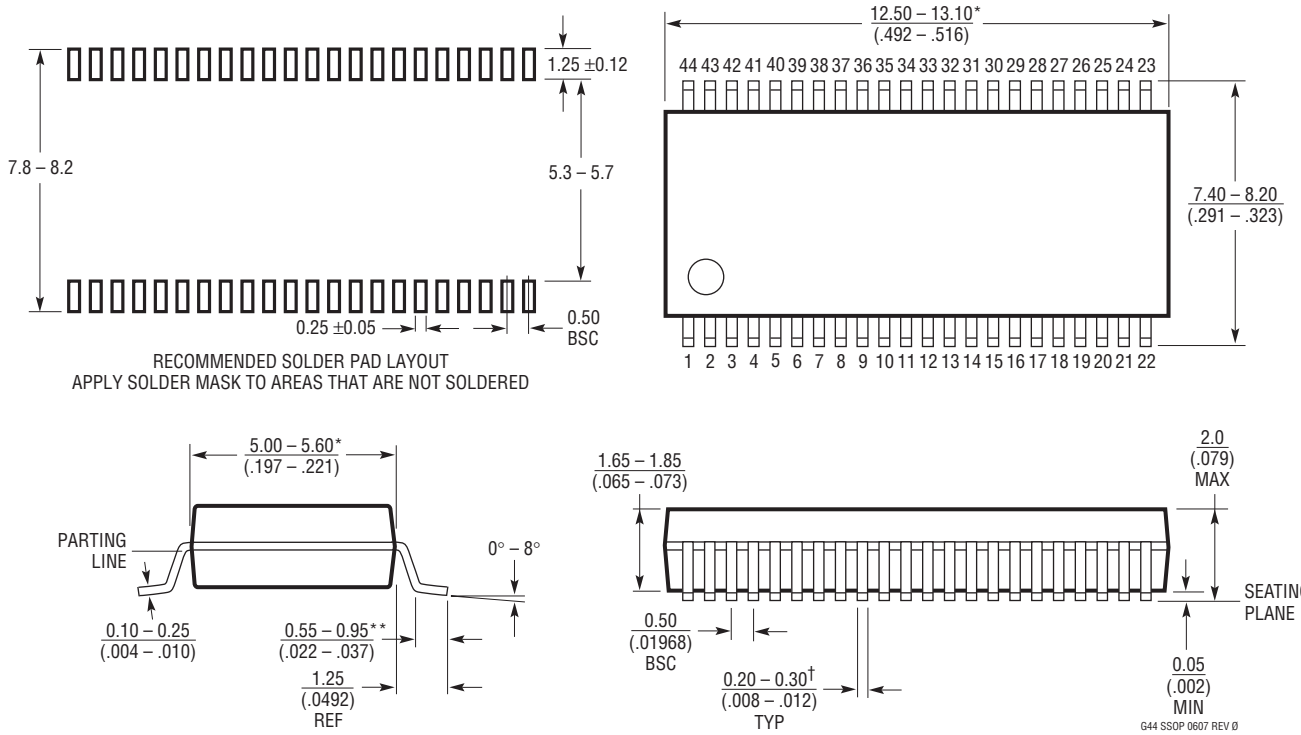
Figure 21. Noise Filtering of the LTC6802-1 ADC

While higher order active filters may provide some improvement, their complexity makes them impractical for high-channel count measurements as a single filter would be required for each input.

Also note that the Sinc2 response has a 2nd order rolloff envelope, providing an additional benefit over a single pole analog filter.

PACKAGE DESCRIPTION

G Package
44-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1754 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC OUTLINE
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
4. DRAWING NOT TO SCALE
5. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH SHALL NOT EXCEED .15mm PER SIDE

**LENGTH OF LEAD FOR SOLDERRING TO A SUBSTRATE

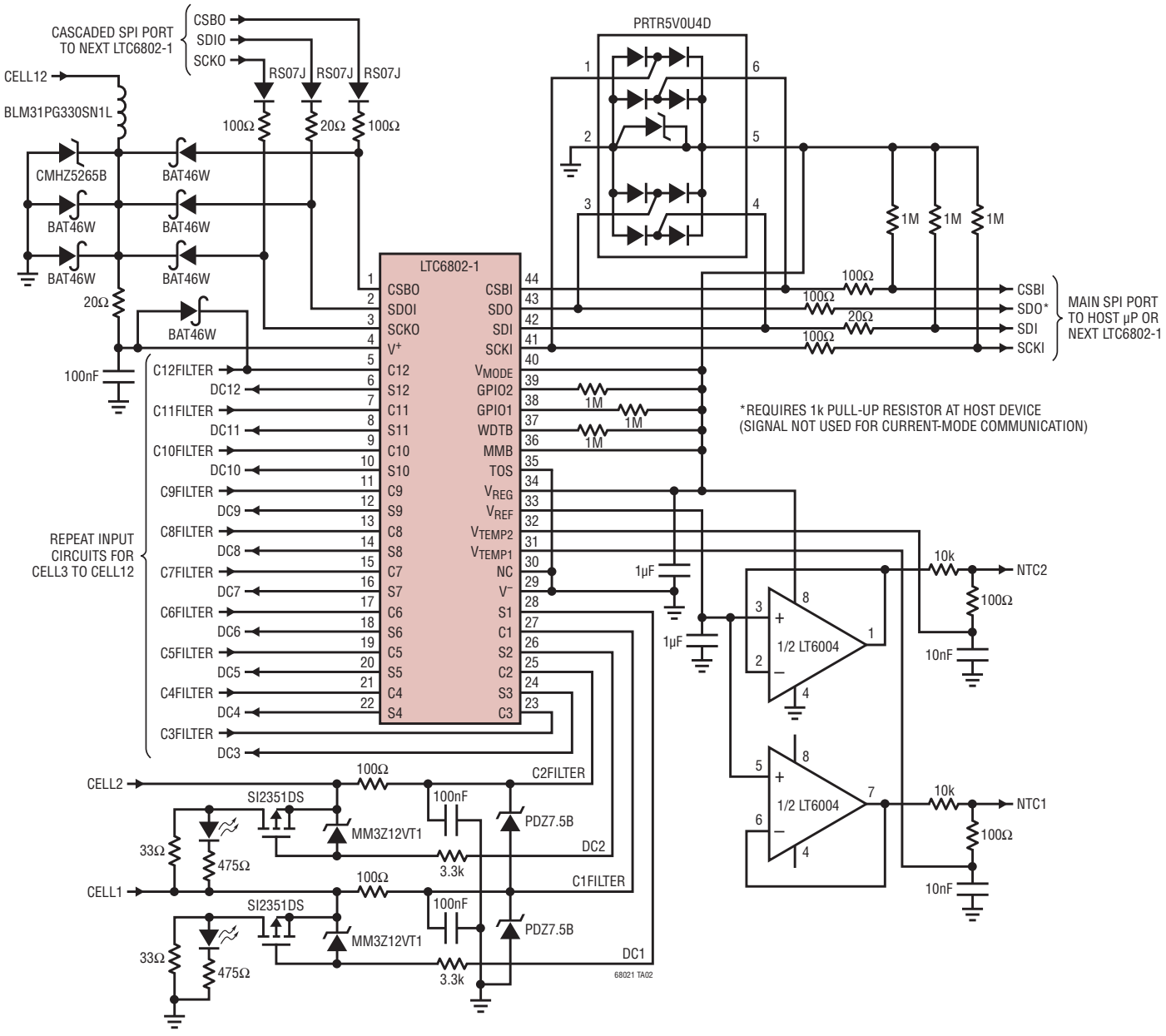
†THE MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS DO NOT EXCEED 0.13mm PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/10	Text Changes to Description	1
		Additions to Absolute Maximum Ratings	2
		Changes to Electrical Characteristics	3, 4
		Changes to Graph G02	5
		Text Changes to Pin Functions	8
		Open Connection Detection Section Replaced	11, 13
		Text Changes to Operation Section	11, 13, 14
		Figures 1, 6 Title Changes	12, 18
		Text Changes to Applications Information Section	16, 28, 29, 30, 31
		Edits to Tables 6, 7, 12, 13	23, 24, 26, 28
		Edit to Figure 12	29
		Edit to Typical Application	38

TYPICAL APPLICATION

Cascadable 12-Cell Li-Ion Battery Monitor



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6802-2	Multicell Battery Stack Monitor with an Individually Addressable Serial Interface	Functionality equivalent to LTC6802-1, Allows for Parallel Communication Battery Stack Topologies

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