SEMICONDUCTOR

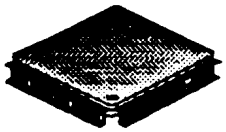
TECHNICAL DATA

DSP56156

Advance Information

16-bit General Purpose Digital Signal Processor

Ceramic Quad Flat Pack (CQFP)
Available in a 112 pin, small footprint, surface mount package.



The DSP56156 is the first member of Motorola's DSP56100 family of HCMOS, low power, 16-bit general purpose Digital Signal Processors (DSP). Designed primarily for speech coding and telecommunications, the DSP56156 has a built-in ΣΔ codec and phase locked loop (PLL). This MPU-style DSP also contains, memories, digital peripherals, and provides a cost effective, high performance solution to many DSP applications. On-Chip Emulation (OnCE™) circuitry provides convenient and inexpensive debug facilities normally available only through expensive external hardware. Development costs are reduced and in-field testing is greatly simplified by using the OnCE. The DSP56156 is an off the shelf part since there are no user programmable ROM's on-chip. The DSP56156ROM is the ROM based version of the DSP56156 which contains a 12K program ROM.

The Central Processing Unit (CPU) consists of three execution units operating in parallel allowing up to six operations to occur in an instruction cycle. This parallelism greatly increases the effective processing speed of the DSP56156. The MPU-style programming model and instruction set allow straightforward generation of efficient, compact code. The basic architectures and development tools of the DSP56100 family, DSP56000 family, and DSP96002 are so similar that learning to design and program one greatly reduces the time needed to learn the others.

DSP56156 Features:

- Up to 30 Million Instructions per Second (MIPS) - 33 ns instruction cycle at 60 MHz.
- Single-cycle 16 x 16-bit parallel multiply-accumulator
- Two 40-bit accumulators including extension byte
- Fractional and integer arithmetic with support for multiprecision arithmetic
- Highly parallel instruction set with unique DSP addressing modes
- Nested hardware DO loops including infinite loops
- Two instruction LMS adaptive filter loop
- Zero-overhead fast interrupts (two instruction cycles)
- Three 16-bit internal data buses and three 16-bit internal address buses
- On-chip peripheral registers memory mapped in data memory space
- Low power Wait and Stop modes
- Operating frequency down to DC
- Single 5V power supply
- Two external interrupt request pins
- 2k X 16-bit on-chip data RAM and 2k X 16-bit on-chip program RAM
- Bootstrap loading from external PROM, Host Interface, or Synchronous Serial Interface 0 (SSI0)
- On-chip sigma-delta voice band codec
  - Operates at sampling clock rates between 100KHz and 3MHz
  - Four software programmable decimation/interpolation ratios
  - Internal voltage reference (2/5 of positive power supply)
  - No off-chip components required
- On-chip, software programmable, frequency synthesizer (PLL)
- Synchronous memory expansion port (Port A) with 16-bit address and data buses
- 24 general purpose I/O pins
- Byte-wide Host Interface with DMA support
- Two independent synchronous serial interfaces
  - built in μ-law and A-law compression/expansion
  - up to 32 software selectable time slots in network mode
- 16-bit timer with external input/output
- On-Chip Emulation (OnCE) for unobtrusive, processor speed independent debugging

PRELIMINARY

OnCE is a trade mark of Motorola, Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

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INTRODUCTION

This data sheet is intended to be used with the *DSP56100 Family Manual* and the *DSP56156 User's Manual*. The *DSP56100 Family Manual* provides a description of the components of the DSP56100 core processor that are common to all DSP56100 family processors and includes a detailed description of the basic DSP56100 family instruction set. The *DSP56156 User's Manual* provides a description of the memory and peripherals that are specific to the DSP56156. The *DSP56156 Data Sheet* provides electrical specifications and timings that are specific to the DSP56156.

The DSP56156 pinout is shown in Figure 1. The input and output signals on the chip are organized into the 13 functional groups shown in Table 1.

Table 1 Functional Group Pin Allocations

Functional Group	Number of Pins
Address and Data Buses	32
Bus Control	9
Interrupt and Mode Control	4
Clock and PLL	3
Host Interface or PIO	15
Timer Interface or PIO	2
SSI Interfaces or PIO	10
On-chip CODEC	7
On-chip emulation (OnCE)	4
Power (Vdd)	9
Ground (Vss)	15
APower (AVdd)	1
AGround (AVss)	1
Total	112

ADDRESS AND DATA BUS (32 PINS)

A0-A15 (Address Bus) - three state, active high outputs. A0-A15 change in t0 and specify the address for external program and data memory accesses. If there is no external bus activity, A0-A15 remain at their previous values. A0-A15 are three-stated during hardware reset.

D0-D15 (Data Bus) - three state, active high, bidirectional input/outputs. Read data is sampled on the trailing edge of t2, while write data output is enabled by the leading edge of t2 and three-stated at the leading edge of t0. If there is no external bus activity, D0-D15 are three-stated. D0-D15 are also three-stated during hardware reset.

BUS CONTROL (9 PINS)

PS/$\overline{DS}$ (Program /Data Memory Select) - three state active low output. This output is asserted only when external data memory is referenced. PS/$\overline{DS}$ timing is the same for the A0-A15 address lines. PS/$\overline{DS}$ is high for program memory access and is low for data memory access. PS/$\overline{DS}$ is in the high impedance state during hardware reset.

R/$\overline{W}$ (Read/Write)- three state, active low output. Timing is the same as for the address lines, providing an "early write" signal. R/$\overline{W}$ (which changes in t0) is high for a read access and is low for

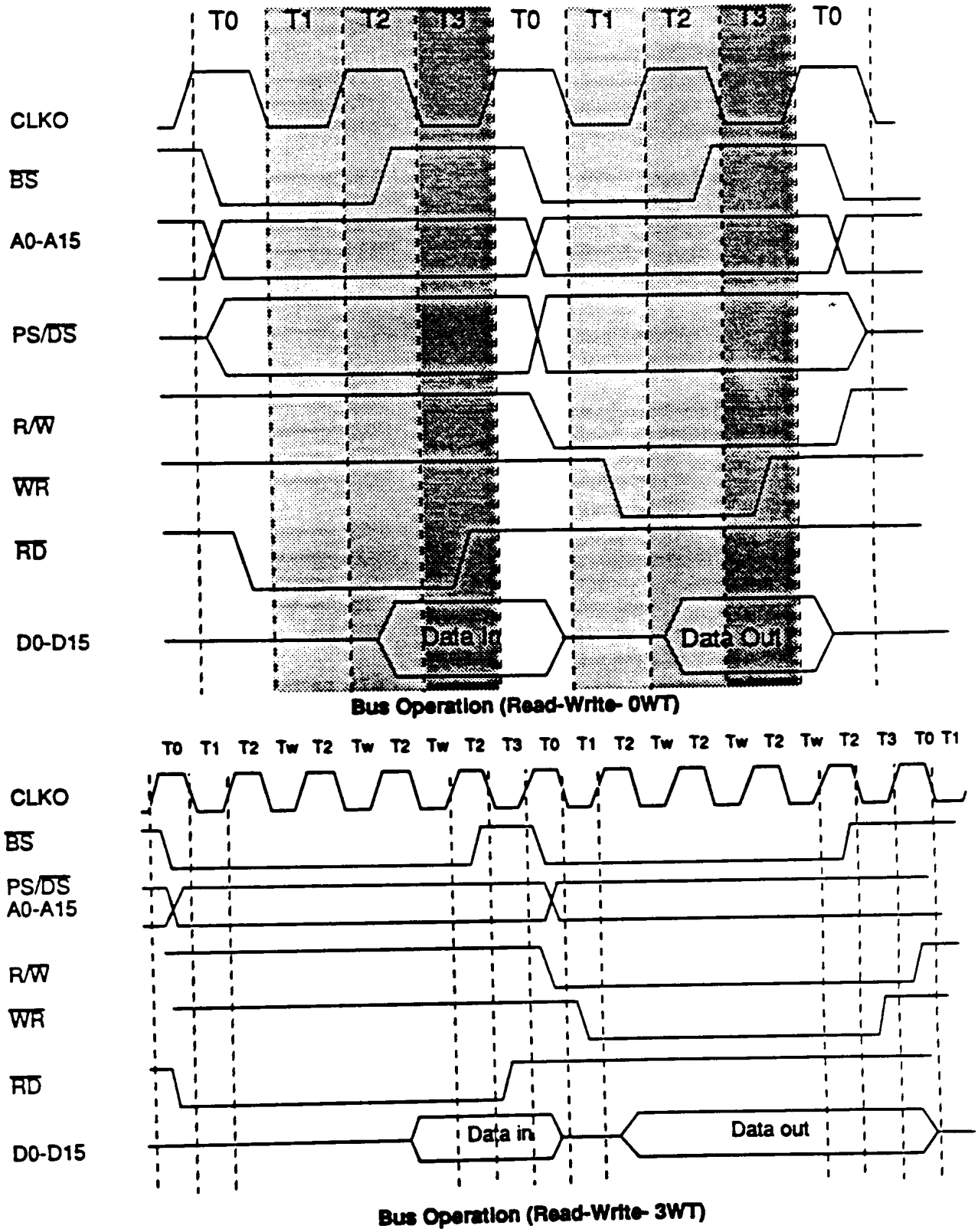


Figure 1 Bus Operation

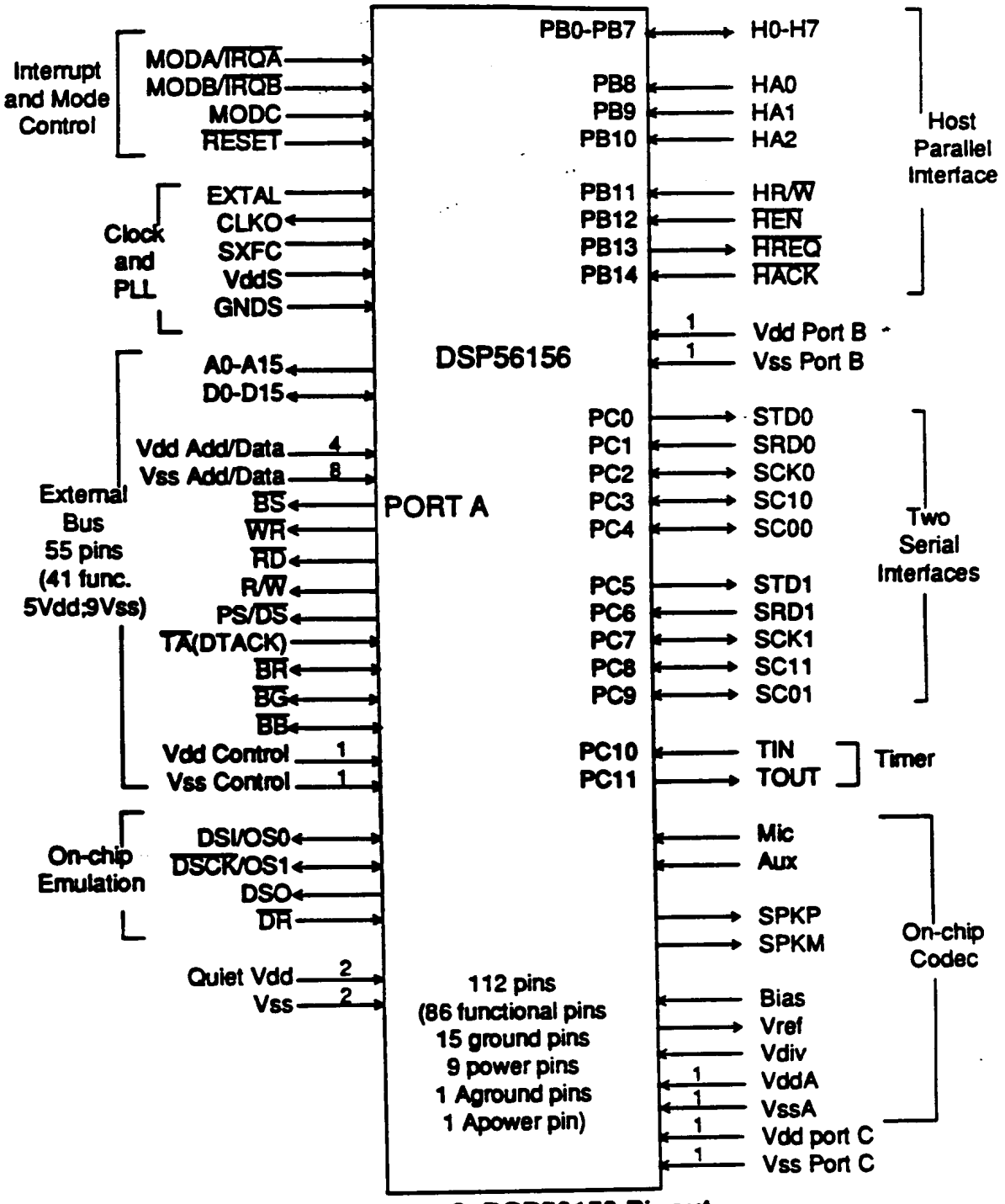


Figure 2 DSP56156 Pinout

a write access. If the external bus is not used during an instruction cycle (t0,t1,t2,t3), R/W goes high in t0. R/W is three-stated during hardware reset.

WR (Write Enable) - three state, active low output. This output is asserted during external memory write cycles. When WR is asserted in t1, the data bus pins D0-D15 become outputs and the DSP puts data on the bus during the leading edge of t2. When WR is deasserted in t3, the external data has been latched inside the external device. When WR is asserted, it qualifies the A0-A15 and PS/DS pins. WR can be connected directly to the WE pin of a static RAM. WR is three-stated during hardware reset or when the DSP is not bus master.

$\overline{RD}$ (Read Enable) - three state, active low output. This output is asserted during external memory read cycles. When $\overline{RD}$ is asserted in late t0/early t1, the data bus pins D0-D15 become inputs and an external device is enabled onto the data bus. When $\overline{RD}$ is deasserted in t3, the external data has been latched inside the DSP. When $\overline{RD}$ is asserted, it qualifies the A0-A15 and PS/$\overline{DS}$ pins. $\overline{RD}$ can be connected directly to the $\overline{OE}$ pin of a static RAM or ROM. $\overline{RD}$ is three-stated during hardware reset or when the DSP is not bus master.

$\overline{BS}$ (Bus Strobe) - active low output. Asserted at the start of a bus cycle (during T0) and deasserted at the end of the bus cycle (during T2). This pin provides an "early bus start" signal which can be used as address latch and as an "early bus end" signal which can be used by an external bus controller. $\overline{BS}$ is three-stated during hardware reset.

$\overline{TA}$ $\overline{TA}$ (Transfer Acknowledge) - active low input. If there is no external bus activity, the $\overline{TA}$ input is ignored by the DSP. When there is external bus cycle activity, $\overline{TA}$ can be used to insert wait states in the external bus cycle. $\overline{TA}$ is sampled on the leading edge of the clock. Any number of wait states from 1 to infinity may be inserted by using $\overline{TA}$. If $\overline{TA}$ is sampled high on the leading edge of the clock beginning the bus cycle, the bus cycle will end 2T after the $\overline{TA}$ has been sampled low on a leading edge of the clock; if the Bus Control Register (BCR) value does not program more wait states. The number of wait states is determined by the $\overline{TA}$ input or by the Bus Control Register (BCR), whichever is longer. $\overline{TA}$ is still sampled during the leading edge of the clock when wait states are controlled by the BCR value. In that case, $\overline{TA}$ will have to be sampled low during the leading edge of the last period of the bus cycle programmed by the BCR (2T before the end of the bus cycle programmed by the BCR) in order not to add any wait states. $\overline{TA}$ should always be deasserted during T3 to be sampled high by the leading edge of T0. If $\overline{TA}$ is sampled low (asserted) at the leading edge of the T0 beginning the bus cycle, and if no wait states are specified in the BCR register, zero wait states will be inserted in the external bus cycle, regardless the status of $\overline{TA}$ during the leading edge of T2.

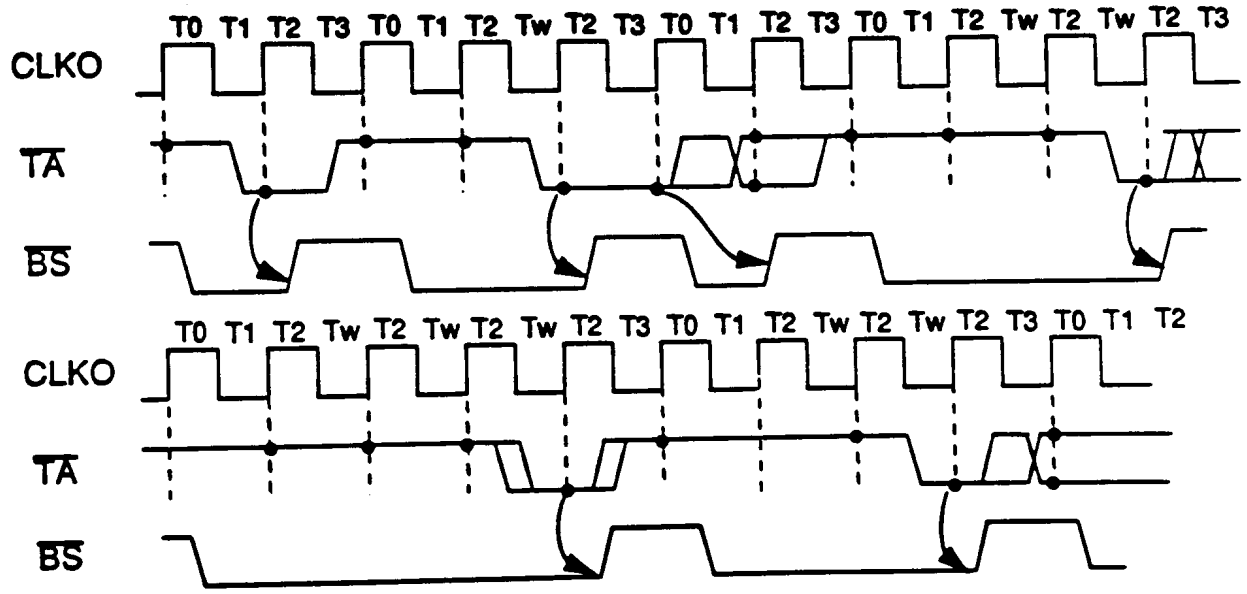


Figure 3 $\overline{TA}$ Controlled Accesses

$\overline{BR}$ (Bus Request) - active low output when in master mode, active low input when in slave mode. After power-on reset, this pin is an input (slave mode). In this mode, the bus request $\overline{BR}$ allows

another device such as a processor or DMA controller to become the master of the DSP external data bus D0-D15 and external address bus A0-A15. The DSP asserts $\overline{BG}$ a few T states after the $\overline{BR}$ input is asserted. The DSP bus controller will release control of the external data bus D0-D15, address bus A0-A15 and bus control pins PS/ $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, and R/$\overline{W}$ at the earliest time possible consistent with proper synchronization. These pins will then be placed in the high impedance state and the $\overline{BB}$ pin will be deasserted. The DSP will continue executing instructions only if internal program and data memory resources are being accessed. If the DSP requests the external bus while $\overline{BR}$ input pin is asserted, the DSP bus controller inserts wait states until the external bus becomes available ($\overline{BR}$ and $\overline{BB}$ deasserted). Note that interrupts are not serviced when a DSP instruction is waiting for the bus controller. Note also that $\overline{BR}$ is prevented from interrupting the execution of a read/ modify/ write instruction.

If the master bit in the OMR register is set, this pin becomes an output (Master Mode). In this mode, the DSP is not the external bus master and has to assert $\overline{BR}$ to request the bus mastership. The DSP bus controller will insert wait states until $\overline{BG}$ input is asserted and will then begin normal bus accesses after the rising of the clock which sampled $\overline{BB}$ high. The $\overline{BR}$ output signal will remain asserted until the DSP no longer needs the bus. In this mode, the Request Hold bit (RH) of the Bus Control Register (BCR) allows $\overline{BR}$ to be asserted under software control.

During external accesses caused by an instruction executed out of external program memory, $\overline{BR}$ remains asserted low for consecutive external X memory accesses and continues toggling for consecutive external P memory accesses unless the Request Hold bit (RH) is set inside the Bus Control Register (BCR).

$\overline{BG}$ (Bus Grant) - active low input when in master mode, active low output when in slave mode. Output after power on reset if the slave is selected, this pin is asserted to acknowledge an external bus request. It indicates that the DSP will release control of the external address bus A0-A15, data bus D0-D15 and bus control pins when $\overline{BB}$ is deasserted. The $\overline{BG}$ output is asserted in response to a $\overline{BR}$ input. When the $\overline{BG}$ output is asserted and $\overline{BB}$ is deasserted, the external address b : A0-A15, data bus D0-D15 and bus control pins are in the high impedance state. $\overline{BG}$ assertion may occur in the middle of an instruction which requires more than one external bus cycle for execution. Note that $\overline{BG}$ assertion will not occur during indivisible read-modify-write instructions (BFSET, BFCLR, BFCHG). When $\overline{BR}$ is deasserted, the $\overline{BG}$ output is deasserted and the DSP regains control of the external address bus, data bus, and bus control pins when the $\overline{BB}$ pin is sampled high.

This pin becomes an input if the master bit in the OMR register is set (Master Mode). It is asserted by an external processor when the DSP may become the bus master. The DSP can start normal external memory access after the $\overline{BB}$ pin has been deasserted by the previous bus master. When $\overline{BG}$ is deasserted, the DSP will release the bus as soon as the current transfer is completed. The state of $\overline{BG}$ may be tested by testing the BS bit in the Bus Control Register.

$\overline{BG}$ is ignored during hardware reset.

$\overline{BB}$ (Bus Busy) - active low input when not bus master, active low output when bus master. This pin is asserted by the DSP when it becomes the bus master and it performs an external access. It is deasserted when the DSP releases bus mastership. $\overline{BB}$ becomes an input when the DSP is no longer the bus master.

INTERRUPT AND MODE CONTROL (3 PINS)

MODA/$\overline{\text{IRQA}}$ (Mode Select A/External Interrupt Request A) - This input has two functions - to select the initial chip operating mode and, after synchronization, to allow an external device to request a DSP interrupt. MODA is read and internally latched in the DSP when the processor exits the reset state. MODA and MODB select the initial chip operating mode. Several clock cycles after leaving the reset state, the MODA pin changes to the external interrupt request $\overline{\text{IRQA}}$. The chip operating mode can be changed by software after reset. The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request which indicates that an external device is requesting service. It may be programmed to be level sensitive or negative edge triggered. If level sensitive triggering is selected, an external pull up resistor is required for wired-OR operation. If the processor is in the stop standby state and $\overline{\text{IRQA}}$ is asserted, the processor will exit the stop state.

MODB/$\overline{\text{IRQB}}$ (Mode Select B/External Interrupt Request B) - This input has two functions - to select the initial chip operating mode and, after internal synchronization, to allow an external device to request a DSP interrupt. MODB is read and internally latched in the DSP when the processor exits the reset state. MODA and MODB select the initial chip operating mode. Several clock cycles after leaving the reset state, the MODB pin changes to the external interrupt request $\overline{\text{IRQB}}$. After reset, the chip operating mode can be changed by software. The $\overline{\text{IRQB}}$ input is an external interrupt request which indicates that an external device is requesting service. It may be programmed to be level sensitive or negative edge triggered. If level sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.

MODC (Mode Select C) - This input is used to select the initial bus operating mode. When tied high, the external bus is programmed in the master mode ($\overline{\text{BR}}$ output and $\overline{\text{BG}}$ input) and when tied low the bus is programmed in the slave mode ($\overline{\text{BR}}$ input and $\overline{\text{BG}}$ output). MODC is read and internally latched in the DSP when the processor exits the reset state. After $\overline{\text{RESET}}$, the bus operating mode can be changed by software by writing the MC bit of the OMR register.

$\overline{\text{RESET}}$ (Reset) - This input is a direct hardware reset of the processor. When $\overline{\text{RESET}}$ is asserted, the DSP is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. When the reset pin is deasserted, the initial chip operating mode is latched from the MODA and MODB pins. The internal reset signal should be deasserted synchronous with the internal clocks.

POWER, GROUND, AND CLOCK (28 PINS)

VCC (8) (Power) - power pins.

VSS (14) (Ground) - ground pins.

VDDS (Synthesizer Power) - This pin supplies a quiet power source to the PLL to provide greater frequency stability.

GNDS (Synthesizer Ground) - This pin supplies a quiet ground source to the PLL to provide greater frequency stability.

VDDA (Power Supply input) - This pin is the positive analog supply input. It should be connected to VCC when the codec is not used.

VSSA (Analog Ground) - This pin is the analog ground return. It should be connected to VSS when the codec is not used.

EXTAL (External Clock/Crystal Input) - This input should be connected to an external clock or to an external oscillator. A sine wave with a minimum swing of 1Vpp can be applied to this pin. After being squared, the input frequency can be used as the DSP core internal clock. In that case, it is divided by two to produce a four phase instruction cycle clock, the minimum instruction time being two input clock periods.This input frequency is also used, after division, as input clock for the on-chip codec and the on-chip phase locked loop (PLL).

CLKO (Clock Output) - This pin outputs a buffered clock signal. By programming two bits (CS1-CS0) inside the PLL Control Register (PLCR), the user can select between outputting a squared version of the signal applied to EXTAL, a squared version of the signal applied to EXTAL divided by 2, and a delayed version of the DSP core master clock. The clock frequency on this pin can be disabled by setting the Clockout Disable bit (CD; bit 7) of the Operating Mode Register (OMR). In this case, the pin can be left floating.

SXFC (External Filter Capacitor) - This pin is used to add an external capacitor to the PLL filter circuit. The capacitor should be connected between SXFC and VDDS.

HOST INTERFACE (15 PINS)

H0-H7 (Host Data Bus) - This bidirectional data bus is used to transfer data between the host processor and the DSP. This bus is an input unless enabled by a host processor read. H0-H7 may be programmed as general purpose parallel I/O pins called PB0-PB7 when the Host Interface (HI) is not being used.

HA0-2 (Host Address 0-2) - These inputs provide the address selection for each HI register and are stable when $\overline{\text{HEN}}$ is asserted. HA0-HA2 may be programmed as general purpose parallel I/O pins called PB8-PB10 when the HI is not being used.

HR/$\overline{\text{W}}$ (Host Read/Write) - This input selects the direction of data transfer for each host processor access. If HR/$\overline{\text{W}}$ is high and $\overline{\text{HEN}}$ is asserted, H0-H7 are outputs and DSP data is transferred to the host processor. If HR/$\overline{\text{W}}$ is low and $\overline{\text{HEN}}$ is asserted, H0-H7 are inputs and host data is transferred to the DSP. HR/$\overline{\text{W}}$ is stable when $\overline{\text{HEN}}$ is asserted. HR/$\overline{\text{W}}$ may be programmed as a general purpose I/O pin called PB11 when the HI is not being used.

$\overline{\text{HEN}}$ (Host Enable) - This input enables a data transfer on the host data bus. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is high, H0-H7 becomes an output and DSP data may be latched by the host processor. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is low, H0-H7 is an input and host data is latched inside the DSP when $\overline{\text{HEN}}$ is deasserted. Normally a chip select signal derived from host address decoding and an enable clock is connected to the Host Enable. $\overline{\text{HEN}}$ may be programmed as a general purpose I/O pin called PB12 when the HI is not being used.

$\overline{\text{HREQ}}$ (Host Request) - This open-drain output signal is used by the HI to request service from the host processor. $\overline{\text{HREQ}}$ may be connected to an interrupt request pin of a host processor, a transfer request of a DMA controller, or a control input of external circuitry. $\overline{\text{HREQ}}$ is asserted when an enabled request occurs in the HI. $\overline{\text{HREQ}}$ is deasserted when the enabled request is cleared or masked, DMA HACK is asserted, or the DSP is reset. $\overline{\text{HREQ}}$ may be programmed as a general purpose I/O pin (not open-drain) called PB13 when the HI is not being used.

HACK (Host Acknowledge) - This input has two functions - (1) to provide a Host Acknowledge signal for DMA transfers or (2) to control handshaking and to provide a Host Interrupt Acknowledge compatible with MC68000 family processors. If programmed as a Host Acknowledge signal, HACK may be used as a data strobe for HI DMA data transfers. If programmed as an MC68000 Host Interrupt Acknowledge, HACK is used to enable the HI Interrupt Vector Register (IVR) onto the Host Data Bus H0-H7 if the Host Request HREQ output is asserted. In this case, all other HI control pins are ignored and the HI state is not affected. HACK may be programmed as a general purpose I/O pin called PB14 when the HI is not being used.

16-BIT TIMER (2 PINS)

TIN (Timer input) - This input receives external pulses to be counted by the on-chip 16-bit timer when external clocking is selected. The pulses are internally synchronized to the DSP core internal clock. TIN may be programmed as a general purpose I/O pin called PC10 when the external event function is not being used.

TOUT (Timer output) - This output generates pulses or toggles on a timer overflow event or a compare event. TOUT may be programmed as a general purpose I/O pin called PC11 when disabled by the timer out enable bits (TO2-TO0).

SYNCHRONOUS SERIAL INTERFACES (SSI0 AND SSI1) (10 PINS)

STD0 (SSI0 Transmit Data) - This output pin transmits serial data from the SSI0 Transmit Shift Register. STD0 may be programmed as a general purpose I/O pin called PC0 when the SSI0 STD0 function is not being used.

SRD0 (SSI0 Receive Data) - This input pin receives serial data and transfers the data to the SSI0 Receive Shift Register. SRD0 may be programmed as a general purpose I/O pin called PC1 when the SSI0 SRD0 function is not being used.

SCK0 (SSI0 Serial Clock) - This bidirectional pin provides the serial bit rate clock for the SSI0 interface. SCK0 may be programmed as a general purpose I/O pin called PC2 when the SSI0 interface is not being used.

SC10 (Serial Control 1) - This bidirectional pin is used by the SSI0 serial interface as frame sync I/O or flag I/O. SC10 may be programmed as a general purpose I/O pin called PC3 when the SSI0 is not using this pin.

SC00 (Serial Control 0) - This bidirectional pin is used by the SSI0 serial interface as frame sync I/O or flag I/O. SC00 may be programmed as a general purpose I/O pin called PC4 when the SSI0 is not using this pin.

STD1 (SSI1 Transmit Data) - This output pin transmits serial data from the SSI1 Transmit Shift Register. STD1 may be programmed as a general purpose I/O pin called PC5 when the SSI1 STD1 function is not being used.

SRD1 (SSI1 Receive Data) - This input pin receives serial data and transfers the data to the SSI1 Receive Shift Register. SRD1 may be programmed as a general purpose I/O pin called PC6 when the SSI1 SRD1 function is not being used.

SCK1 (SSI1 Serial Clock) - This bidirectional pin provides the serial bit rate clock for the SSI1 interface. SCK1 may be programmed as a general purpose I/O pin called PC7 when the SSI1 interface is not being used.

SC11 (Serial Control 1) - This bidirectional pin is used by the SSI1 serial interface as frame sync I/O or flag I/O. SC11 may be programmed as a general purpose I/O pin called PC8 when the SSI1 is not using this pin.

SC01 (Serial Control 0) - This bidirectional pin is used by the SSI1 serial interface as frame sync I/O or flag I/O. SC01 may be programmed as a general purpose I/O pin called PC9 when the SSI1 is not using this pin.

ON-CHIP EMULATION (4 PINS)

DSI/OS0 (Debug Serial Input/Chip Status 0) - The DSI/OS0 pin, when an input, is the pin through which serial data or commands are provided to the OnCE controller. The data received on the DSI pin will be recognized only when the DSP has entered the debug mode of operation. Data must have valid TTL logic levels before the serial clock falling edge. Data is always shifted into the OnCE serial port most significant bit (MSB) first. When the DSP is not in the debug mode, the DSI/OS0 pin provides information about the chip status if it is an output and used in conjunction with the OS1 pin.

$\overline{\text{DSCK}}$/OS1 (Debug Serial Clock/Chip Status 1) - The $\overline{\text{DSCK}}$/OS1 pin, when an input, is the pin through which the serial clock is supplied to the OnCE. The serial clock provides pulses required to shift data into and out of the OnCE serial port. Data is clocked into the OnCE on the falling edge and is clocked out of the OnCE serial port on the rising edge. When the DSP is not in the debug mode, the $\overline{\text{DSCK}}$/OS1 pin provides information about the chip status if it is an output and used in conjunction with the OS0 pin.

DSO (Debug Serial Output) - The debug serial output provides the data contained in one of the OnCE controller registers as specified by the last command received from the command controller. When idle, this pin is high. When the requested data is available, the DSO line will be asserted (negative true logic) for four T cycles (one instruction cycle) to indicate that the serial shift register is ready to receive clocks in order to deliver the data. When the chip enters the debug mode due to an external debug request ($\overline{\text{DR}}$), an internal software debug request (DEBUG), a hardware breakpoint occurrence or a trace/step occurrence, this line will be asserted for three T cycles to indicate that the chip has entered the debug mode and is waiting for commands. Data is always shifted out the OnCE serial port most significant bit (MSB) first.

$\overline{\text{DR}}$ (Debug Request Input) - The debug request input provides a means of entering the debug mode of operation. This pin when asserted (negative true logic) will cause the DSP to finish the current instruction being executed, enter the debug mode, and wait for commands to be entered from the debug serial input line.

ON-CHIP CODEC (7 PINS)

AUX (Auxiliary Input) - This pin is selected as the analog input to the A/D converter when the INS bit is set in the codec control register COCR. This pin should be left floating when the codec is not used.

BIAS (Bias current pin) - This input is used to determine the bias current for the analog circuitry. Connecting a resistor between BIAS and VGNDA will program the current bias generator. This pin should be left floating when the codec is not used.

MIC (Microphone input) - This pin is selected as the analog input to the A/D converter when the INS bit is cleared in the codec control register COCR. This pin should be left floating when the codec is not used.

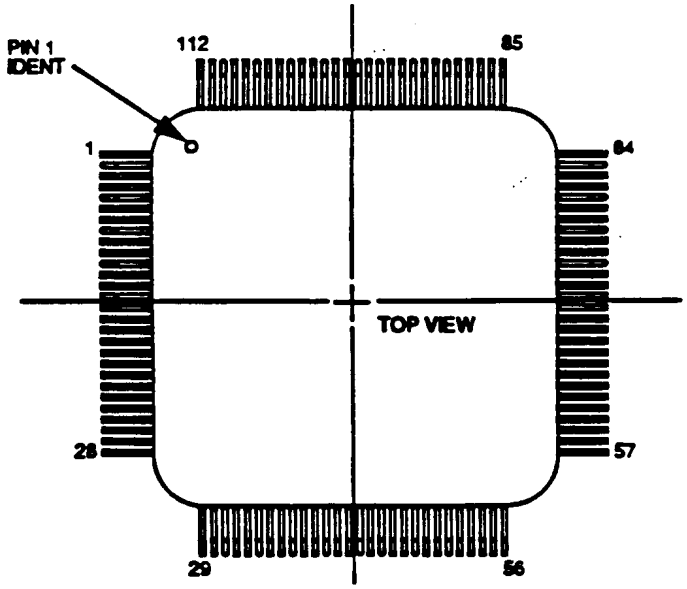
SPKP (Speaker Positive Output) - This pin is the positive analog output from the on-chip D/A converter. This pin should be left floating when the codec is not used.

SPKM (Speaker Negative Output) - This pin is the negative analog output from the on-chip D/A converter. This pin should be left floating when the codec is not used.

VREF (Voltage Reference Output) - This pin is the op-amp buffer output in the reference voltage generator. It has a value of (2/5) VDDA. This pin should be left floating when the codec is not used.

VDIV (Voltage Division Output) - This pin is the input to the op-amp buffer in the reference voltage generator. It is connected to a resistor divider network located within the codec block which provides a voltage equal to (2/5)VDDA. This pin should be connected to the ground via a capacitor when the codec is used and should be left floating when the codec is not used.

PINOUT AND PACKAGE INFORMATION



MOTOROLA
DSP56156
112 CQFP PACKAGE
PIN-OUT

PRELIMINARY

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	GND4	29	MIC	57	H6/PB6	85	MODB
2	D2	30	AUX	58	H5/PB5	86	MODC
3	D3	31	BIAS	59	VDD6	87	A0
4	VDD3	32	$\overline{BG}$	60	H2/PB2	88	A1
5	D4	33	OVDD0	61	H3/PB3	89	GND0
6	D5	34	$\overline{BR}$	62	H4/PB4	90	A2
7	GND5	35	$\overline{BB}$	63	SRD1/PC8	91	A3
8	D6	36	VDD5	64	STD1/PC5	92	VDD1
9	D7	37	$\overline{WR}$	65	H1/PB1	93	A4
10	D8	38	GND6	66	H0/PB0	94	A5
11	D9	39	$\overline{RD}$	67	$\overline{RREQ}$/PB13	95	GND1
12	GND6	40	PS/$\overline{DS}$	68	$\overline{RACK}$/PB14	96	OVDD1
13	D10	41	$\overline{ES}$	69	$\overline{REN}$/PB12	97	A6
14	D11	42	R/$\overline{W}$	70	$\overline{RRW}$/PB11	98	A7
15	VDD4	43	DSO	71	HA2/PB10	99	A8
16	D12	44	$\overline{DSCK}$/OS1	72	HA1/PB9	100	A9
17	D13	45	DSI/OS0	73	GND10	101	GND2
18	GND7	46	CLKO	74	HA0/PB8	102	A10
19	D14	47	QGND0	75	TOUT/PC11	103	VDD2
20	D15	48	GND5	76	VDD7	104	QGND1
21	$\overline{TA}$	49	XFC	77	TIN/PC10	105	A11
22	$\overline{DR}$	50	VDD5	78	SC00/PC4	106	A12
23	VDDA	51	EXTAL	79	SC10/PC3	107	A13
24	SPKP	52	SC01/PC9	80	SCK0/PC2	108	GND3
25	SPKM	53	GND9	81	SRD0/PC1	109	A14
26	GNDA	54	SC11/PC8	82	STD0/PC0	110	A15
27	VDIV	55	SCK1/PC7	83	$\overline{RESET}$	111	D0
28	VREF	56	H7/PB7	84	MODA	112	D1

Note: Do not connect to "NO CONNECT" PINS

	Internal	A0-A15	D0-D15	Bus control	Port B, Once, Port C	Codec
Vcc	QVDD0-1	VDD1-2	VDD3-4	VDD5	VDD6, VDD7	VDDA
GND	QGND0-1	GND0-3	GND4-7	GND8	GND9, GND10	GNDA

The preliminary DC/AC electrical specifications are generated from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

APPENDIX E
ELECTRICAL CHARACTERISTICS AND TIMING

The DSP56156 is fabricated in high density HCMOS with TTL compatible inputs and CMOS compatible outputs.

Maximum Electrical Ratings (VSS = 0 Vdc)

Rating	Symbol	Value	Unit
Supply Voltage	Vdd	-0.3 to +7.0	V
All Input Voltages	V_{in}	VSS- 0.5 toVdd + 0.5	V
Current Drain per Pin excluding Vdd and VSS	I	10	mA
Storage Temperature	T_{stg}	-55 to +150	°C

Operating Conditions

Marking	Speed	Supply Voltage VDD(V)		Junction Temperature T_J (°C)	
		Min	Max	Min	Max
	40 MHz	4.65	5.25	-40	115
	50 MHz	4.65	5.25	-40	115
	60 MHz	4.65	5.25	-40	115

Thermal Characteristics — CQFP Package

Characteristics Thermal Resistance — Ceramic	Symbol	Value	Rating
Junction to Ambient	Θ_{JA}	30	°C/W
Junction to Case (estimated)	Θ_{JC}	7	°C/W

Thermal Characteristics — PQFP Package

Characteristics Thermal Resistance — Ceramic	Symbol	Value	Rating
Junction to Ambient	Θ_{JA}	30	°C/W
Junction to Case (estimated)	Θ_{JC}	13	°C/W

This device contains protective circuitry against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either Vss or Vdd).

Power Considerations

The average chip junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (PD * \Theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

Θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

PINT = I_{CC}*Vdd, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected. An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K/(T_J + 273° C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D * (T_A + 273° C) + \Theta_{JA} * P_D \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation (2) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A. The total thermal resistance of a package (Θ_{JA}) can be separated into two components, Θ_{JA} and C_A, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (Θ_{JC}) and from the case to the outside ambient (C_A). These terms are related by the equation:

$$\Theta_{JA} = \Theta_{JC} + C_A \quad (4)$$

Θ_{JC} is device related and cannot be influenced by the user. However, C_A is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce C_A so that Θ_{JA} approximately equals Θ_{JC}. Substitution of Θ_{JC} for Θ_{JA} in equation (1) will result in a lower semiconductor junction temperature. Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, "Thermal Resistance Measurement Method for MC68XX Microcomponent Devices", and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User—derived values for thermal resistance may differ.

Layout Practices

Each DSP56156 Vdd pin should be provided with a low-impedance path to + 5 volts. Each DSP56156 Vss pin should likewise be provided with a low-impedance path to ground. The power supply pins drive six distinct groups of logic on chip. They are:

Power and Ground Connections for CQFP and PQFP

Vdd	Vss	Function
33,96	47,104	Internal Logic supply pins
92,103	89,95,101,108	Address bus output buffer supply pins
4,15	1,7,12,18	Data bus output buffer supply pins
36	38	Bus control buffer supply pins
59,76	53,73	OnCE, Port B and C output buffer supply pins
23	26	Codec analog supply pins

Power and Ground Connections

The VDD power supply should be bypassed to ground using at least six 0.01-0.1 uF bypass capacitors located either underneath the chip's socket or as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip Vdd and Vss should be kept to less than 1/2" per capacitor lead. The use of at least a four layer board is recommended, employing two inner layers as Vdd and Vss planes. All output pins on the DSP56156 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses as well as the PS/$\overline{DS}$, $\overline{BS}$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $\overline{IRQA}$, $\overline{IRQB}$, and $\overline{HEN}$ pins. Maximum PC trace lengths on the order of 6" are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the Vdd and Vss circuits.

The analog power for the VDDA pin and the analog ground for the VSSA pin should be separated from the digital VDD and ground planes. The analog power and ground planes should only be tied to the digital power and ground planes at one point where current enters and exits only at this point.

The analog VDD and ground planes should not have digital signal running over them if possible.

The analog VDD and ground pins should be decoupled as close to the DSP as possible.

Clocks signals should not be run across many signals and should be kept away from analog power and ground signals as well as any analog signals.

Refer to Analog I/O Figure 1 for more details.

Analog I/O Characteristics

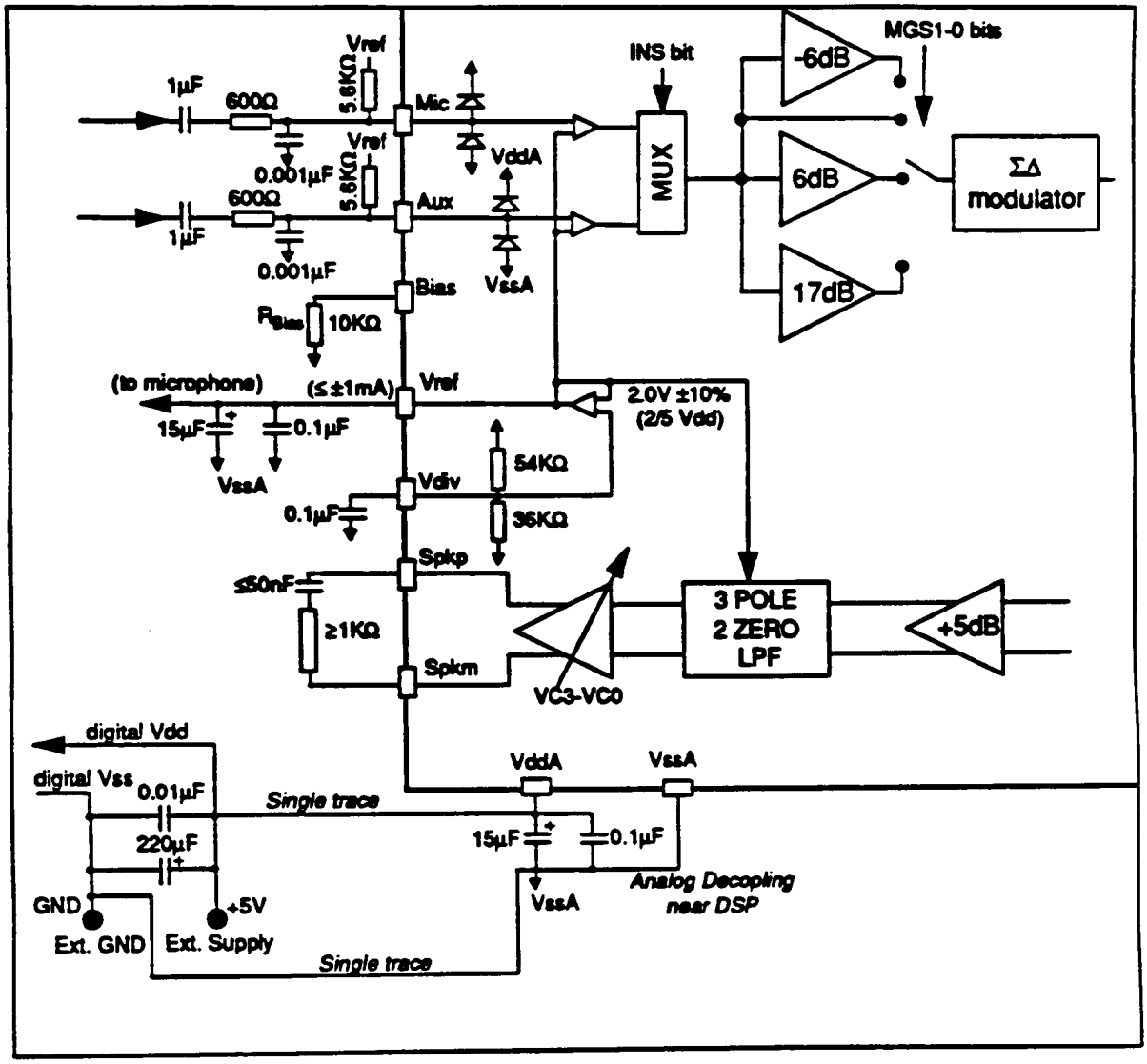
(VddA = 5.0 Vdc +/- 10%, TJ = -40 to +125 °C).
The Analog I/O characteristics of this device are shown below.

Characteristic	Min	Typ	Max	Unit
Input Impedance on Mic & Aux[a]	46	78	1400	kΩ
Input Capacitance on Mic and Aux	—	—	10	pF
Peak Input Voltage on the Mic/Aux Input: (0.14dBm0[b]) -6dB- MGS1-0=00 0dB- MGS1-0=01 6dB- MGS1-0=10 17dB- MGS1-0=11	 — — — —	 — — — —	 1.414 0.707 354 100	 Vp Vp mVp mVp
Internal Input GainVariation; G=-6dB, 0dB,6dB or 17dB (±0.83dB variation due to 10% variation on Vdd):	G-0.83	G	G+0.83	dB
Vref Output Voltage	1.8	2	2.2	V
Vref Output Current	—	—	±1	mA
DC offset between Spkout1 and Spkout2	—	—	100	mV
Allowable Differential Load Capacitance on Spkout1/2(with 1kΩ in series)	0	—	50	nF
Allowable Single-ended Load Capacitance on Spkout1/2(with 0.5kΩ in series)	0[c]	—	100	nF
Maximum Single-ended Signal Output Level	—	—	1	Vp
Maximum Differential Signal Output Level	—	—	2	Vp
Single-ended Load Resistance	500	—	—	Ω
Differential Load Resistance	1	—	—	kΩ
R bias	—	10[d]	—	kΩ
Internal Output Volume Control Variation VC=-20,-15,-10,-5,0,6,12,18,24,30,35 dB (±0.83dB variation due to 10% variation on Vdd)	VC-0.83	VC	VC+0.83	dB

a. Min. value reached for a codec clock of 3MHz, typ. for 2MHz and max. for 100KHz
b. 0dBm0 corresponds to 3.14dB below the input saturation level
c. AC coupling is necessary in single-ended mode when the load resistor is not tied to Vref
d. ±10%

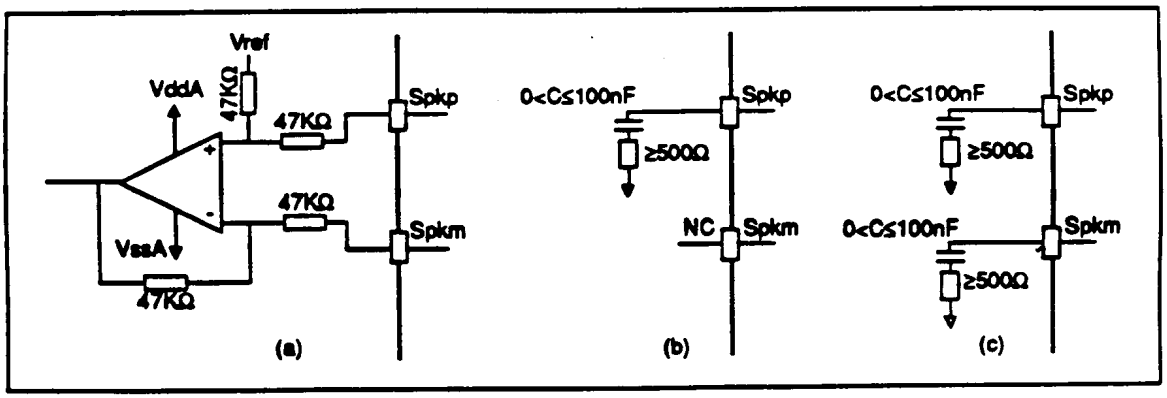
Analog I/O Figure 1 describes the recommended analog I/O and power supply configurations.

The two analog inputs are electrically identical. When one is not used, it can be left floating. When used, an AC coupling capacitor is required. The value of the capacitor along with the input impedance of the pin determine the cut off frequency of a high pass filter. The input impedance of the MIC and AUX varies as a function of the ΣΔ modulator master clock. 78 kΩ is a typical value at 2MHz. An AC capacitor of 1μF defines a high pass filter pole of 2 Hz. A smaller capacitor value will move this pole higher in frequency.



Analog I/O Figure 1 Recommended Analog I/O Configuration

Analog I/O Figure 2 shows three possible single-ended output configurations. Configuration (a) is highly recommended. For configuration (b) and (c), since the load resistor is tied to VssA, an AC coupling capacitor is required.



Analog I/O Figure 2 Single-ended Output Configurations

A/D and D/A Performances

(VddA = 5.0 Vdc +/- 10%, TJ = -40 to +125 °C).
The A/D and D/A performances of this device are shown below.

The results are given for a codec clock of 2.048Mhz and a decimation ratio of 128 with the analog I/O configurations given on Analog I/O Figure 1. The noise is integrated in the band 0-16KHz.

Characteristic	Level	Min.	Typ.	Max.	Unit
Analog to Digital Section Signal to Noise plus Distortion Ratio	0dBm0[a]				dB
	-10dBm0				dB
	-20dBm0				dB
	-50dBm0				dB
Digital Analog to Section Signal to Noise plus Distortion Ratio	0dB				dB
	-10dB				dB
	-20dB				dB
	-50dB				dB

a. 0dBm0 correspond to -3.14dB below the input saturation level

Other On-Chip Codec Characteristics

(VddA = 5.0 Vdc +/- 10%, TJ = -40 to +125 °C, CL = 50 pF + 1 TTL Load).
The Analog I/O characteristics of this device are shown below.

Characteristic	Min	Typ	Max	Unit
Codec Master Clock	0.1	2.048	3	MHz
Codec Sampling rate	78	16000	37000	Hz
Recovery time for the A/D digital output from inactive to active	—			msec
Recovery time for the A/D digital output on input and gain changes	—			msec
Recovery time for the D/A output from inactive to active, Muted to not Muted and changed to output gain	—			msec
Codec group delay	—	—		msec
A/D to D/A Crosstalk	—	—		dB
D/A to A/D Crosstalk	—	—		dBm0
Idle noise at the D/A output	—	—		µVrms
Idle noise at the A/D digital output	—	—		dBm0

DC Electrical Characteristics (VSS = 0 Vdc)

(Vdd = 5.0 Vdc +/- 10%, TJ = -40 to +125 °C, CL = 50 pF + 1 TTL Load).
The DC electrical characteristics of this device are shown below.

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage — Except EXTAL, $\overline{\text{RESET}}$ MODA, MODB,MODC	VIH	2.0	—	Vdd	V
Input Low Voltage — Except EXTAL, MODA, MODB, MODC	VIL	-0.5	—	0.8	V
Input High Voltage — EXTAL	VIHC	4.0	—	Vdd	V
Input Low Voltage — EXTAL	VILC	-0.5	—	0.6	V
Input High Voltage — $\overline{\text{RESET}}$	VIHR	2.5	—	Vdd	V
Input High Voltage — MODA , MODB, MODC	VIHM	3.5	—	Vdd	V
Input Low Voltage — MODA , MODB, MODC	VILM	-0.5	—	2.0	V
Input Leakage Current — EXTAL, $\overline{\text{RESET}}$, MODA, MODB, $\overline{\text{BR}}$	Iin	-1	—	1	uA
Three-State (Off-State) Input Current (@2.4 V/0.5 V)	TSI	-10	—	10	uA
Output High Voltage — (IOH = -10 uA)	VOHC	Vdd -0.1	—	—	V
Output High Voltage — (IOH = -0.4 mA)	VOH	2.4	—	—	V
Output Low Voltage — (IOL = 10 uA)	VOLC	—	—	0.1	V
Output Low Voltage — (IOL = 3.2 mA; R/$\overline{\text{W}}$ IOL = 1.6 mA; Open Drain $\overline{\text{HREQ}}$ IOL = 6.7 mA, TXD IOL = 6.7 mA)	VOL	—	—	0.4	V
Input Capacitance — (see Note 2)	Cin	—	10	—	pF

NOTES:
1. VIL <= 0.2 V, VIH >= Vdd - 0.2 V. No dc loads. EXTAL is driven by square wave.
2. Input capacitance is periodically sampled and not 100% tested in production.

Power Dissipation

(Vdd = 5.0 Vdc +/- 10%, TJ = -40 to +125 °C, CL = 50 pF + 1 TTL Load).
The DC electrical characteristics of this device are shown below.

Conditions	Sym	40 MHz		50 MHz		60 MHz		Unit
		Typ 5.0V	Max 5.5V	Typ 5.0V	Max 5.5V	Typ 5.0V	Max 5.5V	
Digital Vdd with Codec & PLL enabled	IDD							mA
	PD							mW
Digital Vdd with Codec & PLL disabled	IDD							mA
	PD							mW
Digital Vdd with Codec disabled & PLL enabled	IDD							mA
	PD							mW
Digital Vdd Codec enabled & PLL disabled	IDD							mA
	PD							mW
Digital Vdd WAIT Mode with CODEC & PLL enabled	IDD							mA
	PD							mW
Digital Vdd WAIT Mode with CODEC disabled &PLL enabled	IDD							mA
	PD							mW
STOP Mode with PLL and CLKO enabled	IDD							mA
	PD							mW
STOP Mode with PLL and CLKO disabled	IDD							mA
	PD							mW
Analog Vdd with CODEC enabled	IDDA							mA
	PDA							mW
Analog Vdd with CODEC disabled	IDDA							mA
	PDA							mW

In order to minimize the power dissipation, all unused digital inputs pins should be tied inactive to VDD or Vss and all unused I/O pins should be tied inactive through a 10KΩ resistor to VDD or Vss. When the codec is not used, all codec pins should be left floating. VDDA should be connected to VDD and VssA to Vss.

AC Electrical Characteristics (VSS = 0 Vdc)

The timing waveforms in the **AC Electrical Characteristics** are tested with a VIL maximum of 0.5 V and a VIH minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB and MODC. These four pins are tested using the input levels set forth in the **DC Electrical Characteristics**. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. The DSP56156 output levels are measured with the production test machine VOL and VOH reference levels set at 0.8 V and 2.0 V respectively.

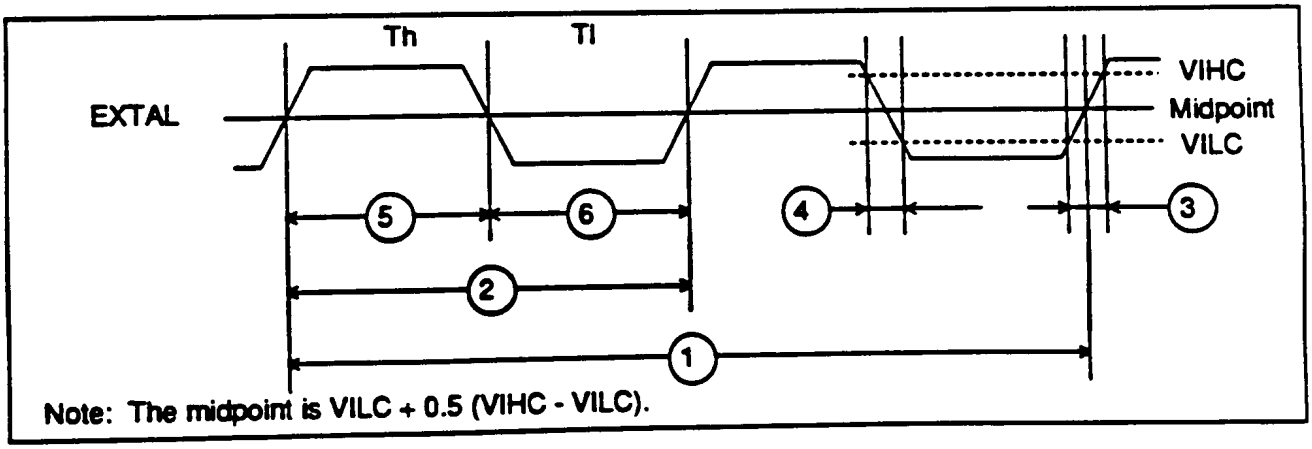
AC Electrical Characteristics — Clock Operation Timing

The system clock to the DSP56156 must be externally supplied to EXTAL.

Num.	Characteristics	Sym.	40MHz		50MHz		60MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of Operation (EXTAL Pin)	f	0	40	0	50	0	60	MHz
1	Instruction Cycle Time =2Tc = 4T	Icyc	50	—	40	—	33	—	ns
	Wait State =Tc =2T	WS	25	—	20	—	16.6	—	ns
2	CLK Cycle Period	Tc	25	—	20	—	16.3	—	ns
3	CLK Rise Time		—	3	—		—		ns
4	CLK Fall Time		—	3	—		—		ns
5	CLK High (f=40 MHz) (see Note 1 and 2) 48-52% duty cycle	Th	12	13					ns
6	CLK Low (f=40 MHz) (see Note 1 and 2) 48%-52% duty cycle	Tl	12	13					ns

Notes:

1. External Clock Input High and External Clock Input Low are measured at 50% of the input transition.
2. T = Icyc / 4 is used in the electrical characteristics. The exact length of each T is affected by the duty cycle of the external clock input.



Clock Figure 1. External Clock Timing

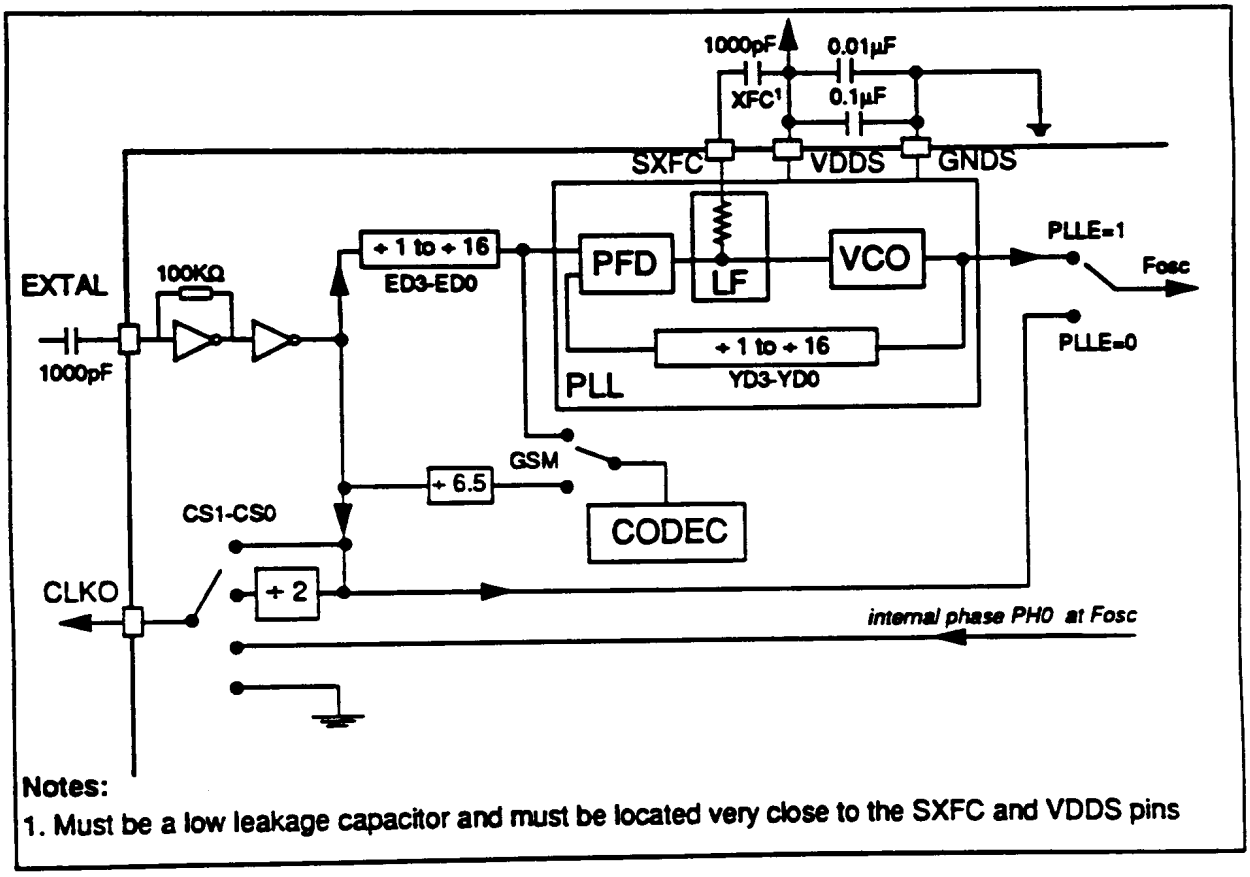
AC Electrical Characteristics — Clock and PLL OperationTiming

Characteristics	Min	Max	Unit
PLL Output frequency	10	Max Fosc[a]	MHz
EXTAL Input Frequency Amplitude	1	Vdd	Vpp

a. Maximum DSP operating frequency.

To operate at 40, 50 or 60Mhz, the part does not necessary need a 40, 50 or 60MHz clock applied to EXTAL. A low speed clock can be applied to EXTAL and the on-chip PLL can be used to multiply the clock up to the desired operating frequency for the DSP.

A sinewave with an amplitude of 1Vpp or more can also be applied to EXTAL. If the amplitude of the sinewave is lower than the normal CMOS level, an AC coupling capacitor is required on EXTAL. This capacitor is not necessary otherwise.



Notes:
1. Must be a low leakage capacitor and must be located very close to the SXFC and VDDS pins

Clock Figure 2 Clocking Configurations

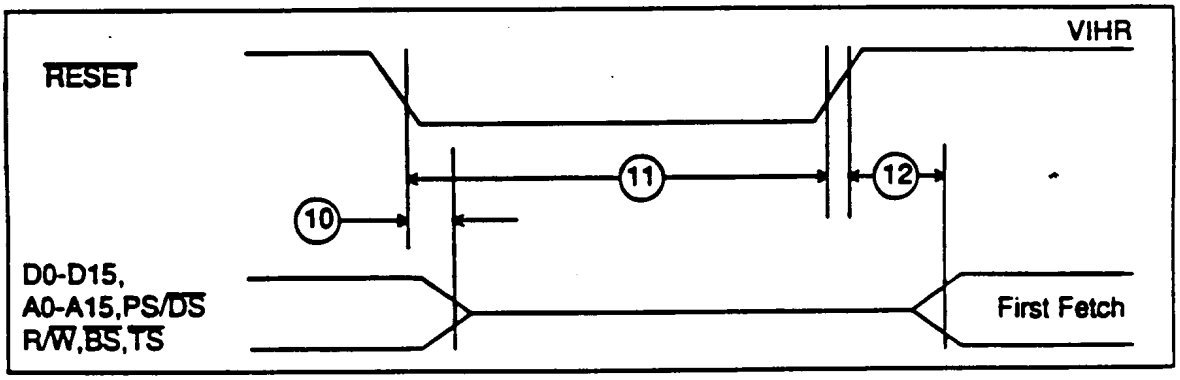
AC Electrical Characteristics
— Reset, Stop, Wait, Mode Select, and Interrupt Timing

(Vdd = 5.0 Vdc +/- 10%, TA = -40 to +125 °C, CL = 50 pF + 1 TTL Load).
WS = Number of wait states programmed into external bus access using BCR (WS = 0 - 31)

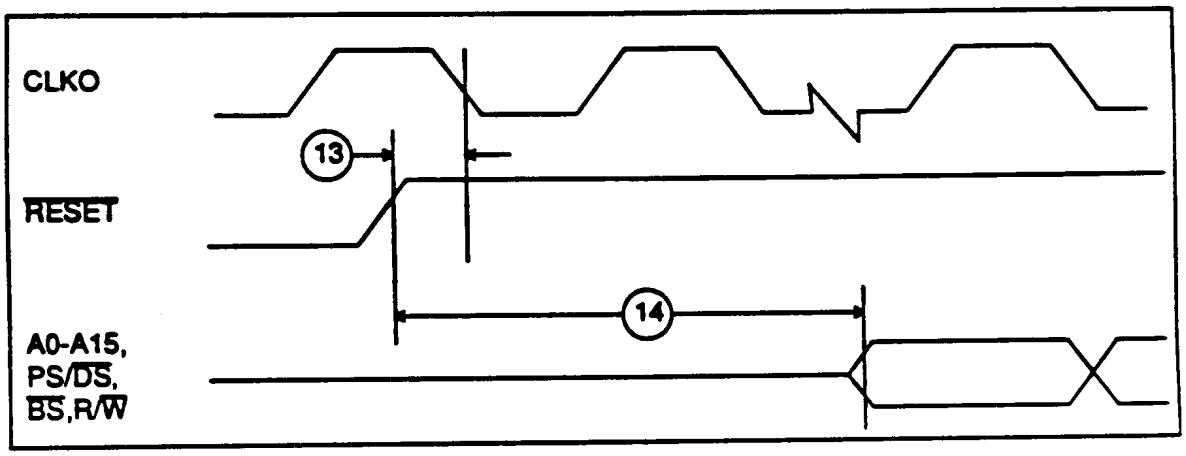
Num	Characteristics	40MHz		50MHz		60MHz		Unit
		Min	Max	Min	Max	Min	Max	
10	$\overline{\text{RESET}}$ Assertion to Address, Data and control signals High Impedance	—	25	—		—		ns
11	Minimum Stabilization Duration (see Note 1) (see Note 2)	600KT 50T	— —		— —		— —	ns ns
12	Asynchronous $\overline{\text{RESET}}$ Deassertion to First	16T	18T +15					ns
13	Synchronous Reset Setup Time from $\overline{\text{RESET}}$	3.5	2T+9					ns
14	Synchronous Reset Delay Time from CLK High to the First External Access	16T +7.5	16T +15					ns
15	Mode Select Setup Time	25	—		—		—	ns
16	Mode Select Hold Time	0	—		—		—	ns
17	Edge-Triggered Interrupt Request Width	9	—		—		—	ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid Caused by the Execution of the First Interrupt Instruction	19T +12	—		—		—	ns
19	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid Caused by the Execution of the First Interrupt Instruction	22T +14	—		—		—	ns
20	Delay from External Data Memory Address Ouput Valid	—	5T-12 +cyc*ws	—		—		ns
21	Delay from General-Purpose Output Valid Caused by the Execution of the First Interrupt Instruction to $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Deassertion for Level Sensitive Fast Interrupts — If 2nd Interrupt Instruction is: Single Cycle Two Cycles	 — —	 2T-14 2T-14 +2*cyc	 — —		 — —		ns

NOTES:

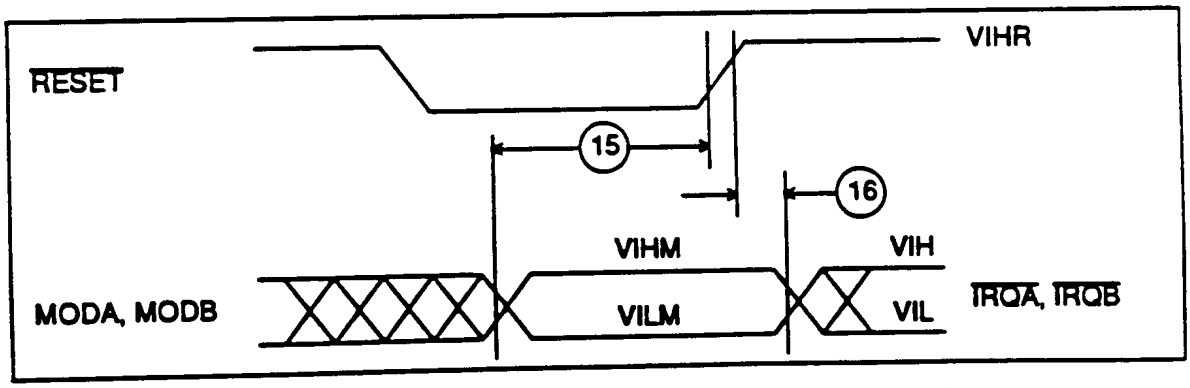
1. Circuit stabilization delay is required during reset when using an external clock in two cases: (1) after power-on reset, and (2) when recovering from Stop mode.
2. Timing specifications 18 through 21 apply only to $\overline{IRQA}$ and $\overline{IRQB}$ in level sensitive mode using fast interrupts to prevent multiple interrupt service. To avoid these timing restrictions, the negative edge triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using level sensitive mode.



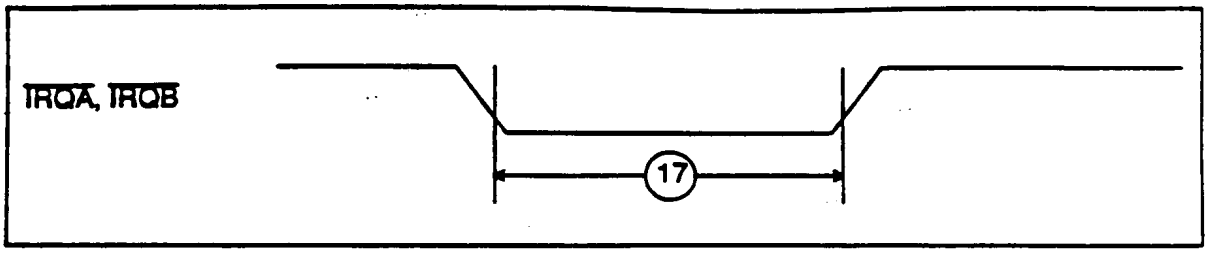
Interrupt Figure 1. Asynchronous Reset Timing



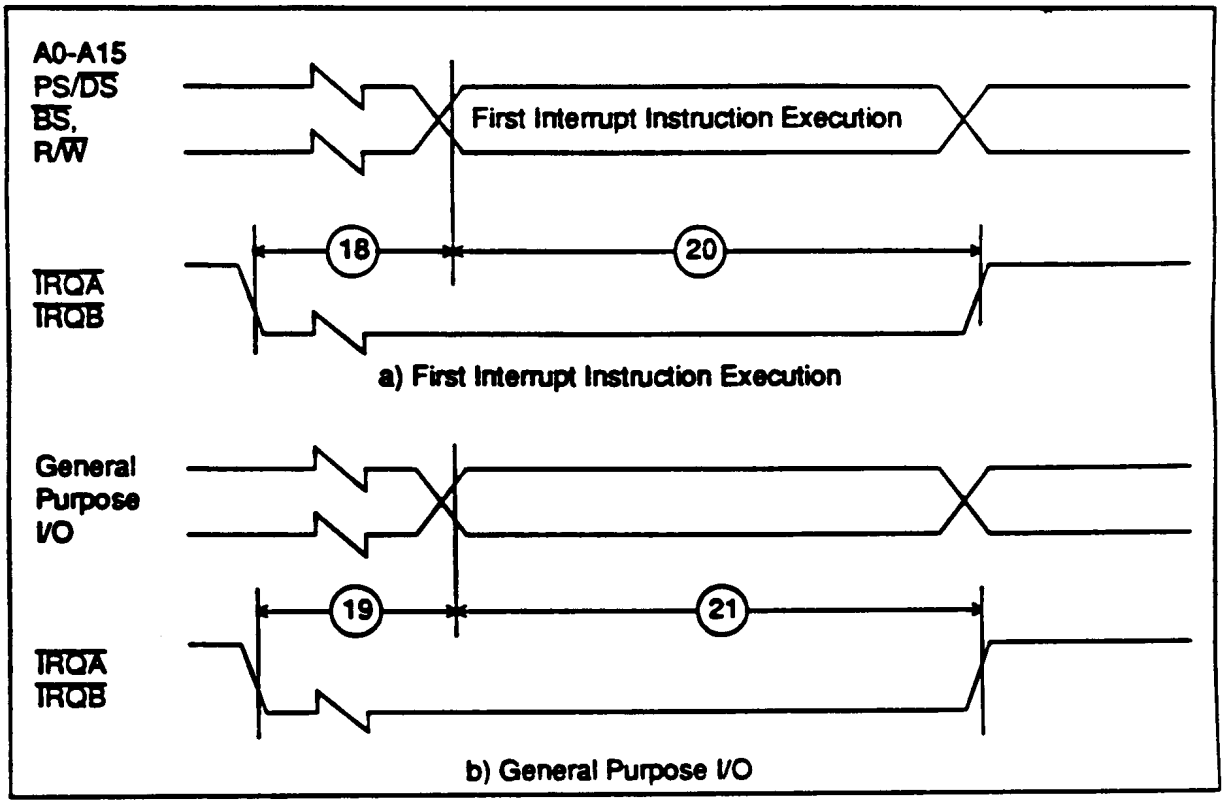
Interrupt Figure 2. Synchronous Reset Timing



Interrupt Figure 3. Operating Mode Select Timing



Interrupt Figure 4. External Interrupt Timing (Negative Edge-Triggered)



Interrupt Figure 5. External Level-Sensitive Fast Interrupt Timing

AC Electrical Characteristics
— Reset, Stop, Wait, Mode Select, and Interrupt Timing (Continued)

(Vdd = 5.0 Vdc +/- 10%, TA = -40 to +125 °C, CL = 50 pF + 1 TTL Load).

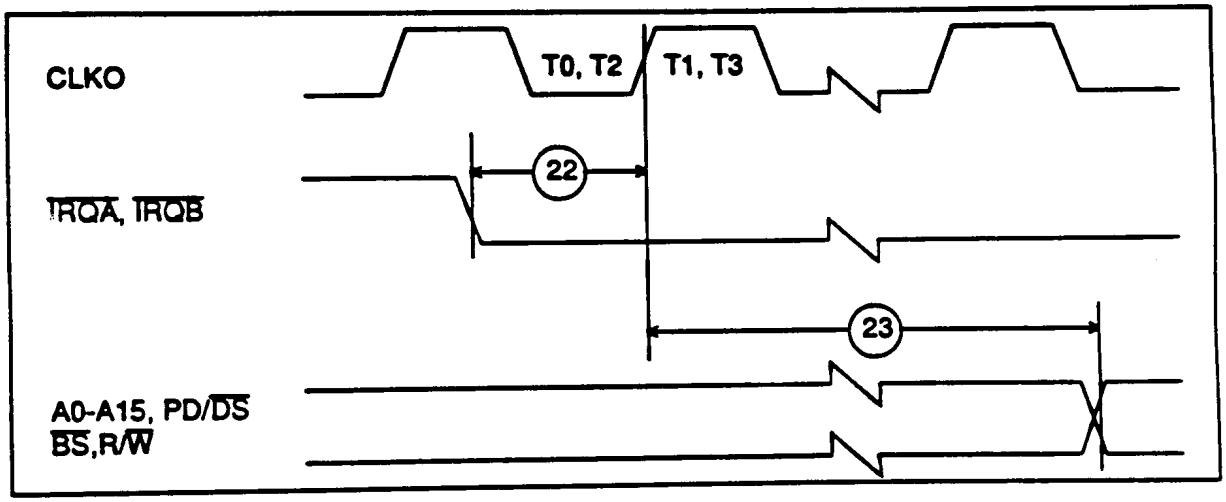
Num	Characteristics	40MHz		50MHz		60MHz		Unit
		Min	Max	Min	Max	Min	Max	
22	Synchronous setup time from $\overline{IRQA}$, $\overline{IRQB}$ assertion to Synchronous rising edge of CLKO (see note 4)	12	cyc-1					ns
23	CLKO high to First Interrupt Vector Address Out Valid after Synchronous recovery from Wait State (see Note 2,4)	27T+ tpd_{min}	27T+ tpd_{max}					ns
24	$\overline{IRQA}$ Width Assertion to Recover from STOP State(see note 3)	13	—		—		—	ns
25	Delay from $\overline{IRQA}$ Assertion to Fetch of first instruction (for STOP)(see note1) OMR bit 6 = 0 OMR bit 6 = 1	 262150 cyc 46T	 — —		 — —		 — —	 ns ns
28	Duration for Level Sensitive $\overline{IRQA}$ Assertion to Fetch of First $\overline{IRQA}$ Interrupt Instruction (forSTOP) — (see note1, 2) OMR bit 6 = 0 OMR bit 6 = 1	 tbd tbd	 tbd tbd					 ns ns
29	Delay from Level Sensitive $\overline{IRQA}$ Assertion toFirst Interrupt Vector Address Out Valid (for STOP) — (see note1, 2) OMR bit 6 = 0 OMR bit 6 = 1	 262150 cyc 46T	 — —		 — —		 — —	 ns ns

Notes:

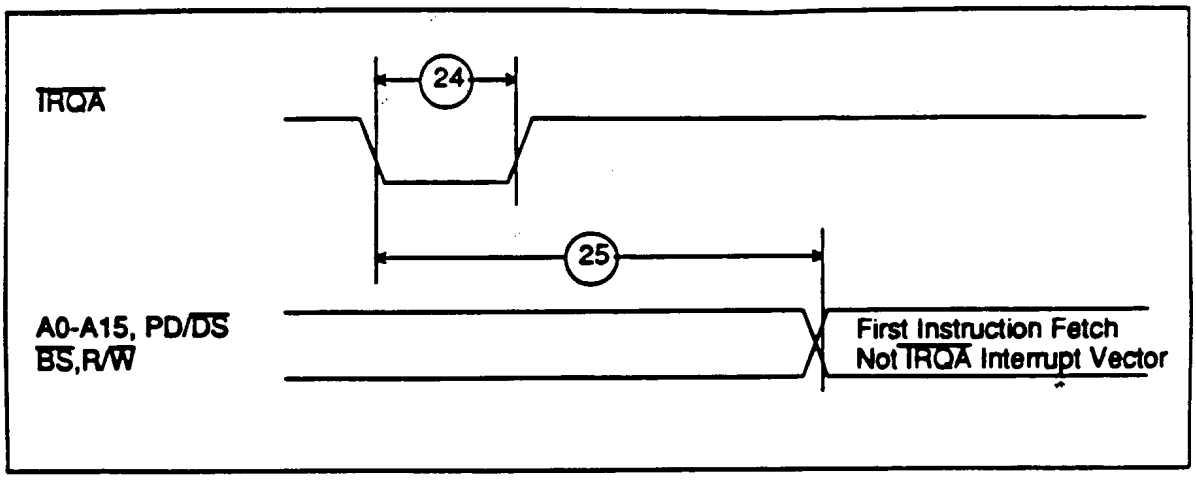
1. Circuit stabilization delay is required during reset when using an external clock in two cases:
   1) after power-on reset, and
   2) when recovering from Stop mode.
2. The interrupt instruction fetch is visible on the pins only in Mode 3.
3. The minimum is specified for the duration of an edge triggered $\overline{IRQA}$ interrupt required to recover from the STOP state without having the $\overline{IRQA}$ accepted.
4. Timing #22 is for all IRQx interrupts while timing #23 is only when exiting WAIT

AC Electrical Characteristics — Wait and Stop Timings (Continued)

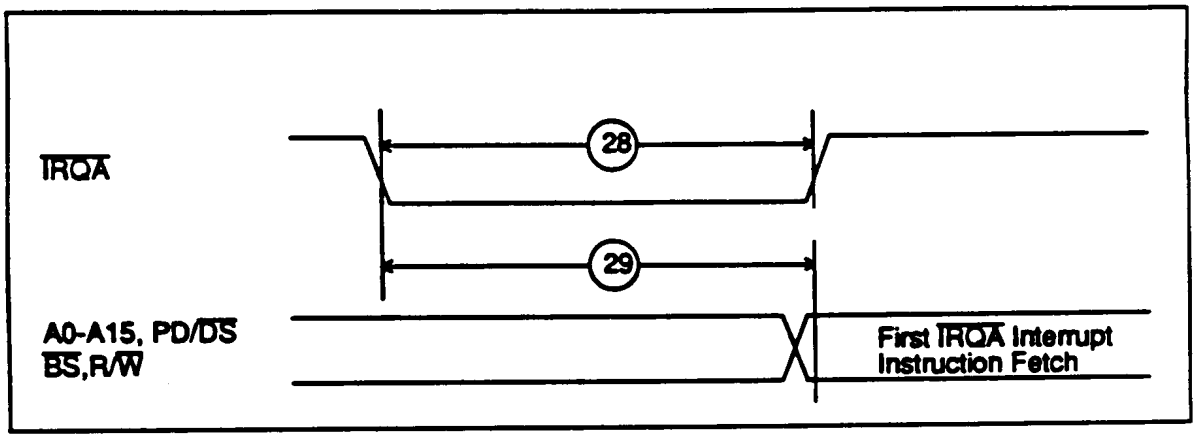
Num	Characteristics	40MHz		50MHz		60MHz		Unit
		Min	Max	Min	Max	Min	Max	
30	$\overline{DR}$ Asserted to CLK high (Setup Time for Synchronous Recovery from Stop or Wait State)	tbd	tbd	tbd	tbd	tbd	tbd	ns
31	CLK high to DSO ($\overline{ACR}$) Valid (Enter Debug Mode) - After Synchronous Recovery from Stop State -After Synchronous Recovery from Wait State	 tbd tbd	 tbd tbd	 tbd tbd	 tbd tbd	 tbd tbd	 tbd tbd	 ns ns
32	$\overline{DR}$ to DSO ($\overline{ACR}$) Valid (Enter Debug Mode) - After Asynchronous Recovery from Stop State - After Asynchronous Recovery from Wait State	 tbd tbd	 tbd tbd	 tbd tbd	 tbd tbd	 tbd tbd	 tbd tbd	ns ns
33	$\overline{DR}$ Assertion Width - to Recover from WAIT/STOP - to Recover from WAIT/STOP and enter debug mode	 tbd tbd	 tbd tbd	 tbd tbd	 tbd tbd	 tbd tbd	 tbd tbd	 ns ns



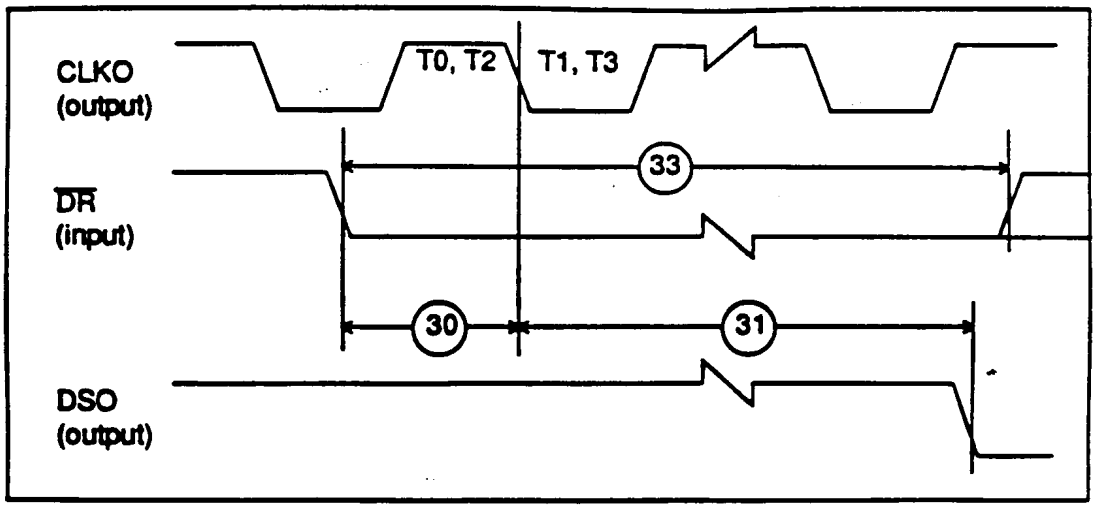
WAIT and STOP Figure 1. Synchronous Interrupt from Wait State Timing



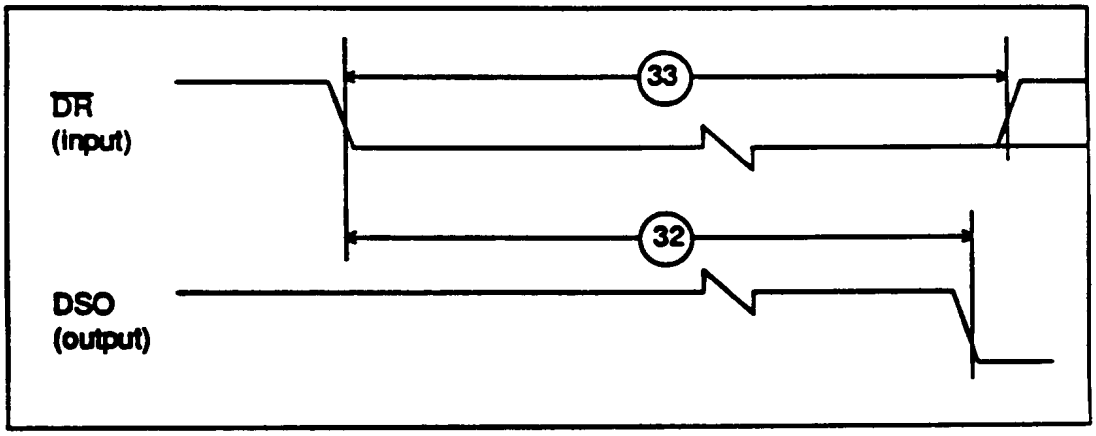
WAIT and STOP Figure 2.
Recovery fromSTOP State using Asynchronous Interrupt Timing



WAIT and STOP Figure 3.
Recovery from Stop State Using IRQA Interrupt Service



WAIT and STOP Figure 4.
Recovery from WAIT/STOP State Using $\overline{DR}$ Pin— Synchronous Timing



WAIT and STOP Figure 5.
Recovery from WAIT/STOP State Using $\overline{DR}$ Pin— Asynchronous Timing

AC Electrical Characteristics
Capacitance Derating —External Bus Synchronous Timing

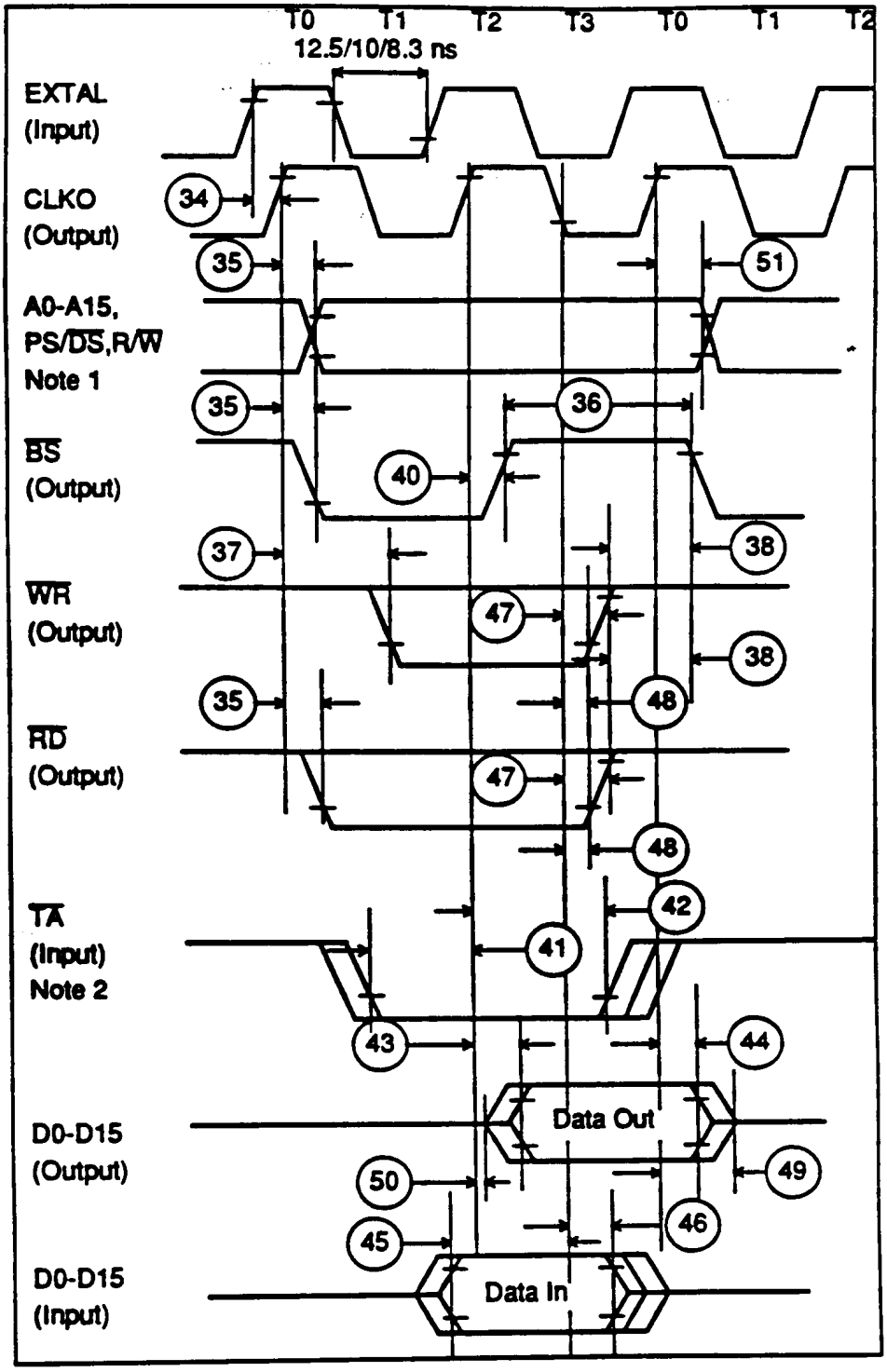
VCC = 5.0 Vdc +/- 10%, T_J = -40 to +125° C, CL = 50 pF + 1 TTL Load.

The DSP56156 External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the External Bus pins (A0-A15, D0-D23, PS/$\overline{DS}$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading.

When an internal memory access follows an external memory access, the PS/$\overline{DS}$, R/$\overline{W}$, $\overline{RD}$ and $\overline{WR}$ strobes remain deasserted and A0-A15 do not change from their previous state.

Num.	Characteristic	40MHz		50MHz		60MHz		Unit
		Min	Max	Min	Max	Min	Max	
34	CLK in (EXTAL) High to CLKO High	2.4	9	2.4	9	2.4	9	ns
35	CLKO High to a. A0-A15 Valid b.PS/$\overline{DS}$, R/$\overline{W}$ Valid $\overline{BS}$, $\overline{RD}$ Asserted	 4.7 4.7	 12 14	 4.7 4.7	 12 14	 4.7 4.7	 12[a] 14	 ns ns
36	$\overline{BS}$ Width deasserted	18.3	—	13.4	—	9.8	—	ns
37	CLKO High to $\overline{WR}$ Asserted Low	T+ 3.1	T+ 12.4	T+ 3.1	T+ 12.4	T+ 3.1	T+ 12.4	ns
38	$\overline{WR}$ and $\overline{RD}$ deasserted High to $\overline{BS}$ Asserted Low (2 Successive Bus Cycles)	14.3	15.8	11.8	13.3	10.2	11.8	ns
39								
40	CLKO High to $\overline{BS}$ deasserted	2.6	10.3	2.6	10.3	2.6	10.3	ns
41	$\overline{TA}$ Valid to CLKO High (Setup)	4.5	—	4.5	—	4.5	—	ns
42	CLKO High to $\overline{TA}$ Invalid (Hold)	0	—	0	—	0	—	ns
43	CLKO High to D0-D15 Out Valid	1.7	7.1	1.7	7.1	1.7	7.1	ns
44	CLKO High to D0-D15 Out Invalid	2.0	—	2.0	—	2.0	—	ns
45	D0-D15 In Valid to CLKO Low (Setup)	6	—	6	—	6	—	ns
46	CLKO Low to D0-D15 In Invalid (Hold)	0	—	0	—	0	—	ns
47	CLKO Low to $\overline{WR}$, $\overline{RD}$ deasserted	—	10.5	—	10.5	—	10.5	ns
48	$\overline{WR}$,$\overline{RD}$ Hold Time from CLKO Low	2.2	—	2.2	—	2.2	—	ns
49	CLKO High to D0-D15 Three-state	0	6	0	6	0	6	ns
50	CLKO High to D0-D15 Out Active	1.2	4.2	1.2	4.2	1.2	4.2	ns
51	CLKO High to A0-A15, PS/$\overline{DS}$, R/$\overline{W}$ Invalid	2.8	-	2.8	-	2.8	-	ns

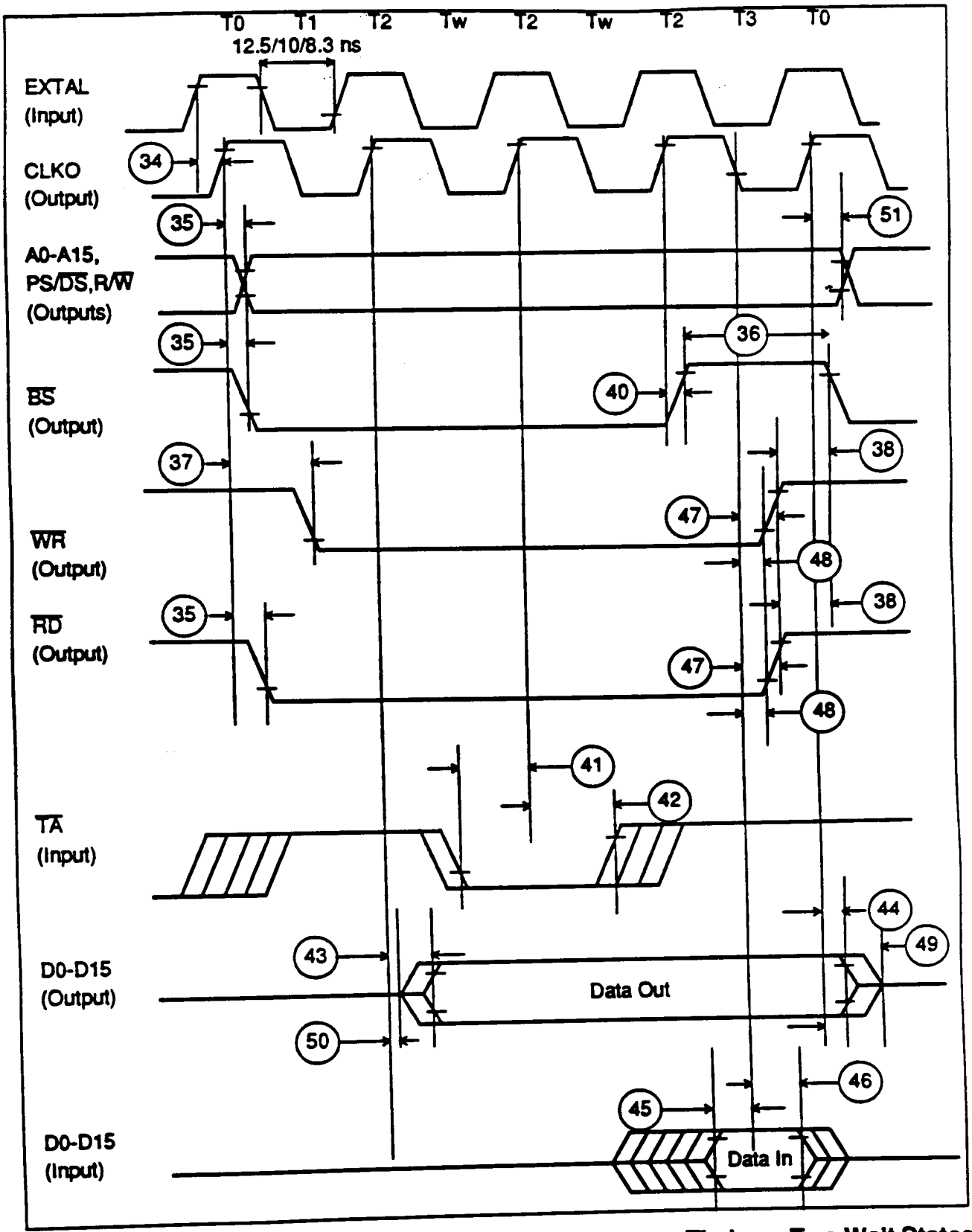
a. 10ns for CL=25 pF



Sync. External Bus Figure 1. External Bus Synchronous Timing — No Wait States

Note 1: During Read-Modify-Write instructions and internal instructions, the address lines do not change state

Note 2: $\overline{TA}$ sampled low during the leading edge of T2 can cause two actions:
- If the T2 is the last of the bus cycle (before T3), it will force zero wait states for the next bus cycle, if the next cycle is an external bus access
- If the T2 is preceding a Tw, it will terminate the current bus cycle within 4 Ts.



Sync. External Bus Figure 2. External Bus Synchronous Timing – Two Wait States

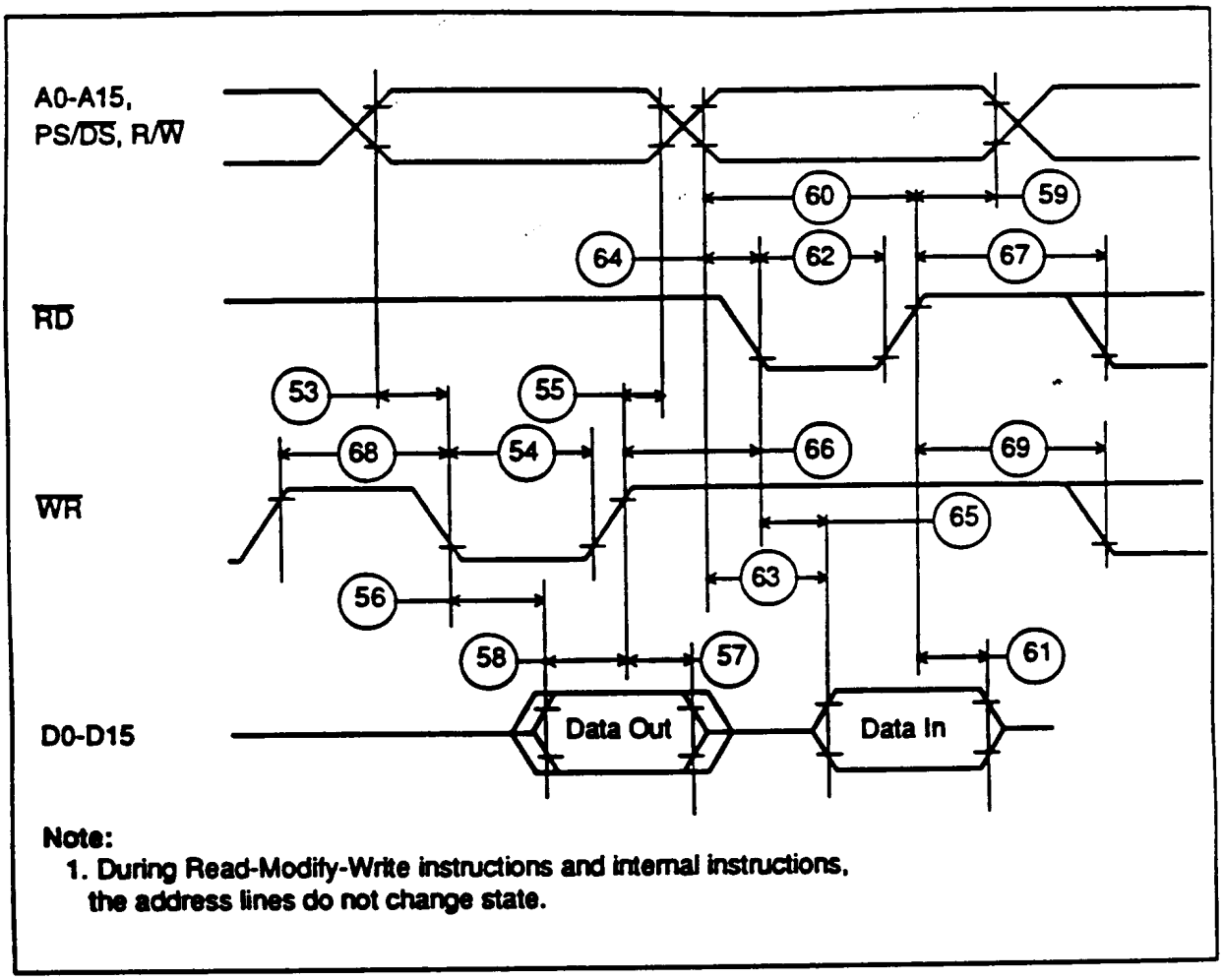
AC Electrical Characteristics
External Bus Asynchronous Timing

VCC = 5.0 Vdc +/- 10%, T_J = -40 to +125° C, CL = 50 pF + 1 TTL Load.

cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
WS = Number of Wait States, Determined by BCR Register (WS = 0 to 31)
WT = WS*cyc=2T*WS

Num.	Characteristic		40MHz		50MHz		60MHz		Unit
			Min	Max	Min	Max	Min	Max	
53	Address Valid to $\overline{WR}$ Asserted		13.2	16.7	10.8	14.2	9	12.6	ns
54	$\overline{WR}$ Width Asserted	WS=0 WS>0	20.2 WT+ 20.2	— —	15.1 WT+ 15.1	— —	11.8 WT+ 11.8	— —	ns
55	$\overline{WR}$ deasserted to R/$\overline{W}$, Address Invalid		9.7	—	7.3	—	5.7	—	ns
56	$\overline{WR}$ Asserted to D0-D15 Out Valid		7.1	11.0	4.5	8.4	2.8	6.9	ns
57	Data Out Hold Time from $\overline{WR}$ deasserted		6.3	11.5	3.7	9	2.2	7.7	ns
58	Data Out Set up Time to $\overline{WR}$ deasserted	WS=0 WS>0	13.7 WT+ 13.7	— —	11.3 WT+ 11.3	— —	9.5 WT+ 9.5	— —	ns
59	$\overline{RD}$ deasserted to Adress not valid		7.2	—	4.8	—	3.1	—	ns
60	Address valid to $\overline{RD}$ deasserted		37.9	—	30.5	—	25.3	—	ns
61	Input data hold to $\overline{RD}$ deasserted		0.0	—	0.0	—	0.0	—	ns
62	$\overline{RD}$ Assertion width	WS=0 WS>0	31.2 WT+ 31.2	— —	23.8 WT+ 23.8	— —	18.6 WT+ 18.6	— —	ns
63	Address valid to input data valid	WS=0 WS>0	— —	20 WT+ 20	— —	12 WT+ 12	— —	8[a] WT+ 8	ns
64	Address valid to $\overline{RD}$ Asserted		2.2	5.7	2.2	5.7	2.2	5.7	ns
65	$\overline{RD}$ asserted to input data valid	WS=0 WS>0	— —	20 WT+ 20	— —	12 WT+ 20	— —	8[b] WT+ 20	ns
66	$\overline{WR}$ deasserted to $\overline{RD}$ asserted		14.3	—	11.8	—	10.2	—	ns
67	$\overline{RD}$ deasserted to $\overline{RD}$ asserted		14.3	—	11.8	—	10.2	—	ns
68	$\overline{WR}$ deasserted to $\overline{WR}$ asserted		25.3	—	20.3	—	17.0	—	ns
69	$\overline{RD}$ deasserted to $\overline{WR}$ asserted		25.3	—	20.3	—	17.0	—	ns

a. 10 ns for CL=25 pF
b. 10 ns for CL=25 pF



Note:
1. During Read-Modify-Write instructions and internal instructions, the address lines do not change state.

Async. External Bus Figure 1. External Bus Asynchronous Timing

AC Electrical Characteristics — Bus Arbitration Timing — Slave Mode

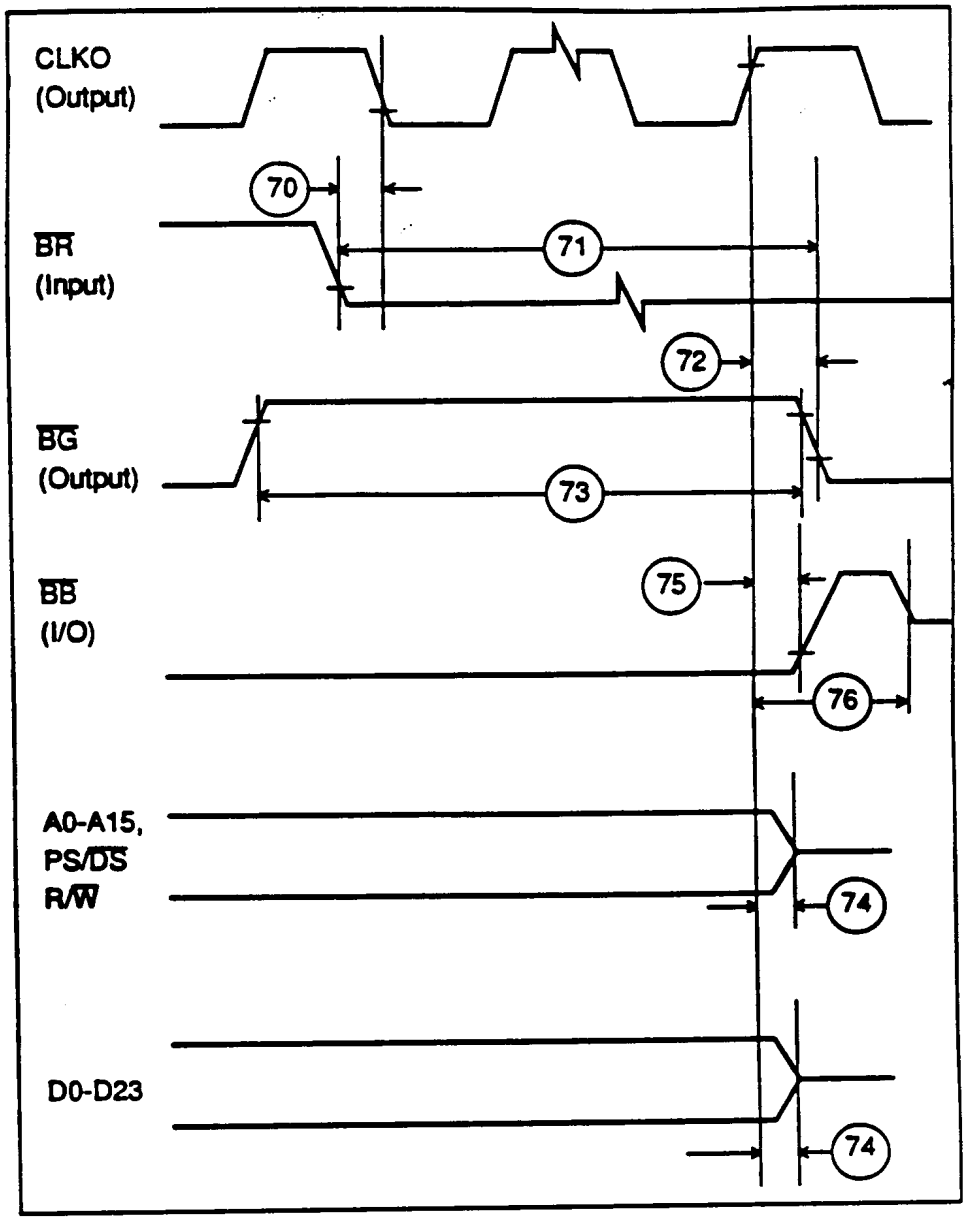
VCC = 5.0 Vdc +/- 10%, T_J = -40 to +125° C, CL = 50 pF + 1 TTL Load.

cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
WS = Number of Wait Statesfor X or P external memory , Determined by BCR Register (WS = 0 to 31)
WT = WS*cyc=2T*WS
Wx = Number of Wait States for X external memory, Determined by BCR Register (WS = 0 to 31)
Wp = Number of Wait States for P external memory, Determined by BCR Register (WS = 0 to 31)

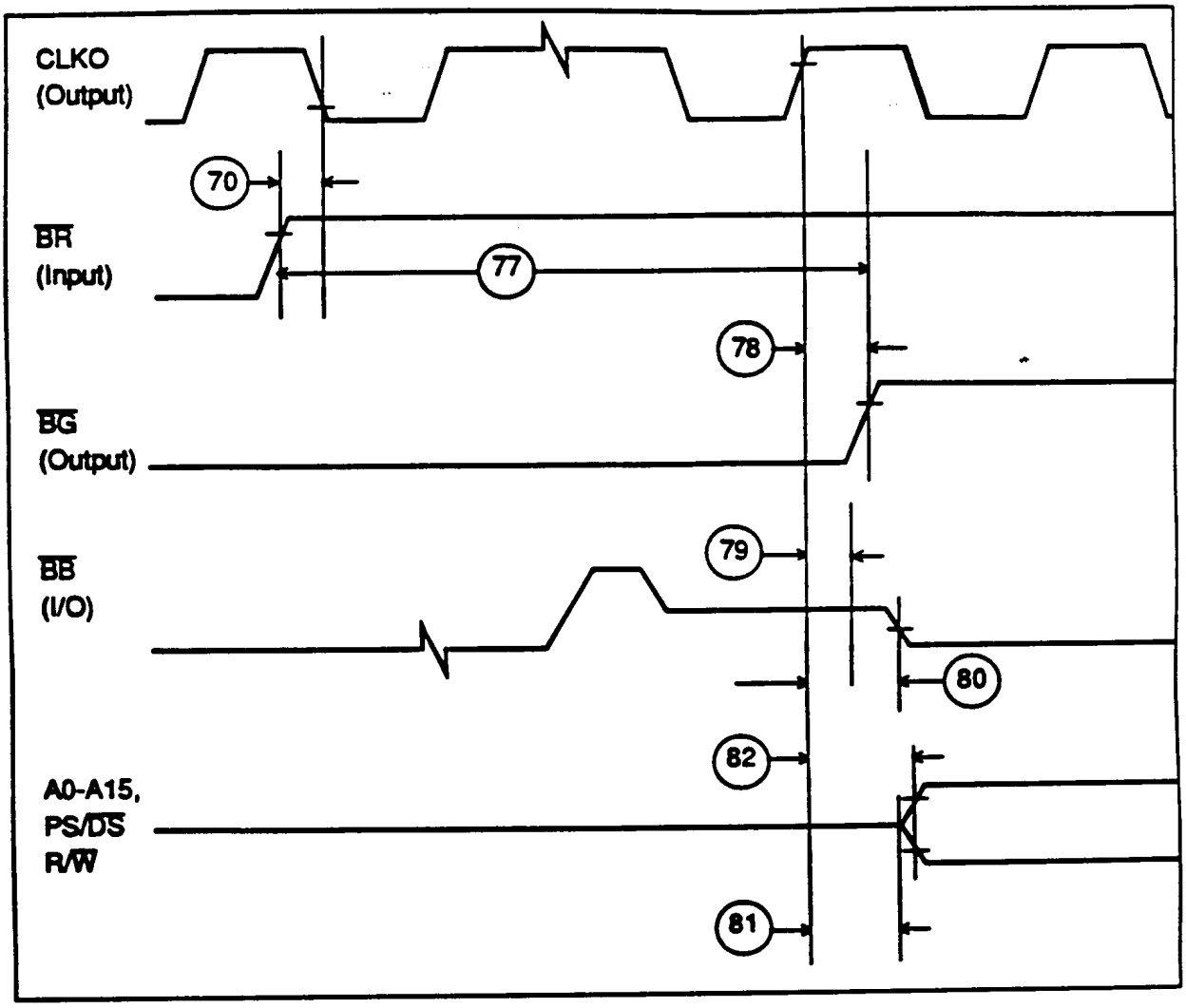
Num	Characteristics		40/50/60 MHz		Unit
			Min	Max	
70	$\overline{BR}$ Input to CLKO low setup time		0	1	ns
71	Delay from $\overline{BR}$ Input Assertion to $\overline{BG}$ Output Assertion	(See note 1) (See note 2) (See note 3) (See note 4) (See note 5)	5T+1.9 3T+1.9 5T+1.9 NA T+1.9	9T+4.2 6T+WT+4.2 26T+4T*Wx +2T*Wp+4.2 NA 3T+4.2	ns
72	CLKO high to $\overline{BG}$ Output Assertion		1.9	5.2	ns
73	$\overline{BG}$ Output Deassertion duration	(See note 1) (See note 5) (See note 7)	5T-0.5 2T-0.5 3T-0.5	— — —	ns
74	CLKO High to Control Bus high impedance		2.7	6.5	ns
75	CLKO High to $\overline{BB}$ Output Deassertion		3.2	7.8	ns
76	CLKO High to $\overline{BB}$ Input		3.3	8.1	ns
77	$\overline{BR}$ Input Deassertion to $\overline{BG}$ Output Deassertion	(See note 1) (See note 5) (See note 8)	4T+2.5 3T+3.2 3T+3.2	9T+6.4 8T+7.8 8T+8.0	ns
78	CLKO Low to $\overline{BG}$ Deassertion CLKO High to $\overline{BG}$ Deassertion CLKO High to $\overline{BG}$ Deassertion	(See note 1) (See note 5) (See note 8)	2.5 3.2 3.2	6.4 7.8 8.0	ns
79	CLKO High to $\overline{BB}$ Output Active		1.3	3.6	ns
80	CLKO High to $\overline{BB}$ Output Assertion		2.3	5	ns
81	CLKO High to Address and Control Bus Active		1	3	ns
82	CLKO High to Address and Control Bus Valid		2	4.4	ns

NOTES:

1. With no external access from the DSP56156
2. During external read or write access
3. During external read-modify-write access
4. During STOP mode — external bus is released and $\overline{BG}$ is always low
5. During WAIT mode
7. With external accesses pending by the DSP56156
8. Slave mode, when bus is still busy after bus request has been deasserted



Slave Arbitration Figure 1. Bus Arbitration Timing — Slave Mode — Bus Release.

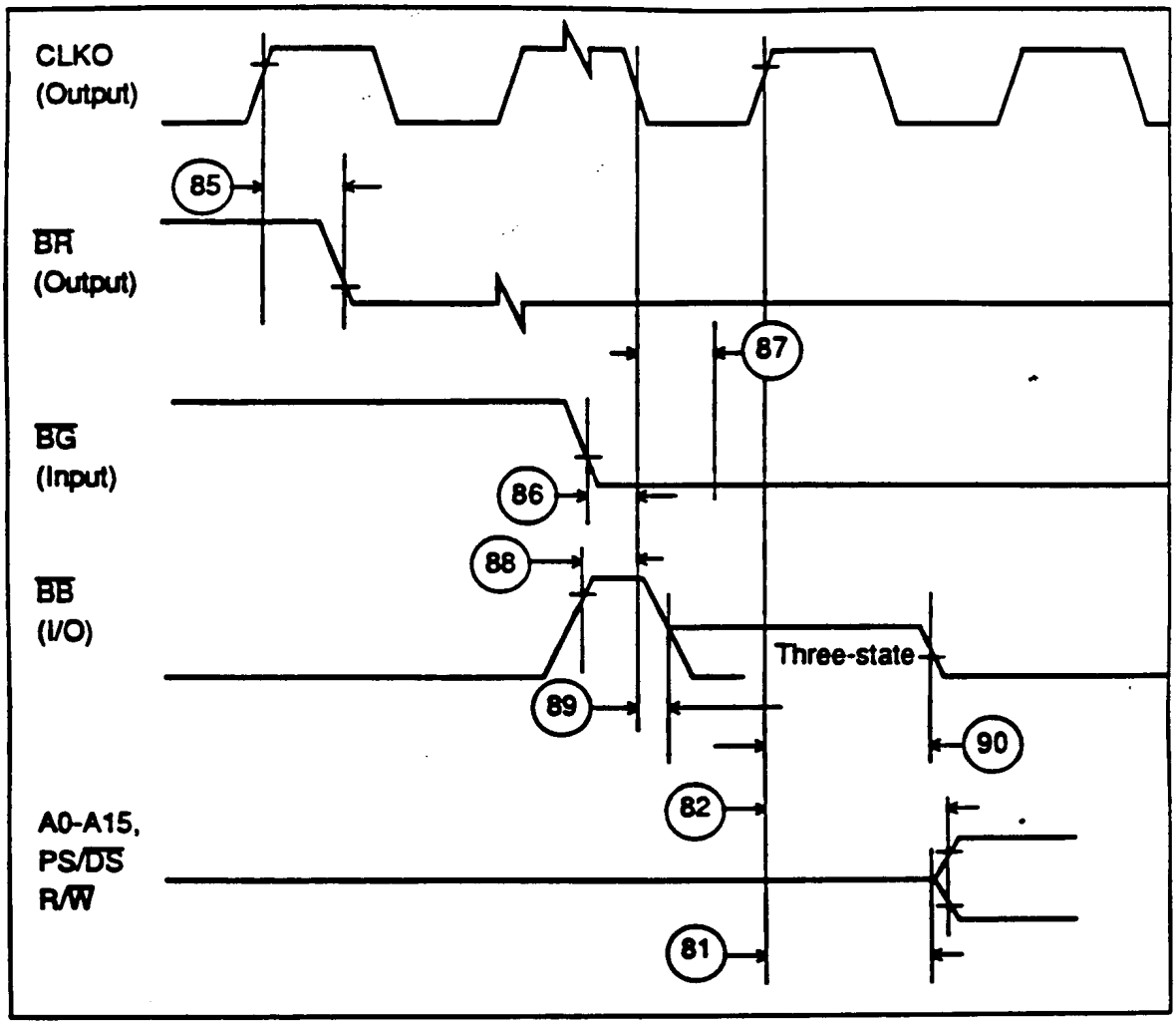


Slave Arbitration Figure 2.
Bus Arbitration Timing — Slave Mode — Bus Acquisition.

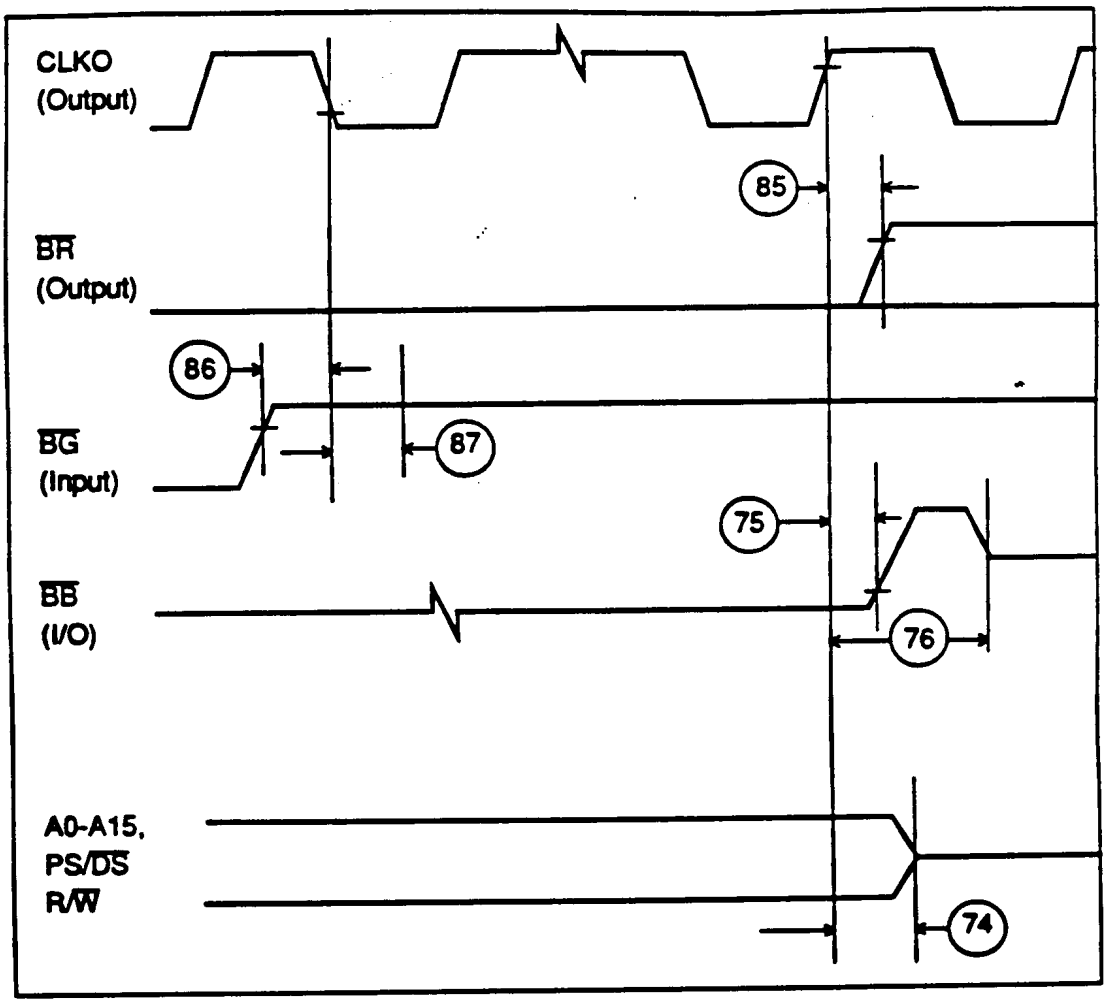
AC Electrical Characteristics — Bus Arbitration Timing — Master Mode

VCC = 5.0 Vdc +/- 10%, T_J = -40 to +125° C, CL = 50 pF + 1 TTL Load.

Num.	Characteristic	40MHz		50MHz		60MHz		Unit
		Min	Max	Min	Max	Min	Max	
85	CLKO high to $\overline{BR}$ Output Assertion CLKO high to $\overline{BR}$ Output Deassertion	2.1	8.5	2.1	8.5	2.1	8.5	ns
86	$\overline{BG}$ Input Asserted/ Deasserted to CLKO Low (Setup)	9.2	—	6.5	—	4.5	—	ns
87	CLKO Low to $\overline{BG}$ Input Invalid (Hold)	0	—	0	—	0	—	ns
88	$\overline{BB}$ Input Deasserted to CLKO Low (Setup)	9.2	—	6.5	—	4.5	—	ns
89	CLKO Low to $\overline{BB}$ Input Deasserted (Hold)	0	—	0	—	0	—	ns
90	CLKO High to $\overline{BB}$ Output Asserted	2.1	5.9	2.1	5.9	2.1	5.9	ns



Master Arbitration Figure 1.
Bus Arbitration Timing — Master Mode — Bus Acquisition.



Master Arbitration Figure 2.
Bus Arbitration Timing — Master Mode — Bus Release.

HOST PORT USAGE CONSIDERATIONS

Careful synchronization is required when reading multibit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected. The situation exists in the Host port. The considerations for proper operation are discussed below.

Host Programmer Considerations

1. Unsynchronized Reading of Receive Byte Registers
   When reading receive byte registers, RXH or RXL, the Host programmer should use interrupts or poll the RXDF flag which indicates that data is available. This assures that the data in the receive byte registers will be stable.

2. Overwriting Transmit Byte Registers
   The Host programmer should not write to the transmit byte registers, TXH or TXL, unless the TXDE bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the HRX register.

3. Synchronization of Status Bits from DSP to Host
   HC, HREQ, DMA, HF3, HF2, TRDY, TXDE, and RXDF (refer to *DSP56156 User's Manual*, I/O Interface section, Host/DMA Interface Programming Model for descriptions of these status bits) status bits are set or cleared from inside the DSP and read by the Host processor. The Host can read these status bits very quickly without regard to the clock rate used by the DSP, but the possibility exists that the state of the bit could be changing during the read operation. This is generally not a system problem, since the bit will be read correctly in the next pass of any Host polling routine.
   However, if the Host asserts the $\overline{\text{HEN}}$ for more than timing number 101a (T101a), with a minimum cycle time of timing number 102a (T102a), then the status is guaranteed to be stable
   A potential problem exists when reading status bits HF3 and HF2 as an encoded pair. If the DSP changes HF3 and HF2 from 00 to 11, there is a small probability that the Host could read the bits during the transition and receive 01 or 10 instead of 11. If the combination of HF3 and HF2 has significance, the Host could read the wrong combination.
   Solution:
   a. Read the bits twice and check for consensus.
   b. Assert $\overline{\text{HEN}}$ access for T101a so that status bit transitions are stabilized.

4. Overwriting the Host Vector
   The Host programmer should change the Host Vector register only when the Host Command bit (HC) is clear. This change will guarantee that the DSP interrupt control logic will receive a stable vector.

5. Cancelling a Pending Host Command Exception
   The Host processor may elect to clear the HC bit to cancel the Host Command Exception request at any time before it is recognized by the DSP. Because the Host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the Host exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time the HC bit is cleared.

DSP Programmer Considerations

1. Reading HF0 and HF1 as an Encoded Pair
   DMA, HF1, HF0, and HCP, HTDE, and HRDF (refer to *DSP56156User's Manual*, I/O Interface section, Host/DMA Interface Programming Model for descriptions of these status bits) status bits are set or cleared by the Host processor side of the interface. These bits are individually synchronized to the DSP clock.
   A potential problem exists when reading status bits HF1 and HF2 as an encoded pair, i.e., the four combinations 00, 01, 10, and 11 each have significance. A very small probability exists that the DSP will read the status bits synchronized during transition. The solution to this potential problem is to read the bits twice for consensus.

AC Electrical Characteristics — Host I/O Timing

(VCC = 5.0 Vdc +/- 10%, TJ = -40° to +125° C, CL = 50 pF + 1 TTL Load, see Host Figures 1 through 6)
T = Icyc / 4
cyc=Clock cycle =1/2 instruction cycle= 2 T cycle
tHSDL = Host Synchronization Delay Time
t_{suh} : Host processor data setup time
Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications

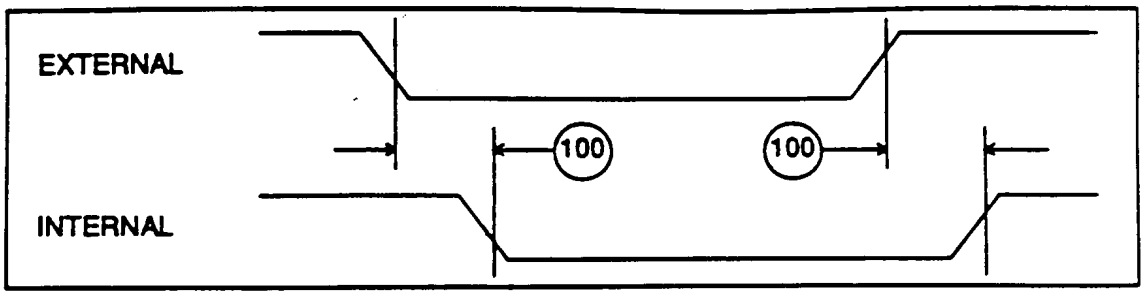
Num.	Characteristic	40MHz		50MHz		60MHz		Unit
		Min	Max	Min	Max	Min	Max	
100	Host Synchronous Delay (see Note 1)	T	3T	T	3T	T	3T	ns
101	HEN/HACK Assertion Width (see Note 2) a.CVR,ICR, IDR Read b.Read c.Write	2T+30 25+t_{suh} 20	 — —	2T+30 25+t_{suh} 20	 — —	2T+30 25+t_{suh} 20	 — —	ns
102	HEN/HACK Deassertion Width (see Note 2)	25	—	25	—	25	—	ns
103	Minimum Cycle Time Between Two HEN Assertion for Consecutive CVR, ICR, ISR reads	4T+30	—	4T+30	—	4T+30	—	ns
104	Host Data Input Setup Time Before HEN/HACK Deassertion	3	—	3	—	3	—	ns
105	Host Data Input Hold Time After HEN/HACK Deassertion	5	—	5	—	5	—	ns
106	HEN/HACK Assertion to Output Data Activefrom High Impedance	0	—	0	—	0	—	ns
107	HEN/HACK Assertion to Output Data Valid	—	25	—	25	—	25	ns
108	HEN/HACK Deassertion to Output Data High Impedance	—	15	—	15	—	15	ns
109	Output Data Hold Time After HEN/HACK Deassertion	5	—	5	—	5	—	ns

AC Electrical Characteristics — Host I/O Timing (Continued)

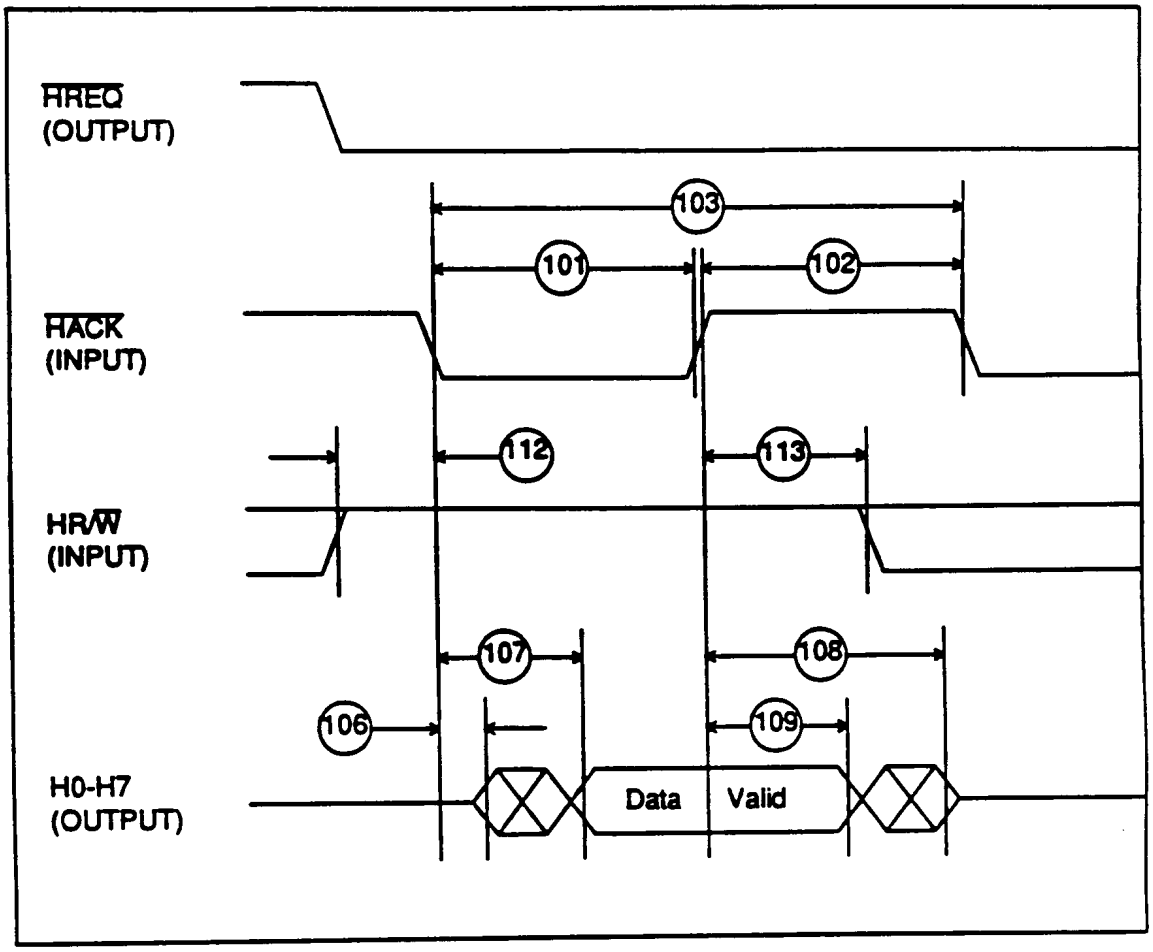
Num	Characteristic	40MHz		50MHz		60MHz		Unit
		Min	Max	Min	Max	Min	Max	
110	HR/$\overline{W}$ Low Setup Time Before $\overline{HEN}$ Assertion	0	—	0	—	0	—	ns
111	HR/$\overline{W}$ Low Hold Time After $\overline{HEN}$ Deassertion	4	—	4	—	4	—	ns
112	HR/$\overline{W}$ High Setup Time to $\overline{HEN}$ Assertion	0	—	0	—	0	—	ns
113	HR/$\overline{W}$ High Hold Time After $\overline{HEN}$/$\overline{HACK}$ Deassertion	3	—	3	—	3	—	ns
114	HA0-HA2 Setup Time Before $\overline{HEN}$ Assertion	0	—	0	—	0	—	ns
115	HA0-HA2 Hold Time After $\overline{HEN}$ Deassertion	6	—	6	—	6	—	ns
116	DMA $\overline{HACK}$ Assertion to $\overline{HREQ}$ Deassertion(see Note 3)	5	2T +35	5	2T +35	5	2T +35	ns
117	DMA $\overline{HACK}$ Deassertion to $\overline{HREQ}$ Assertion(see Note 3)							
	for DMA RXL Read	t_{HSDL} +3T+5	—	t_{HSDL} +3T+5	—	t_{HSDL} +3T+5	—	ns
	for DMA TXL Write	t_{HSDL} +2T+5	—	t_{HSDL} +2T+5	—	t_{HSDL} +2T+5	—	ns
	for All Other Cases	5	—	5	—	5	—	ns
118	Delay from $\overline{HEN}$ Deassertion to $\overline{HREQ}$ Assertion for RXL Read (see Note 3)	t_{HSDL} +3T+5	—	t_{HSDL} +3T+5	—	t_{HSDL} +3T+5	—	ns
119	Delay from $\overline{HEN}$ Deassertion to $\overline{HREQ}$ Assertion for TXL Write (see Note 3)	t_{HSDL} +2T+5	—	t_{HSDL} +2T+5	—	t_{HSDL} +2T+5	—	ns
120	Delay from $\overline{HEN}$ Assertion to $\overline{HREQ}$ Deassertion for RXL Read, TXL Write (see Note 3)	5	2T +35	5	2T +35	5	2T +35	ns

NOTES:

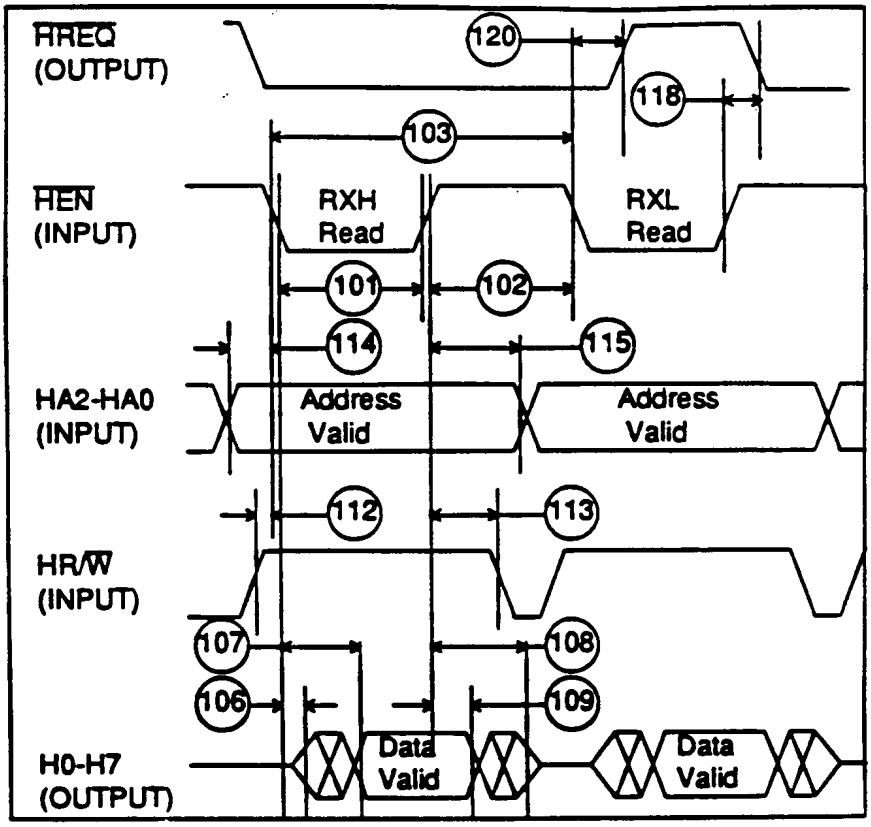
1. "Host synchronization delay (tHSDL)" is the time period required for the DSP56156 to sample any external asynchronous input signal, determine whether it is high or low, and synchronize it to the internal clock.
2. See **HOST PORT USAGE CONSIDERATIONS**.
3. $\overline{HREQ}$ is pulled up by 1kΩ.



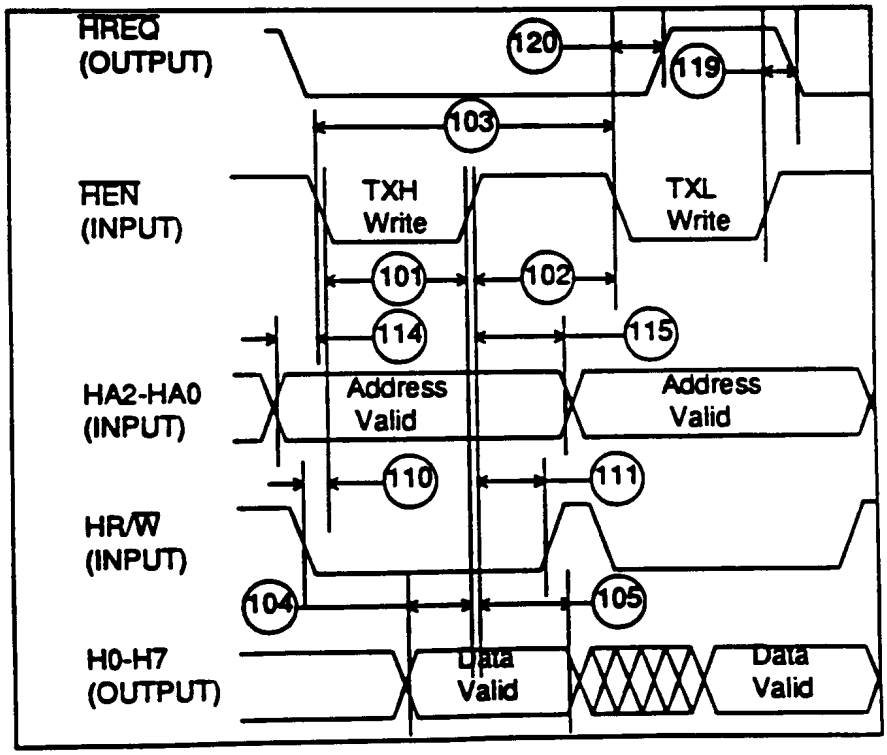
Host Figure 1. Host Synchronization Delay



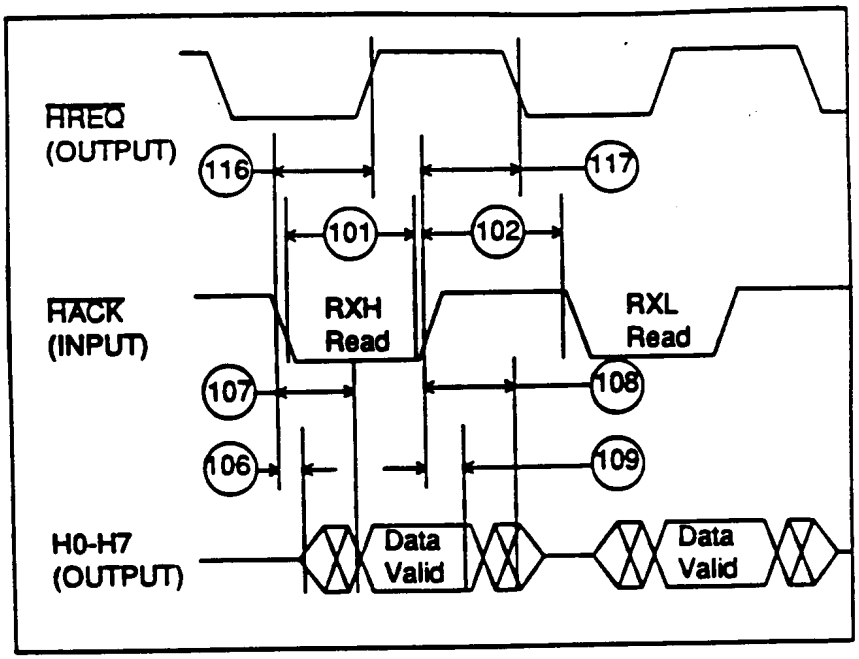
Host Figure 2. Host Interrupt Vector Register (IVR) Read



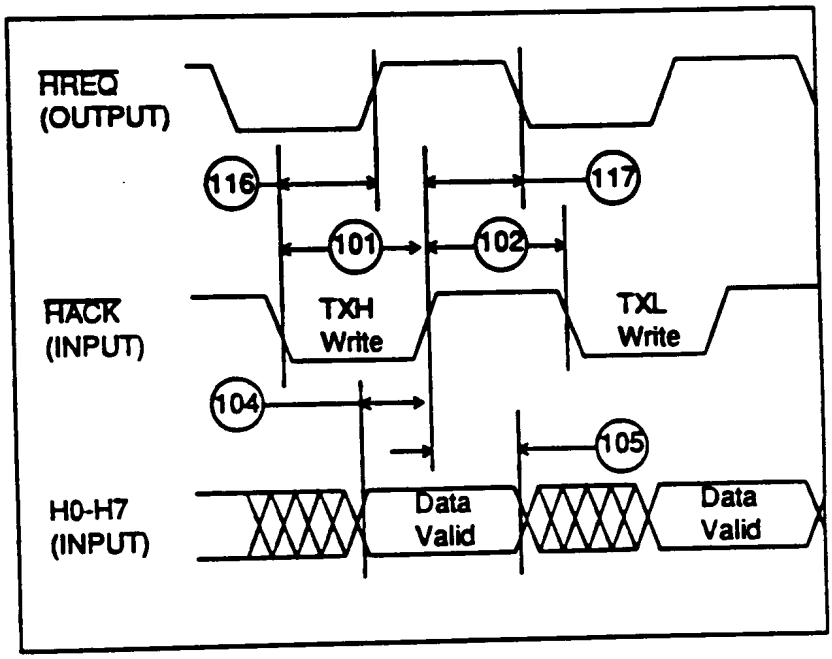
Host Figure 3. Host Read Cycle (Non-DMA Mode)



Host Figure 4. Host Write Cycle (Non-DMA Mode)



Host Figure 5. Host DMA Read Cycle



Host Figure 6. Host DMA Write Cycle

AC Electrical Characteristics — SSI Timing

(VCC = 5.0 Vdc +/- 10%, TJ = -40° to + 125° C, CL = 50 pF + 1 TTL Load, see SSI Figure 1 and 2)

T = Icyc / 4
SCK Pin = Serial Clock
FST (SCx0 Pin) = Transmit Frame Sync
FSR (SCx1 Pin) = Receive Frame Sync
i ck = Internal Clock
x ck = External Clock
i ck a = Internal Clock, Asynchronous Mode (Asynchronous implies that FSR and FST are two different frame sync)
i ck s = Internal Clock, Synchronous Mode (Synchronous implies that only one frame sync FS is used)
bl = bit length
wl = word length

NOTE:
All the timings for the SSI are given for a non-inverted serial clock polarity (SCKP=0 in CRB) and a non-inverted frame sync (FSI=0 in CRB). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK and/or the frame sync FSR/FST in the tables and in the figures.

Num.	Characteristic	40MHz		50MHz		60MHz		Case	Unit
		Min	Max	Min	Max	Min	Max		
130	Clock Cycle (see Note 1)	100	—		—		—	—	ns
131	Clock High Period	50	—		—		—	—	ns
132	Clock Low Period	50	—		—		—	—	ns
133	Output Clock Rise/Fall Time	—	4	—		—		—	ns
134	SCK Rising Edge to FSR Out (bl) High	— —	30 15	— —		— —		x ck i ck a	ns
135	SCK Rising Edge to FSR Out (bl) Low	— —	25 5	— —		— —		x ck i ck a	ns
136	SCK Rising Edge to FSR Out (wl) High	— —	27 8	— —		— —		x ck i ck a	ns
137	SCK Rising Edge to FSR Out (wl) Low	— —	27 6	— —		— —		x ck i ck a	ns
138	Data In Setup Time Before SCK Falling Edge	30 20 20	— — —		— — —		— — —	x ck i ck a i ck s	ns
139	Data In Hold Time After SCK Falling Edge	25 15	— —		— —		— —	x ck i ck s	ns

AC Electrical Characteristics — SSI Timing (Continued)

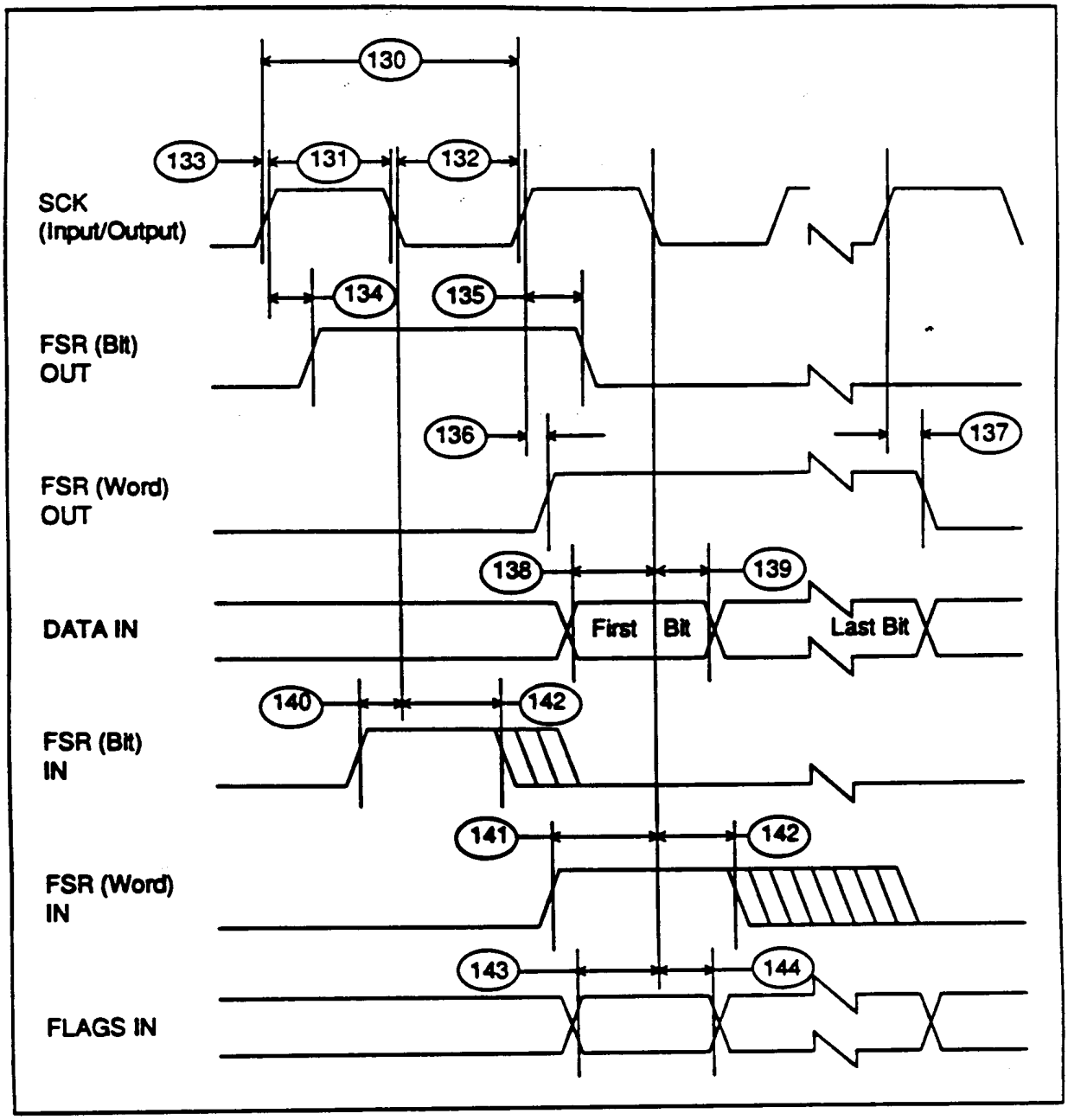
Num.	Characteristic	40MHz		50MHz		60MHz		Case	Unit
		Min	Max	Min	Max	Min	Max		
140	FSR Input (bl) High Before SCK Falling Edge	25 15	— —		— —		— —	x ck i ck a	ns
141	FSR Input (wl) High Before SCK Falling Edge	25 15	— —		— —		— —	x ck i ck a	ns
142	FSR Input Hold Time After SCK Falling Edge	30 10	— —		— —		— —	x ck i ck a	ns
143	Flags Input Setup Before SCK Falling Edge	25 15	— —		— —		— —	x ck i ck a	ns
144	Flags Input Hold Time After SCK Falling Edge	25 10	— —		— —		— —	x ck i ck a	ns
145	SCK Rising Edge to FST Out (bl) High	— —	30 12	— —		— —		x ck i ck	ns
146	SCK Rising Edge to FST Out (bl) Low	— —	25 8	— —		— —		x ck i ck	ns
147	SCK Rising Edge to FST Out (wl) High	— —	27 8	— —		— —		x ck i ck	ns
148	SCK Rising Edge to FST Out (wl) Low	— —	27 8	— —		— —		x ck i ck	ns
149	SCK Rising Edge to Data Out Enable from High Impedance	— —	25 8	— —		— —		x ck i ck	ns

AC Electrical Characteristics — SSI Timing (Continued)

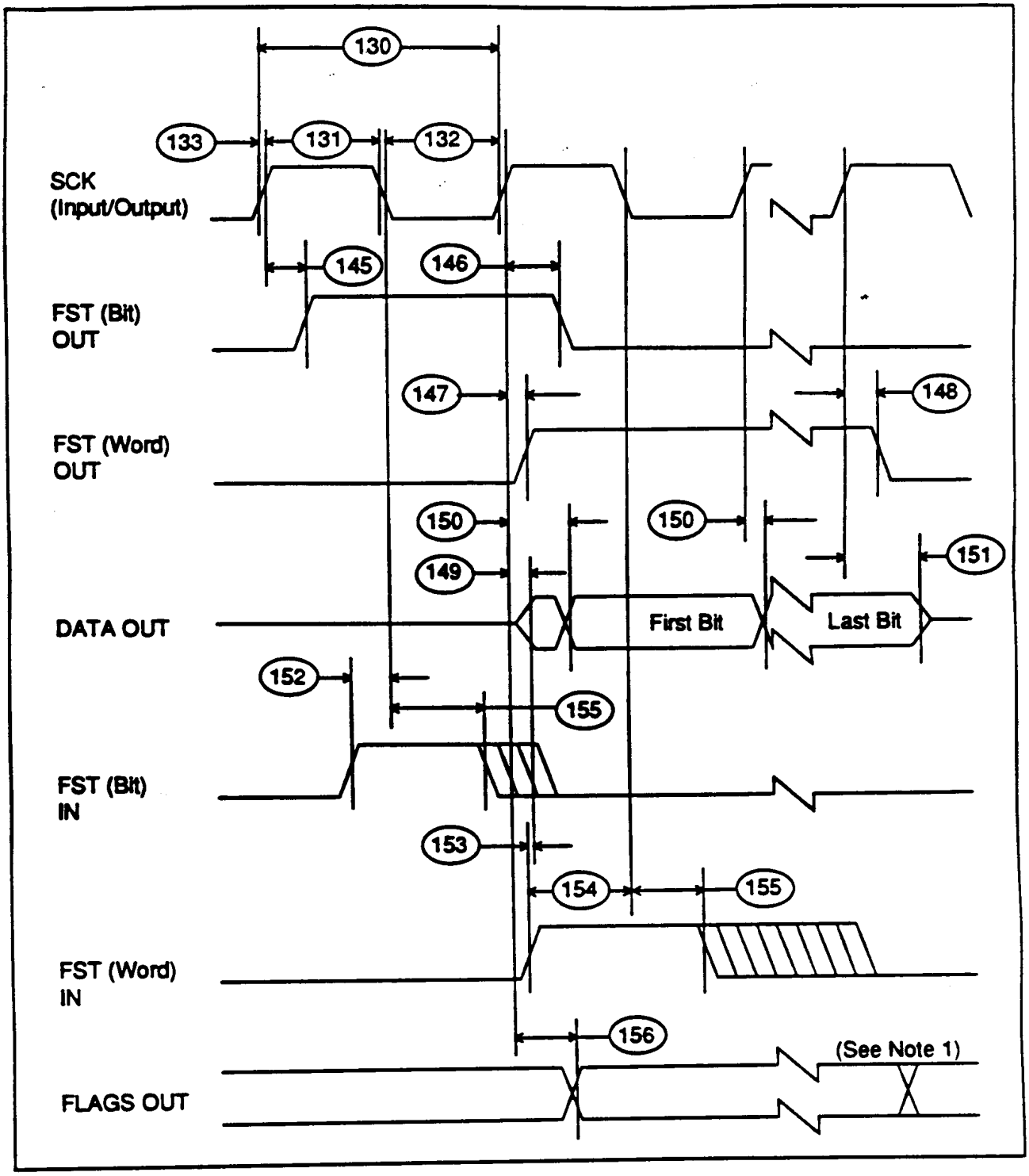
Num.	Characteristic	40MHz		50MHz		60MHz		Case	Unit
		Min	Max	Min	Max	Min	Max		
150	SCK Rising Edge to Data Out Valid	— —	25 8	— —		— —		x ck i ck	ns
151	SCK Rising Edge to Data Out High Impedance	— —	30 30	— —		— —		x ck i ck	ns
152	FST Input (bl) Setup Time Before SCK Falling Edge	30 25	— —		— —		— —	x ck i ck	ns
153	FST Input (wl) to Data Out Enable from High Impedance	—	24	—		—		—	ns
154	FST Input (wl) Setup Time Before SCK Falling Edge	30 25	— —		— —		— —	x ck i ck	ns
155	FST Input Hold Time After SCK Falling Edge	25 6	— —		— —		— —	x ck i ck	ns
156	Flag Output Valid After SCK Rising Edge	— —	26 5	— —		— —		x ck i ck	ns

NOTES:

1. For internal clock, External Clock Cycle is defined by Icyc and SSI control register.



SSI Figure 1. SSI Receiver Timing



SSI Figure 2. SSI Transmitter Timing

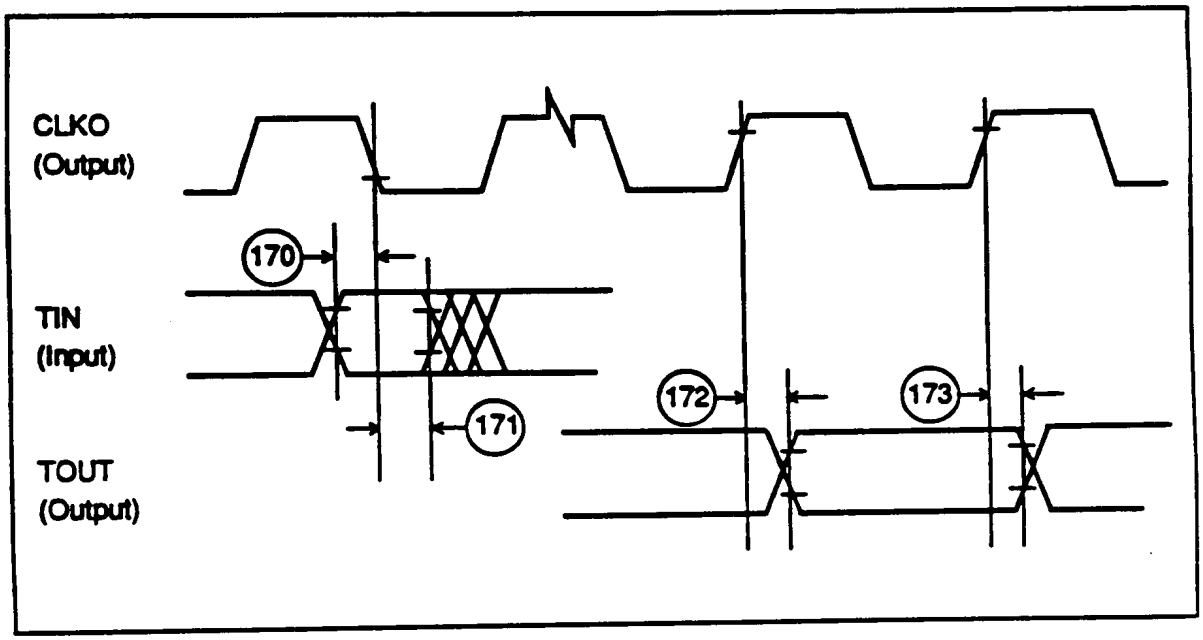
NOTE:

1. In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

AC Electrical Characteristics — Timer Timing

(VCC = 5.0 Vdc +/- 10%, TJ = -40 to +125 °C, CL = 50 pF + 1 TTL Load).

Num.	Characteristic	40MHz		50MHz		60MHz		Unit
		Min	Max	Min	Max	Min	Max	
170	TIN Valid to CLKO low (Setup time)	6	—	6	—	6	—	ns
171	CLKO Low to TIN Invalid (Hold time)	0	—	0	—	0	—	ns
172	CLKO High to TOUT Asserted	3.5	14	3.5	14	3.5	14	ns
173	CLKO High to TOUT Deasserted	5.1	20.7	5.1	20.7	5.1	20.7	ns
174	Tin Period	8T	—	8T	—	8T	—	ns
175	Tin High/Low Period	4T	—	4T	—	4T	—	ns



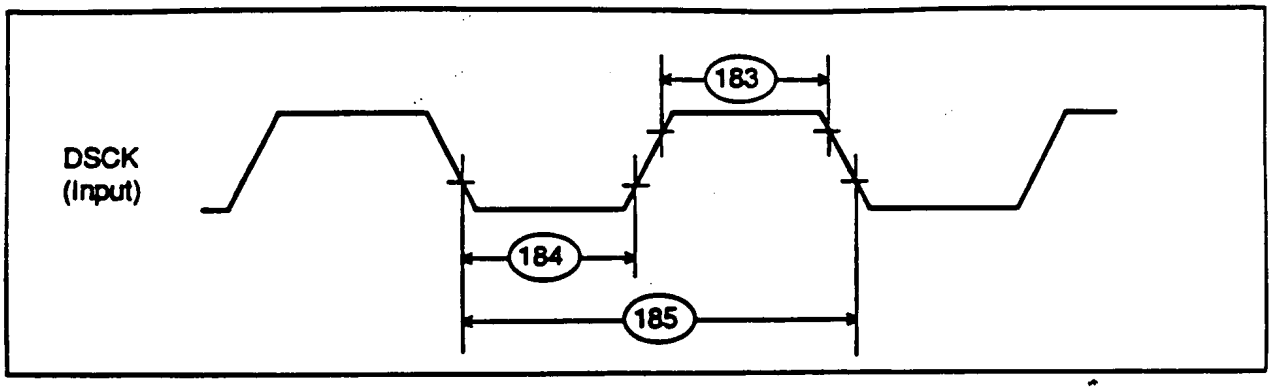
Timer Figure 1. Timer Timing

AC Electrical Characteristics — OnCE Timing

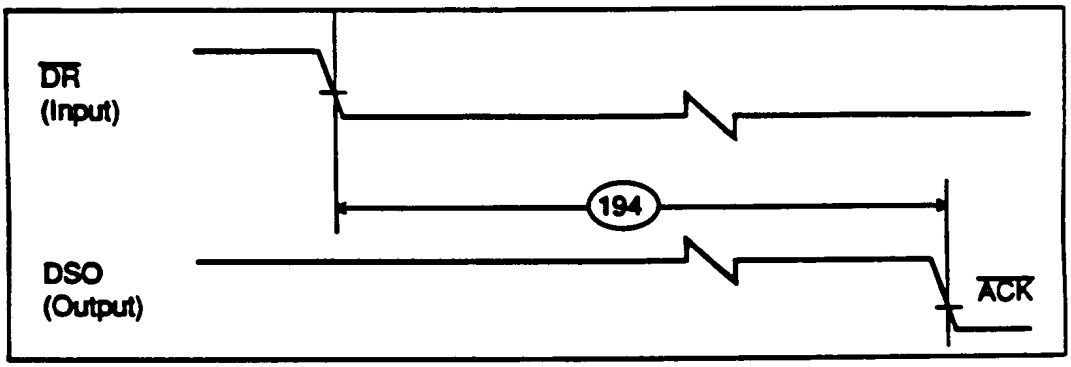
VCC = 5.0 Vdc +/- 10%, TJ = -40° to +125° C, CL = 50 pF + 1 TTL Load).

Num.	Characteristic	40/50/60 MHz		Unit
		Min	Max	
180	DSCK High to DSO Valid	—	37	ns
181	DSI Valid to DSCK Low (Setup)	5.2	—	ns
182	DSCK Low to DSI Invalid (Hold)	0	—	ns
183	DSCK High (See note 1)	2Tc	—	ns
184	DSCK Low (See note 1)	2Tc	—	ns
185	DSCK Cycle Time (See note 1)	4Tc	—	ns
186	CLKO High to OS0-OS1 Valid		14.5	ns
187	CLKO High to OS0-OS1 Invalid	—	—	ns
188	Last DSCK High to OS0-OS1 (See note 2) Last DSCK High to $\overline{ACK}$ Active (data) (See note 2) Last DSCK High to $\overline{ACK}$ Active (command) (See note 2)	10T+Td+14.5 10T+Td+13.5 21T+Td+13.5	— —	ns
189	DSO ($\overline{ACK}$) Asserted to OS0-OS1 Three-state	—	0	ns
190	DSO ($\overline{ACK}$) Asserted to First DSCK High	3Tc	—	ns
191	DSO ($\overline{ACK}$) Width Asserted: a. when entering debug mode b. when acknowledging command/data transfer	 3T-2 2Tc+0.5	 3T-5 2Tc+3	 ns ns
192	Last DSCK High of Read Register to First DSCK High of Next Command	6Tc	—	ns
193	DSCK High to DSO Invalid (See note 2)	Td+11.2	—	ns
194	$\overline{DR}$ asserted to DSO ($\overline{ACK}$) Asserted	11T+19.5	—	ns

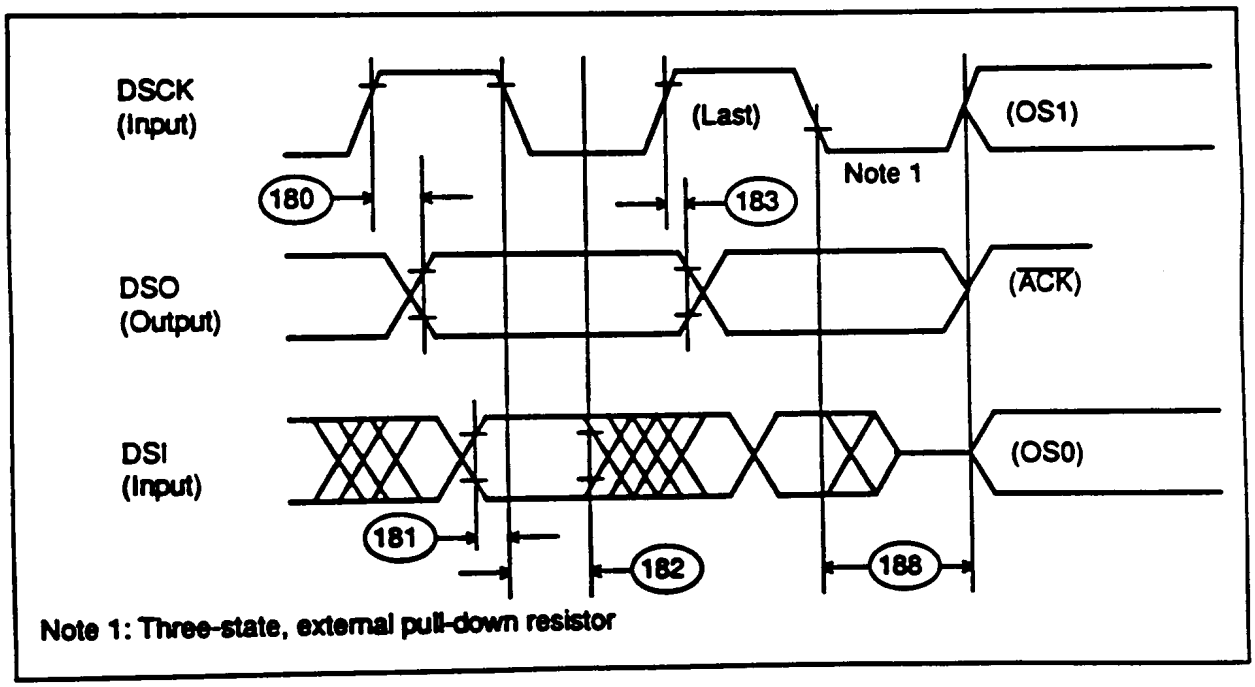
NOTES:
1. 45%-55% duty cycle
2. Td=DSCK High (183)



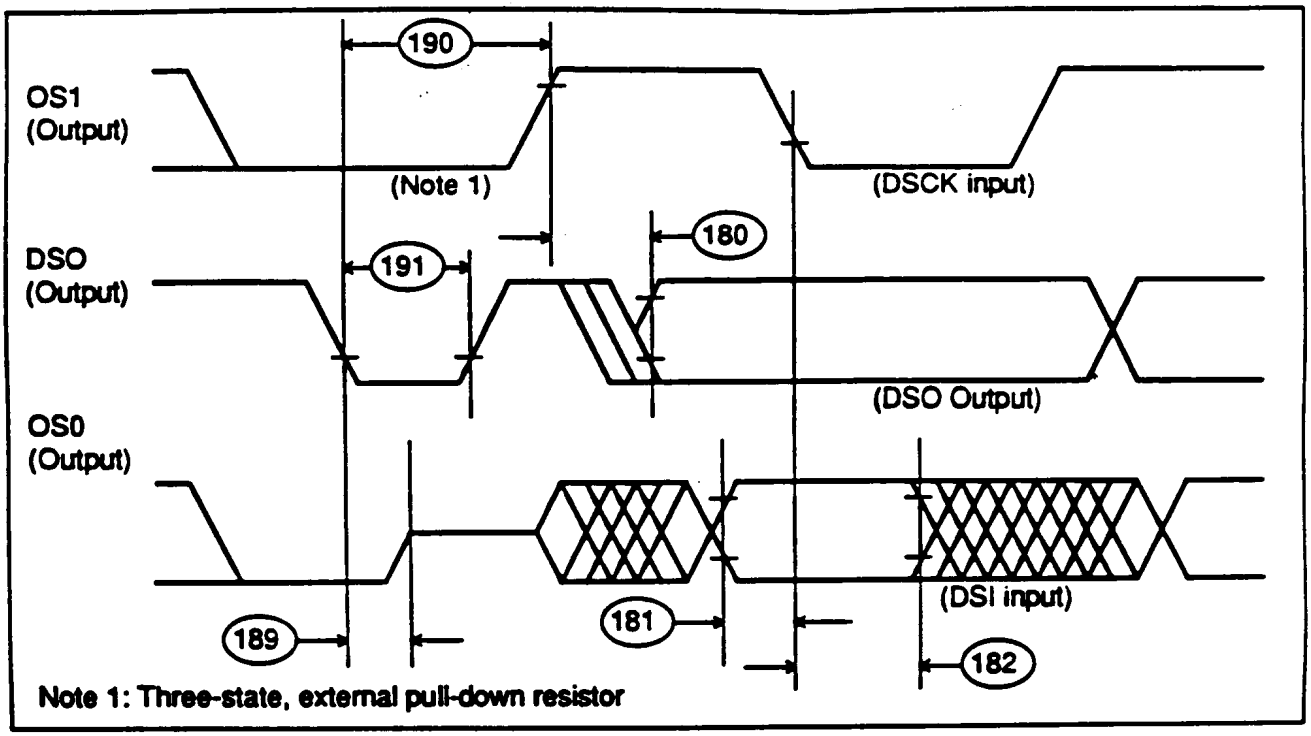
OnCE Figure 1. OnCE Serial Clock Timing



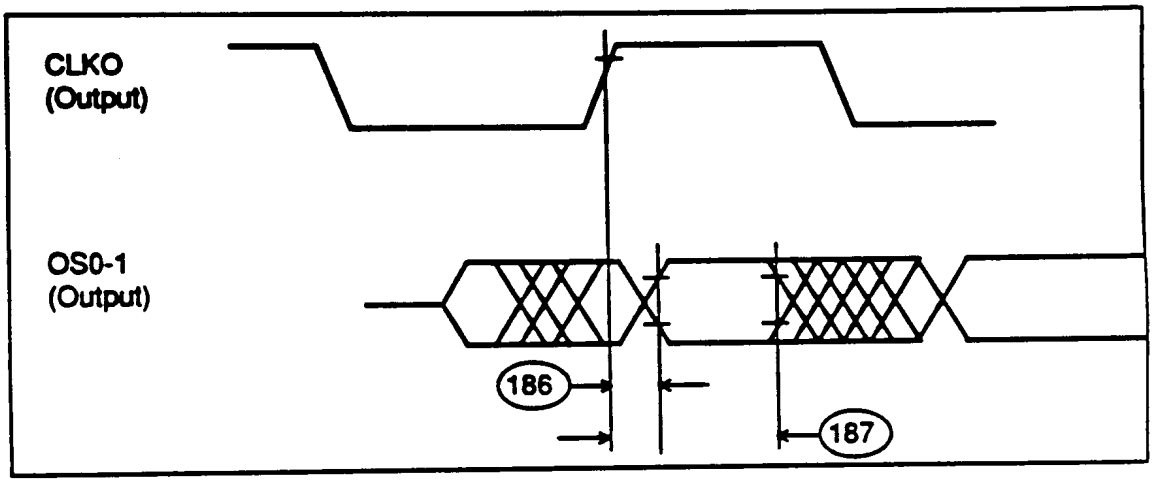
OnCE Figure 2. OnCE Acknowledge Timing



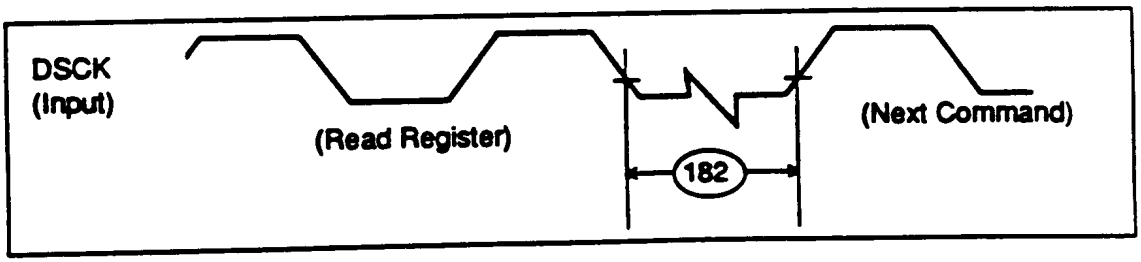
OnCE Figure 3. OnCE Data I/O To Status Timing



OnCE Figure 4. OnCE Data I/O To Status Timing



OnCE Figure 5. OnCE CLK To Status Timing



OnCE Figure 6. OnCE DSCK Next Command After Read Register Timing