

Z89314/318

DIGITAL TELEVISION CONTROLLER

FEATURES

- | Part Number | Z8 ROM (Kbyte) | Z8 RAM* (Kbyte) | Speed (MHz) |
|-------------|----------------|-----------------|-------------|
| Z89314 | 16 | 512 | 12 |
| Z89318 | 10 | 512 | 12 |
- *General-Purpose
- 40-Pin DIP Package
 - 4.5- to 5.0-Volt Operating Range
 - Z89C00 RISC Processor Core
 - 0°C to +70°C Temperature Range
 - Direct Closed Caption Decoding
 - TV Tuner Serial Interface
 - Customized Character Set
 - Character Control Mode
 - Directly Controlled Receiver Functions

GENERAL DESCRIPTION

The Z89314/318 are members of Zilog's family of Digital Television Controllers designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities.

The powerful Z89C00 RISC processor core allows users to control on-board peripheral functions and registers using the standard processor instruction set.

In closed caption mode, text can be decoded directly from the composite video signal and displayed on the screen with assistance from the processor's digital signal processing capabilities. The character representation in this mode allows for a simple attribute control through the insertion of control characters.

The character control mode provides access to the full set of attribute controls. The modification of attributes is allowed on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

Display attributes include underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency are made possible through a fully customized 512 character set, formatted in two 256 character banks.

Serial interfacing with the television tuner is provided through the tuner serial port. This version of the Z89300 series does not offer I²C capability

Additional hardware provides the capability to display two to three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Fringing circuitry can be activated to improve the visibility of text by surrounding the character lines with a one-pixel border.

Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

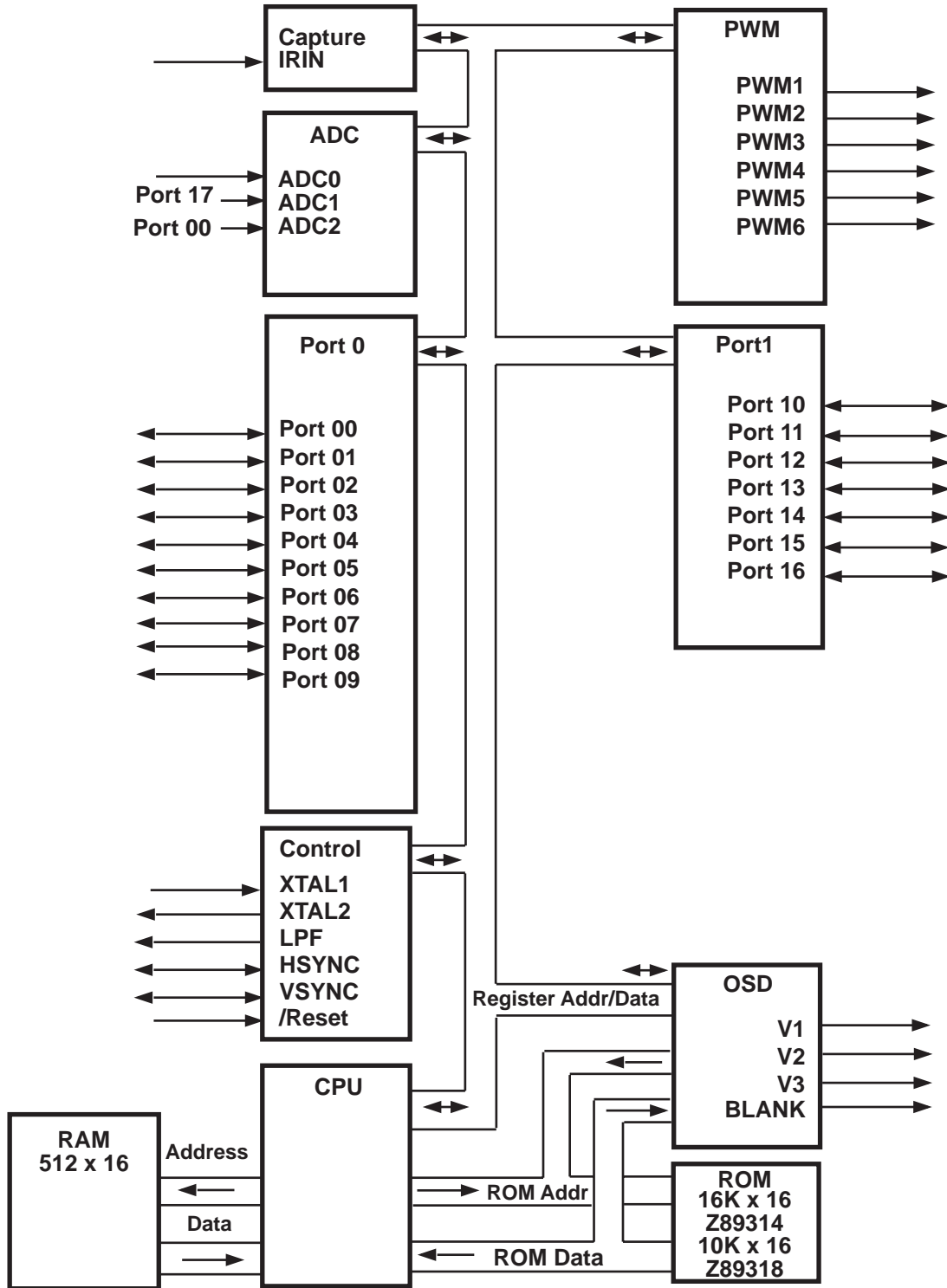
Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

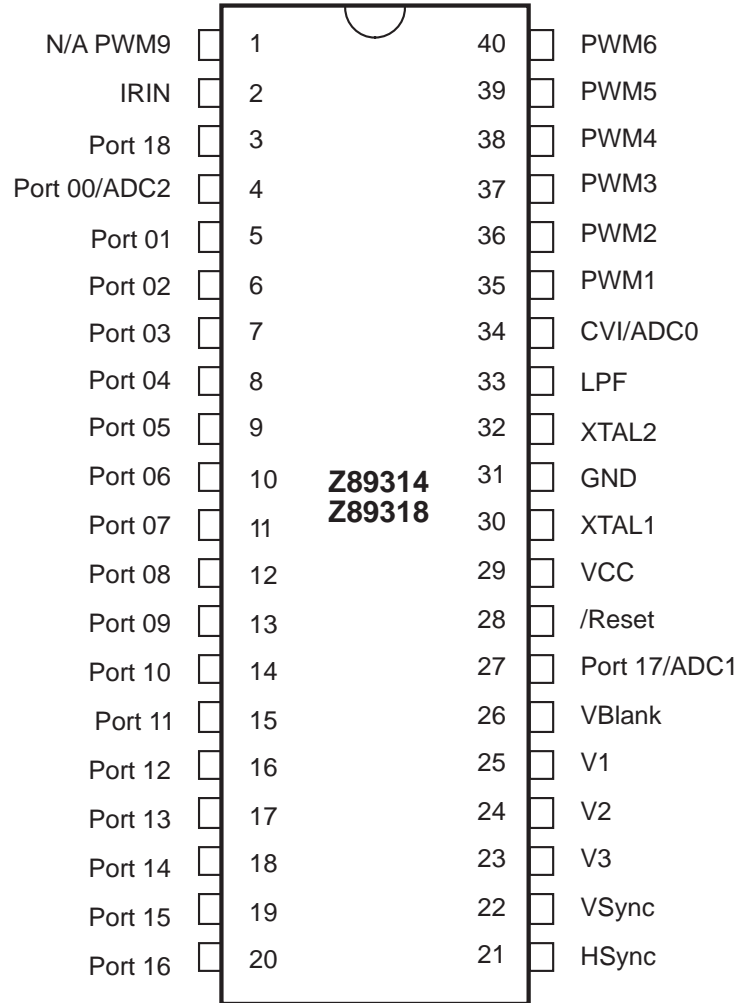
Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

PIN DESCRIPTION



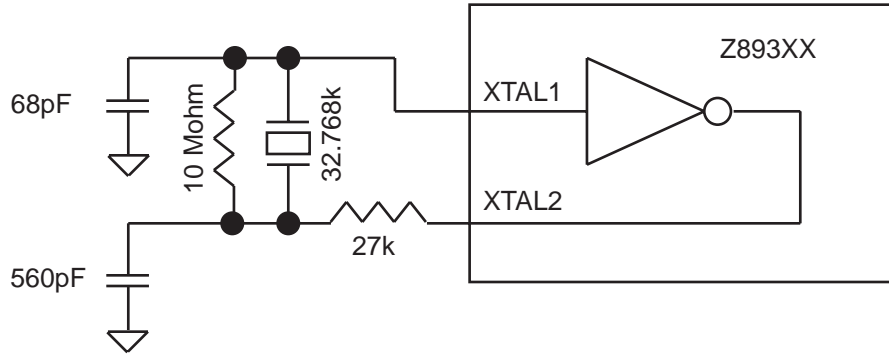
40-Pin DIP Configuration

PIN DESCRIPTION (Continued)
 Z89314/318

Pin Name	Function	Z89314 40-Pin	Configuration	
			Direction	Reset
V _{CC}	+5 V	29,-	PWR	-
GND	0 V	31,-	PWR	-
IRIN	Infrared Remote Capture Input	2	I	I
ADC[5:0]	4-Bit Analog to Digital Converter Input	-, -, -, 4, 27, 34	AI	I
PWM[8:1] ^a	8-Bit Pulse Width Modulator Output	-, -, 40, 39, 38 37, 36, 35	OD	O
Port0[F:0] ^b	Bit Programmable Input/Output Ports	-, -, -, -, -, -, 13, 12, 11	B	I
Port1[9:0] ^a	Bit Programmable Input/Output Ports	10, 9, 8, 7, 6, 5, 4 -, 3, 27, 20, 19, 18, 17, 16, 15, 14	B	I
XTAL1	Crystal Oscillator Input	30	AI	I
XTAL2	Crystal Oscillator Output	32	AO	O
LPF	Loop Filter	33	AB	O
HSYNC	H_Sync	21	B	I
VSYNC	V_Sync	22	B	I
/RESET	Device Reset	28	I	I
V[3:1]	OSD Video Output (Typically Drive B, G, and R Outputs)	23, 24, 25	O	O
Blank	OSD Blank Output	26	O	O
Half Blank	OSD Half Blank Output	N/A	O	
SCLK ^e	Internal Processor SCLK	20	O	

Notes:

- a) PWM [8,7] is not available on the 40-pin DIP version.
- b) Port0 [F:A] is not available on the 40-pin DIP version.
- c) Port19 is not available on the 40-pin DIP version.
- d) Half Blank output is a function shared with Port0F.
Half Blank output is not available on the 40-pin DIP version.
- e) Internal processor SCLK is shared with Port16.



32K Oscillator Recommended Circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Power Supply Voltage	0	7	V	
V_{ID}	Input Voltage	-0.3	$V_{CC} + 0.3$	V	Digital Inputs
V_{IA}	Input Voltage	-0.3	$V_{CC} + 0.3$	V	Analog Inputs (A/D0...A/D4)
V_O	Output Voltage	-0.3	$V_{CC} + 0.3$	V	All Push-Pull Digital Output
V_O	Output Voltage	-0.3	$V_{CC} + 8.0$	V	Open-Drain PWM Outputs (PWM1...PWM8)
I_{OH}	Output Current High		-10	mA	One Pin
I_{OH}	Output Current High		-100	mA	All Pins
I_{OL}	Output Current Low		20	mA	One Pin
I_{OL}	Output Current Low		200	mA	All Pins
T_A	Operating Temperature	0	70	°C	
T_A	Storage Temperature	-65	150	°C	

DC CHARACTERISTICS
 $T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = 4.5 \text{ V to } +5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units	Conditions
V_{IL}	Input Voltage Low	0	$0.2 V_{CC}$	0.4	V	
V_{IH}	Input Voltage High	$0.6 V_{CC}$	V_{CC}	3.6	V	
V_{PU}	Max. Pull-Up Voltage		12		V	PWM0...PWM8 Only
V_{OL}	Output Voltage Low		0.4	0.16	V	@ $I_{OL} = 1 \text{ mA}$
V_{OL}^3	Output Voltage High	$V_{CC} - 0.9$		4.75	V	@ $I_{OL} = 0.75 \text{ mA}$
V_{XL}	Input Voltage XTAL1 Low		$0.3 V_{CC}$	1.0	V	External Clock
V_{XH}	Input Voltage XTAL1 High	$V_{CC} - 2.0$		3.5	V	Generator Driven
V_{HY}^1	Schmitt Hysteresis	3.0	0.75	0.5	V	On XTAL1 Input Pin
I_{IR}	Reset Input Current		150	90	μA	$V_{RL} = 0 \text{ V}$
I_{IL}	Input Leakage	-3.0	3.0	0.01	μA	@ 0 V and V_{CC}
I_{CC}	Supply Current		100	60	mA	
I_{CC1E}^2	Supply Current of the OTP		700	300	μA	Sleep Mode @ 32 KHz
I_{CC1}^2	Supply Current		300	100	μA	Sleep Mode @ 32 KHz
I_{CC2}	Supply Current		40	5	μA	Sleep Mode

Notes:

1. Not in the EOS.
2. Z89314 is not an OTP.
3. Labeled incorrect.

AC CHARACTERISTICS

$T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units
T_{PC}	Input Clock Period	16	100	32	μS
T_{RC}, T_{FC}	Clock Input Rise and Fall			12	μS
T_{DPOR}	Power On Reset Delay	0.8		1.2	s

AC CHARACTERISTICS*

$T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; F_{OSC} = 32.768 \text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units
T_{WRES}	Power-On Reset Min. Width		5TPC		μS
T_{DH_S}	H_Sync Incoming Signal Width	5.5	12.5	11	μS
T_{DV_S}	V_Sync Incoming Signal Width	0.15	1.5	1.0	mS
T_{DE_S}	Time Delay Between Leading Edge of V_Sync and H_Sync in Even Field	-12	+12	0	μS
T_{DO_S}	Time Delay Between Leading Edge of H_Sync in Odd Field	20	44	32	μS
T_{WHV_S}	H_Sync/V_Sync Edge Width		2.0	0.5	μS

***Notes:**

The above AC Characteristics are ROM code/software dependent and are not measurable internally.

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