DATA SHEET

SAA7712H
Sound effects DSP

Preliminary specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

1.1 Hardware features

- Digital Signal Processor (DSP) core:
  - 18 bits data width, 12 bits coefficient width
  - Separate X, Y and P memories (both 384 bytes word XRAM and YRAM, 3 kbytes word PROM)
  - 1 kbytes delay line memory suited for Dolby Pro Logic Surround.
- Inputs:
  - 2 slave 18-bit digital stereo inputs: I^2S-bus and LSB-justified serial formats
  - 2 master 18-bit digital stereo inputs: I^2S-bus and LSB-justified serial formats.
- Outputs:
  - 4 DACs with 4-times oversampling and noise shaping, fed to 4 output pins and configurable from the DSP program, as left, right, front and surround channels of a Dolby Pro Logic Surround system
  - 2 master 18-bit digital stereo outputs: I^2S-bus and LSB-justified serial formats.
- 4-channel 5-band or 2-channel 10-band I^2C-bus controlled parametric equalizer
- I^2C-bus microcontroller interface for:
  - Access to full X and Y memory space
  - Control of hardware settings: selectors, programmable clock generations, etc.
- Controllable Phase-Locked Loop (PLL) to generate the high frequency DSP clock from common fundamental oscillator crystal
- 3.3 V process with 3.3 or 5 V digital periphery:
  - 3.3 or 5 V I^2S-bus and I^2C-bus microcontroller interfacing.
- Operating temperature range from 0 to 70 °C.

1.2 Software features

- **Dolby Pro Logic Surround/Dolby 3 stereo:** Trademark of Dolby Laboratories Licensing Corporation
- **Noise generation:** A pink noise generator is included for installation of the Dolby Pro Logic/Dolby 3 stereo mode
- **Hall/Matrix Surround:** When no Dolby Pro Logic Surround source material is available then this mode can be used to produce a signal in the surround channel
- **Incredible Surround (222-IS):** This algorithm expands the stereo width (stereo expander). This is intended to be used when the 2 speakers are placed close together (TV set and Midi set).
- **Robust Incredible Surround (222-RIS):** Same as incredible surround only an alternative algorithm
- **3D Surround (422) or Incredible Virtual Surround:** Dolby Pro Logic Surround reproduced by 2 speakers (L and R)
- **IS-3D Surround (422-IS):** Same as 3D Surround (422) only with extra stereo width expander on left and right
- **RIS-3D Surround (422-RIS):** Same as IS-3D Surround (422) with alternative algorithm
- **3D Surround (423) or Incredible Virtual Surround:** Dolby Pro Logic Surround reproduced by 3 speakers (L, C and R)
- **IS-3D Surround (423-IS):** Same as 3D Surround (423) only with extra stereo width expander on left and right
- **RIS-3D Surround (423-RIS):** Same as IS-3D Surround (423-IS) with alternative algorithm

- **Voice cancelling (karaoke):** Rejects voice out of source material, mainly intended to be used with karaoke. Several karaoke modes available in stereo mode and in Dolby Pro Logic mode, such as (auto) voice cancel, (auto) centre voice cancel, (auto) multi left and (auto) multi right.
- **Microphone mix modes (karaoke):** Mono microphone mixed to left, right and centre channel
- **Spectrum analysis:** 3-band spectrum analyser is provided
- **Dolby B:** Both a Dolby B encoder as well as a Dolby B decoder is implemented
- **2 Room solution:** In all modes not requiring more than 2 output channels (stereo and karaoke incredible surround) it is also possible to feed the source signal to the other 2 output channels (with same processed or not processed signal)
- **Dynamic Bass Enhancement (DBE):** Dynamic bass enhancement generates a sub-woofer channel, which is either a separate output or is added to the front channels
- **Volume processing:** Independent volume processing of all 4 output channels
- **AC-3/MPEG-2:** Inputs available intended to be used with an AC-3/MPEG-2 co-processor. In this mode the SAA7712H can be used as post-processor.
- **Output redirection:** Several output configurations are possible (normal 4 channel, special 4 + 2 channel, record 2 + 2 channel, 6 or 6 + 2 channel).

Depending on the sample frequency several combinations of the above mentioned features are possible.

2 APPLICATIONS

The SAA7712H can be used in TV sets with:

- Dolby Pro Logic Surround, incredible surround, 3D Surround and advanced acoustics processing
- Multi-channel sound decoding (AC-3 and MPEG-2) on a co-processor. The SAA7712H can be used for post-processing.

3 GENERAL DESCRIPTION

The SAA7712H provides for digital signal processing power in TV systems and home theatre systems.

A DSP core is equipped with digital inputs and outputs, a 5-band parametric equalizer accelerator, a digital co-processor interface and a delay line memory. This architecture accommodates on-chip standard sound processing, incredible surround, Dolby Pro Logic Surround and other surround sound processing algorithms. The architecture also supports co-processing, e.g. to add to the processing power of the internal DSP core or for multi-channel surround decoding.

All settings and parameters are controlled by an I^2C-bus interface. The available interfaces support a high application flexibility.

The DSP core communicates over 32 dedicated registers. The selected digital input is master for the data rate of the DSP core. This input can be selected among 2 slave I^2S-bus inputs. The 4 outputs from the core are passed through 4 DACs and then routed to 4 output pins.

Two master I^2S-bus outputs and two master I^2S-bus inputs can serve as an I^2S-bus co-processor interface.

Eight of the remaining registers are used for communication with the hardware equalizer, and eight for communication with the delay line memory.

All I^2S-bus inputs and outputs support the Philips I^2S-bus format as well as 16, 18 and 20-bit LSB-justified formats.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD3V}	supply voltage 3.3 V analog and digital	with respect to V_{SS}	3	3.3	3.6	V
V_{DD5V}	supply voltage 5 V periphery	with respect to V_{SS}	3	3.3 or 5	5.5	V
I_{DDD3V}	DC supply current of the 3.3 V digital core part	at f_{DSP18}; maximum activity of the DSP	–	–	80	mA
I_{DDD5V}	DC supply current of the 5 V digital periphery part	at f_{DSP18}; maximum activity of the DSP; V_{DD5} = 5 V	–	–	5	mA
		at f_{DSP18}; maximum activity of the DSP; V_{DD5} = 3.3 V	–	–	5	mA
I_{DDA}	DC supply current of the analog part	at zero input and output signal	–	–	10	mA
P_{tot}	total power dissipation	at f_{DSP18}; maximum activity of the DSP	–	–	0.4	W
(THD + N)/S	DAC total harmonic distortion-plus-noise to output signal	R_L > 5 kΩ; f = 1 kHz; A-weighted	–	–75	–60	dBA
DR_{DAC}	DAC dynamic range	f = 1 kHz; –60 dB; A-weighted	90	96	–	dBA
DS_{DAC}	DAC digital silence	f = 20 Hz to 17 kHz; A-weighted	–	–107	–102	dBA
f_{xtal}	crystal frequency		10.000	–	19.456	MHz
f_{DSP16}	DSP clock frequency	f_{xtal} = 16.384 MHz	–	–	32.256	MHz
f_{DSP18}	DSP clock frequency	f_{xtal} = 18.432 MHz	–	–	32.544	MHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7712H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT318-1

6 BLOCK DIAGRAM

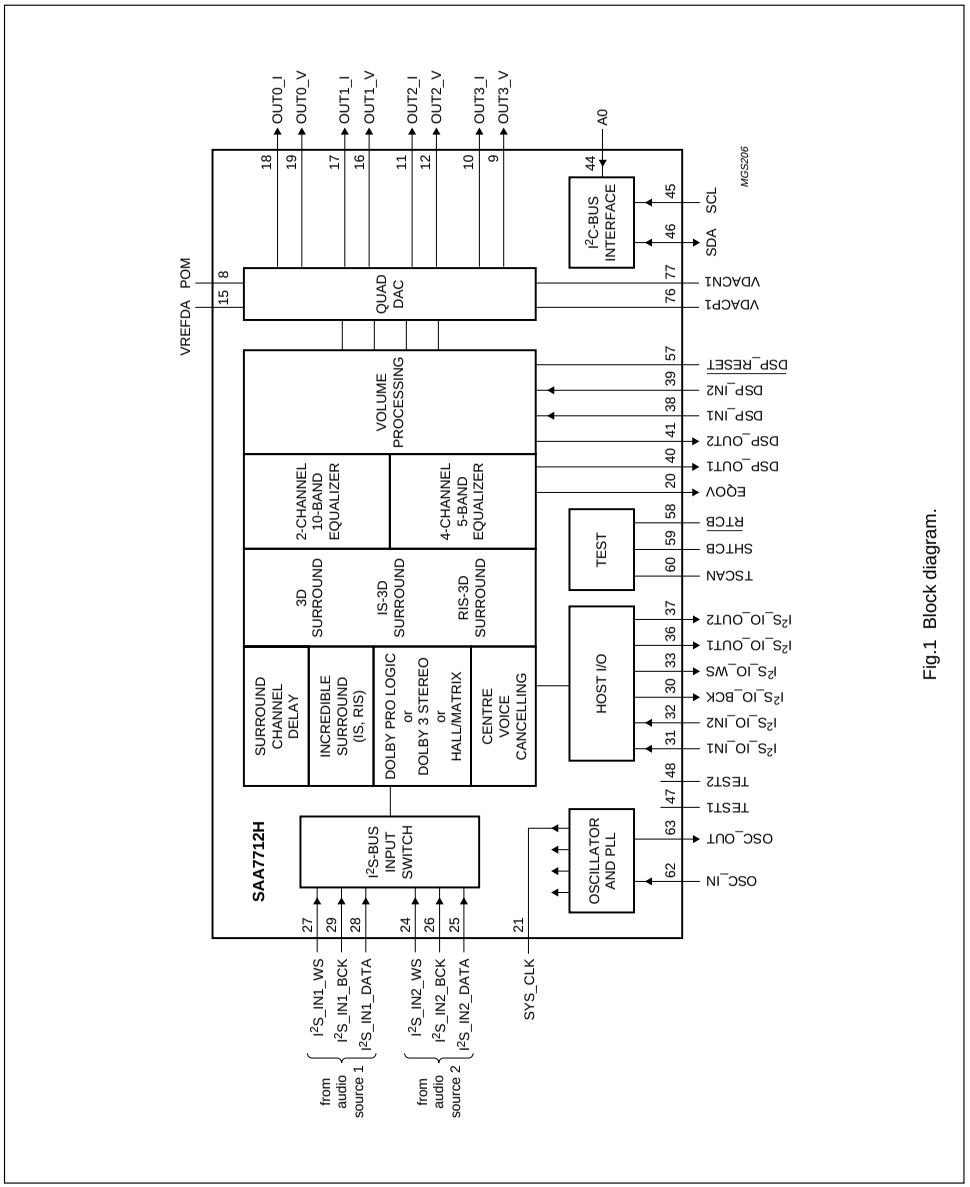


Fig.1 Block diagram.

7 PINNING INFORMATION

SYMBOL	PIN	DESCRIPTION	PIN TYPE
n.c.	1	not connected	
n.c.	2	not connected	
n.c.	3	not connected	
n.c.	4	not connected	
n.c.	5	not connected	
n.c.	6	not connected	
n.c.	7	not connected	
POM	8	power-on mute; timing determined by external capacitor	AP2D
OUT3_V	9	analog voltage output 3	AP2D
OUT3_I	10	analog current output 3	AP2D
OUT2_I	11	analog current output 2	AP2D
OUT2_V	12	analog voltage output 2	AP2D
V_{SSA2}	13	analog ground supply 2	APVSS
V_{DDA2}	14	analog supply voltage 2 (3 V)	APVDD
VREFDA	15	voltage reference of the analog part	AP2D
OUT1_V	16	analog voltage output 1	AP2D
OUT1_I	17	analog current output 1	AP2D
OUT0_I	18	analog current output 0	AP2D
OUT0_V	19	analog voltage output 0	AP2D
EQOV	20	equalizer overflow line output	B4CR
SYS_CLK	21	test pin output	BT4CR
V_{DDD5V1}	22	digital supply voltage 1; peripheral cells only (3 or 5 V)	VDD5
V_{SSD5V1}	23	digital ground supply 1; peripheral cells only (3 or 5 V)	VSS5
I^2S_IN2_WS	24	I^2S-bus or LSB-justified format word select input from a digital audio source 2	IBUFD
I^2S_IN2_DATA	25	I^2S-bus or LSB-justified format left-right data input from a digital audio source 2	IBUFD
I^2S_IN2_BCK	26	I^2S-bus clock or LSB-justified format input from a digital audio source 2	IBUFD
I^2S_IN1_WS	27	I^2S-bus or LSB-justified format word select input from a digital audio source 1	IBUFD
I^2S_IN1_DATA	28	I^2S-bus or LSB-justified format left-right data input from a digital audio source 1	IBUFD
I^2S_IN1_BCK	29	I^2S-bus clock or LSB-justified format input from a digital audio source 1	IBUFD
I^2S_IO_BCK	30	I^2S-bus bit clock output for interface with DSP co-processor chip	BT4CR
I^2S_IO_IN1	31	I^2S-bus input data channel 1 from DSP co-processor chip	IBUFD
I^2S_IO_IN2	32	I^2S-bus input data channel 2 from DSP co-processor chip	IBUFD
I^2S_IO_WS	33	I^2S-bus word select output for interface with DSP co-processor chip	BT4CR
V_{DDD5V2}	34	digital supply voltage 2; peripheral cells only (3 or 5 V)	VDD5
V_{SSD5V2}	35	digital ground supply 2; peripheral cells only (3 or 5 V)	VSS5
I^2S_IO_OUT1	36	I^2S-bus output data channel 1 to DSP co-processor chip	BT4CR
I^2S_IO_OUT2	37	I^2S-bus output data channel 2 to DSP co-processor chip	BT4CR
DSP_IN1	38	digital input 1 of the DSP core (F0 of the status register)	IBUFD

SYMBOL	PIN	DESCRIPTION	PIN TYPE
DSP_IN2	39	digital input 2 of the DSP-core (F1 of the status register)	IBUFD
DSP_OUT1	40	digital output 1 of the DSP-core (F2 of the status register)	B4CR
DSP_OUT2	41	digital output 2 of the DSP-core (F3 of the status register)	B4CR
V_{DDD5V3}	42	digital supply voltage 3; peripheral cells only (3 or 5 V)	VDD5
V_{SSD5V3}	43	digital ground supply 3; peripheral cells only (3 or 5 V)	VSS5
A0	44	I^2C-bus slave subaddress selection input	IBUFD
SCL	45	I^2C-bus serial clock input	SCHMITCD
SDA	46	I^2C-bus serial data input/output	BD4SCI4
TEST1	47	test pin 1	BD4CR
TEST2	48	test pin 2	BT4CR
V_{SSD3V1}	49	digital ground supply 1 of 3 V core only	VSS3S
V_{SSD3V2}	50	digital ground supply 2 of 3 V core only	VSS3S
V_{SSD3V3}	51	digital ground supply 3 of 3 V core only	VSS3S
V_{DDD3V1}	52	digital supply voltage 1 of 3 V core only	VDD3
V_{DDD3V2}	53	digital supply voltage 2 of 3 V core only	VDD3
V_{SSD3V4}	54	digital ground supply 4 of 3 V core only	VSS3S
V_{SSD3V5}	55	digital ground supply 5 of 3 V core only	VSS3S
V_{SSD3V6}	56	digital ground supply 6 of 3 V core only	VSS3S
$\overline{\text{DSP\_RESET}}$	57	reset (active LOW)	IBUFU
$\overline{\text{RTCB}}$	58	asynchronous reset test control block (active LOW)	IBUFD
SHTCB	59	shift clock test control block	IBUFD
TSCAN	60	scan control	IBUFD
V_{SS_OSC}	61	ground supply crystal oscillator circuit	VSS3S
OSC_IN	62	crystal oscillator input; crystal oscillator sense for gain control or forced input in slave mode	OSC
OSC_OUT	63	crystal oscillator output; drive output to 11.2896 MHz crystal	OSC
V_{DD_OSC}	64	3 V supply voltage crystal oscillator circuit	VDD3
n.c.	65	not connected	
n.c.	66	not connected	
n.c.	67	not connected	
n.c.	68	not connected	
n.c.	69	not connected	
n.c.	70	not connected	
n.c.	71	not connected	
n.c.	72	not connected	
n.c.	73	not connected	
n.c.	74	not connected	
n.c.	75	not connected	
VDACP1	76	not used	
VDACN1	77	not used	

SYMBOL	PIN	DESCRIPTION	PIN TYPE
n.c.	78	not connected	
n.c.	79	not connected	
n.c.	80	not connected	

Table 1 Pin types

PIN NAME	PIN DESCRIPTION
B4CR	4 mA slew rate controlled digital output
BD4CR	4 mA slew rate controlled digital I/O
BD4CRD	4 mA slew rate controlled digital I/O with pull-down resistor
BT4CR	4 mA slew rate controlled 3-state digital output
IBUF	digital input
IBUFU	digital input with pull-up resistor
IBUFD	digital input with pull-down resistor
BD4SCI4	I^2C-bus input/output with open-drain NMOS 4 mA output
SCHMITCD	Schmitt trigger input
AP2D	analog input/output
OSC	analog input/output
VDD5	5 V V_{DD} internal
VDD3	3 V V_{DD} internal
VSS3S	3 or 5 V V_{SS} internal substrate
VSS5	5 V V_{SS} external
APVDD	analog V_{DD}
APVSS	analog V_{SS}

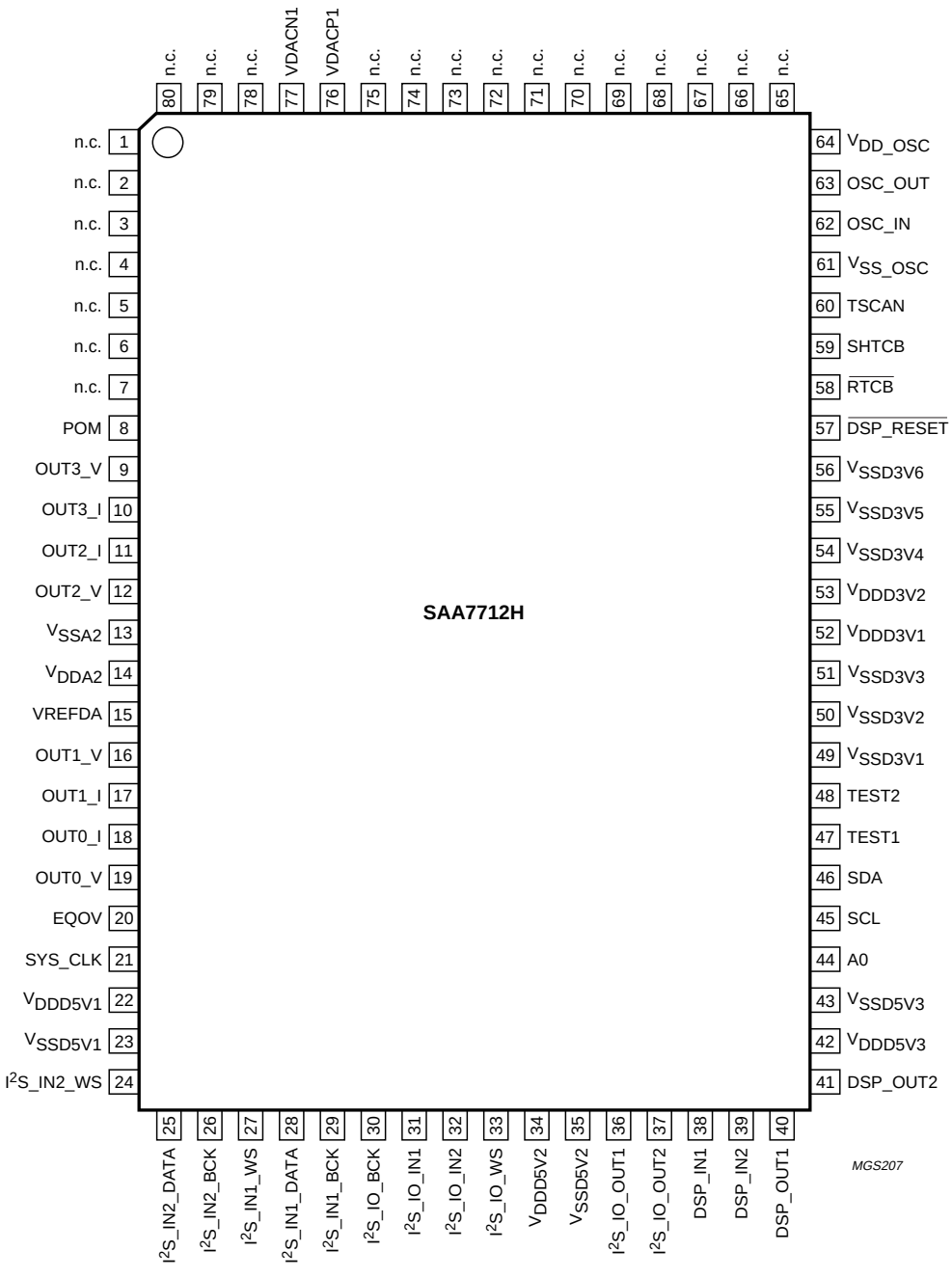


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 Analog outputs

8.1.1 Analog output circuit

Depending on the configuration of the equalizer sections, the SAA7712H has 2 or 4 analog outputs which are supplied by the same power supply. Each of these outputs has a voltage and a current pin (see Fig.3). The signals are available on 2 outputs (OUT0 and OUT1), or 4 outputs (OUT0, OUT1, OUT2 and OUT3).

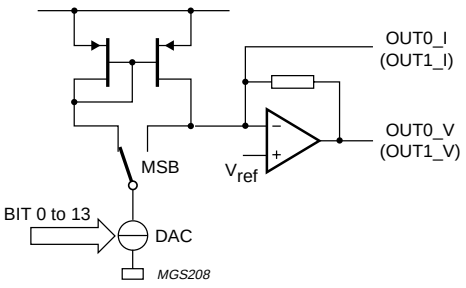


Fig.3 Analog output circuit.

8.1.2 DAC frequency

The sample rate (f_s) of the selected source is the frame rate of the DSP. The word clock for the upsample filter and the clock for the DACs, at $4f_s$, are derived internally from the word select of the selected audio source.

8.1.3 DACs

Each of the four low noise high dynamic range DACs consists of a signed-magnitude DAC with current output, followed by a buffer operational amplifier.

8.1.4 Upsample filter

To reduce spectral components above the audio band, a fixed 4 times oversampling and interpolating digital filter is used. The filters give an out-of-audio-band attenuation of at least 29 dB. The filter is followed by a first-order noise shaper to expand the dynamic range to more than 105 dB.

The band around multiples of the sample frequency of the DAC ($4f_s$) is not affected by the digital filter. A capacitor must be added in parallel with the DAC output amplifier to attenuate this out-of-band noise further to an acceptable level.

In Fig.4 the overall frequency spectrum at the DAC audio output without external capacitor or low-pass filter for the audio sampling frequencies of 38 kHz is shown. In Fig.5 the detailed spectrum around f_s is shown for an f_s of 38, 44.1 and 48 kHz. The pass band bandwidth (–3 dB) is $\frac{1}{2}f_s$.

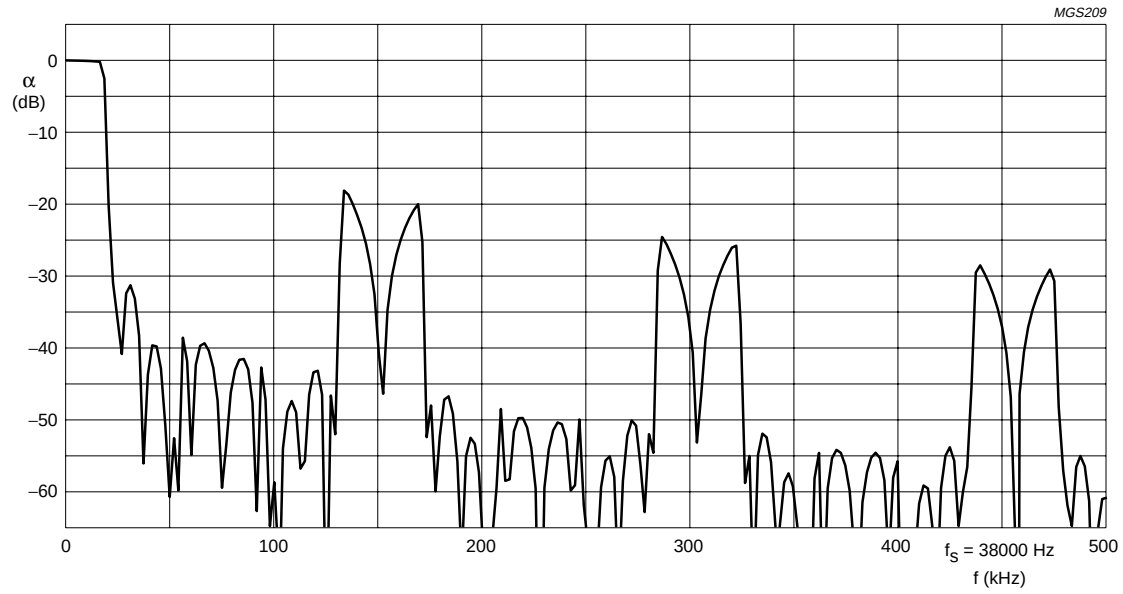


Fig.4 Overall frequency spectrum audio output.

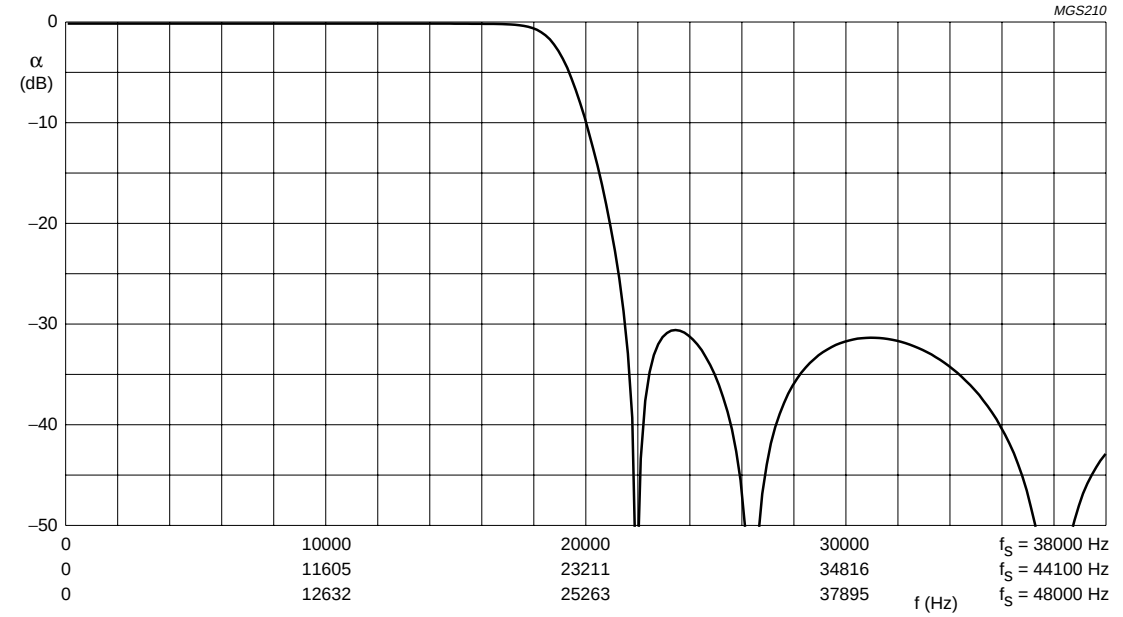


Fig.5 Detailed frequency spectrum audio output.

8.1.5 PERFORMANCE

The signed-magnitude noise-shaped DAC has a dynamic range in excess of 100 dB. The signal-to-noise ratio of the audio output at full-scale is determined by the word length of the converter. The noise at low outputs is fully determined by the noise performance of the DAC. Since it is a signed-magnitude type, the noise at digital silence is also low. As a disadvantage, the total THD is higher than conventional DACs. The typical total harmonic distortion-plus-noise to signal ratio as a function of the output level is shown in Fig.6.

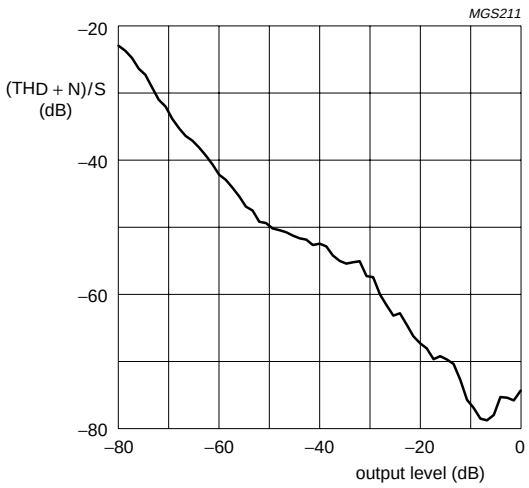


Fig.6 Typical (THD + N)/S curve as a function of the output level.

8.1.6 POWER-ON MUTE (POM)

To avoid any uncontrolled noise at the audio outputs after power-on of the IC, the reference current source of the DAC is switched off. The capacitor on pin POM determines the time after which this current has a soft switch-on. So at power-on the current audio signal outputs are always muted. The loading of the external capacitor is done in two stages via two different current sources. The loading starts at a current level that is 9 times lower than the current loading after the voltage on pin POM has passed the 1 V level. This results in an almost dB linear behaviour.

8.1.7 POWER-OFF PLOP SUPPRESSION

Power should still be provided to the analog part of the DAC, while the digital part is switching off. As a result, the output voltage will decrease gradually allowing the power amplifier some extra time to switch-off without audible plops. If a 5 V power supply is present, the supply voltage of the analog part of the DAC can be fed from the 5 V power supply via a 1.8 V zener diode. A capacitor, connected to the 3.3 V power supply, provides power to the analog part when the 5 V power supply is switching off fast.

8.1.8 PIN VREFDA

With two internal resistors half the supply voltage (V_{DDA2}) is obtained and coupled to an internal buffer. This reference voltage is used as DC voltage for the output operational amplifiers and as reference for the DAC. In order to obtain the lowest noise and to have the best ripple rejection, a filter capacitor has to be added between this pin and ground.

8.1.9 INTERNAL DAC CURRENT REFERENCE

As a reference for the internal DAC current and for the DAC current source output, a current is drawn from the level on pin VREFDA to pin V_{SSA2} (ground) via an internal resistor. The absolute value of this resistor also determines the absolute current of the DAC. This means that the absolute value of the current is not that fixed due to the spread of the current reference resistor value. This, however, does not influence the absolute output voltages because these voltages are also derived from a conversion of the DAC current to the actual output voltage via internal resistors.

8.1.10 SUPPLY OF THE ANALOG OUTPUTS

All the analog circuitry of the DACs and the operational amplifiers are fed by 2 supply pins, V_{DDA2} and V_{SSA2}. Pin V_{DDA2} must have sufficient decoupling to prevent THD degradation and to ensure a good power supply rejection ratio.

The digital part of the DAC is fully supplied from the chip core supply.

8.2 I²S-bus inputs and outputs

8.2.1 DIGITAL DATA STREAM FORMATS

For communication with external digital sources a serial 3-line bus is used. This I²S-bus has one line for data, one line for clock and one line for the word select.

See Fig.7 for the general waveform formats of the four possible formats.

The serial digital inputs (and outputs) of the SAA7712H are capable of handling multiple formats: Philips I²S-bus and LSB-justified formats of 16, 18 and 20 bits word sizes.

In Philips I²S-bus format, the number of bit clock (BCK) pulses may vary in the application. When the transmitter word length is smaller than the receiver word length, the receiver will fill in zeroes at the LSB side. When the transmitter word length exceeds the receiver word length, the LSBs are skipped. For correct operation of the DACs, there should be a minimum of 16 bit clocks per word select.

In the LSB-justified formats, the transmitter and receiver must be set to the same format. Be aware that a format switch between 20, 18 and 16 bits LSB-justified formats is done by changing the relative timing of the word select edges. The data bits remain unchanged. In the 20 bits format, the 2 LSBs are zeroes. In the 16 bits format, the 2 data bits following the word select edge are not zero, but undefined. In fact, these are the LSBs of the 18-bit word.

The timing specification for the waveforms of the serial digital inputs and outputs are given in Fig.17.

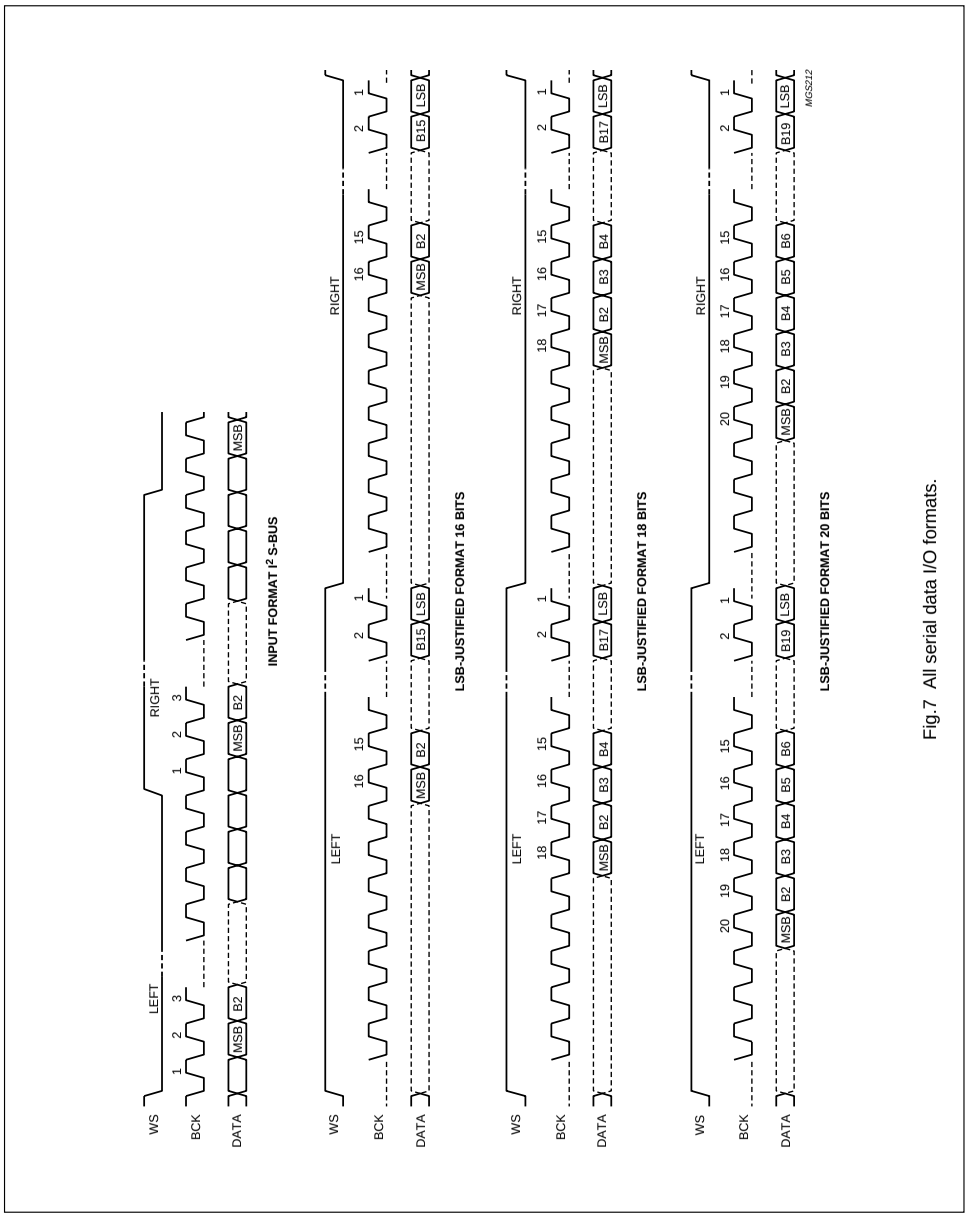


Fig.7 All serial data I/O formats.

8.2.2 SLAVE I²S-BUS INPUTS

The SAA7712H has two slave I²S-bus inputs, I²S_IN1 and I²S_IN2 with respective data lines I²S_IN1_DATA and I²S_IN2_DATA, word select lines I²S_IN1_WS and I²S_IN2_WS and bit clock lines I²S_IN1_BCK and I²S_IN2_BCK. The external source is master and supplies the bit clock and word select. The I²C-bus bits audio_format(2 to 0) allow for selection of the desired I²S-bus format (see Table 13). The bits, needed for selecting a certain format, are explained in Table 2.

The input circuitry is limited in handling the number of BCK pulses per WS period. If the word rate of the selected digital input source is f_s, the bit clock must be a continuous clock in the range of $16f_s \leq f_{bit(CLK)} \leq 256f_s$. The minimum limit of the audio sample frequency is determined by $^1/_{18}f_{SCL}$. The maximum limit of the audio sample frequency is determined by DSP_clock/481 Hz.

Table 2 I²C-bus audio_format mode bits (0FF9H, see Table 13)

AUDIO_FORMAT			OUTPUT
BIT 9	BIT 8	BIT 7	
0	0	0	internal format (for test purposes only)
–	0	1	LSB-justified, 16 bits
–	1	0	LSB-justified, 18 bits
–	1	1	LSB-justified, 20 bits
1	0	0	standard I²S-bus (default)

The selection of the DSP input among the decimated analog input and the I²S-bus inputs I²S_IN1 and I²S_IN2 is controlled with I²C-bus bit audio_source (see Table 13). The meaning of this bit can be found in Table 3.

Table 3 I²C-bus audio_source mode bit (0FF9H, see Table 13)

AUDIO_SOURCE	OUTPUT
Bit 5	
0	I²S_IN1 (default)
1	I²S_IN2

8.2.3 MASTER I²S-BUS INPUTS AND OUTPUTS

For the co-processor I/O interface, the SAA7712H acts as a master. The SAA7712H supplies both the bit clock and word select. The I²C-bus bits host_io_format(1 and 0) allow for selection of the desired I²S-bus format (see Table 13).

The bits needed for selecting a certain format are given in Table 4.

All I²S-bus output lines, I²S_IO_WS, I²S_IO_BCK, I²S_IO_OUT1 and I²S_IO_OUT2, can be 3-stated with I²C-bus bit en_host_io (see Table 13).

The word select and bit clock of the co-processor I/O interface are derived from the word select and bit clock of the audio source selected according to Table 3.
The incoming bit clock can be divided by 1, 2, 4 or 8 depending on the needs of an external connected co-processor. These selections can be done with I²C-bus bits cloop_mode(2 to 0) (see Table 13). The meaning of these bits is shown in Table 5.

Table 4 I²C-bus host_io_format bits (0FF9H, see Table 13)

HOST_IO_FORMAT		OUTPUT
BIT 11	BIT 10	
0	0	standard I²S-bus (default)
0	1	LSB-justified format, 16 bits
1	0	LSB-justified format, 18 bits
1	1	LSB-justified format, 20 bits

Table 5 I²C-bus cloop_mode bits (0FF9H, see Table 13)

CLOOP_MODE			OUTPUT
BIT 15	BIT 14	BIT 13	
0	–	–	bypass WS (default)
1	–	–	WS 50% duty factor
–	0	0	bypass BCLK (default)
–	0	1	divide BCLK by 2
–	1	0	divide BCLK by 4
–	1	1	divide BCLK by 8

8.3 Equalizer accelerator

8.3.1 Introduction

The equalizer accelerator is a hardware accelerator to the DSP core. Both its inputs and outputs are stored in registers of the DSP core.

The equalizer cannot be used and cannot be programmed if no word select and bit clock signal are present on a selected digital source input; see audio_source bit in Table 3 (I²S_IN1 or I²S_IN2). The minimum required DSP_clock is $481f_s$.

The equalizer accelerator contains one second-order filter data path that is 20 times multiplexed. With this circuit, a 2-channel equalizer of 10 second-order sections per channel or a 4-channel equalizer of 5 second-order sections per channel can be realised. The centre frequency, gain and Q-factor of all 20 second-order sections can be set independently from each other. Every section is followed by a selectable attenuation of 0 or 6 dB. Per section, 4 bytes of the I²C-bus register are needed to store the settings. The equalizer settings can be updated during normal operation. An application program supports the programming of the equalizer.

If the gain setting causes the audio signal to exceed the maximum level in one of the filter sections, the signal will be clipped and the equalizer overflow output (pin EQOV) will be set HIGH until the end of the next audio sample period.

8.3.2 Configuration of equalizer sections

The equalizer accelerator can make a 2-channel equalizer of 10 second-order sections per channel or a 4-channel equalizer of 5 second-order sections per channel.
The sections of one channel can be chained one after the other. Depending on the I²C-bus control bit two_four (see Table 11), the 20 filter sections are combined for the appropriate configuration, as illustrated in Fig.8.

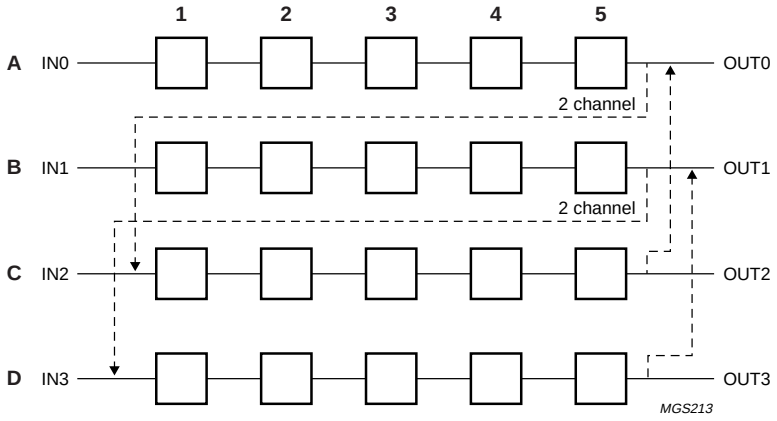


Fig.8 Configurations of the equalizer sections.

8.3.3 Overflow detection

The equalizer has an overflow flag. This flag is fed to output pin EQOV. If an overflow is detected in one of the filter sections, the signal is clipped to the maximum allowed level. The overflow flag is immediately set. It remains at a HIGH-level during the remaining part of the current audio sample period and for the whole next sample period. If no overflow is detected during this next sample period, the overflow flag goes to a LOW-level at the beginning of the sample period after that. Otherwise, the overflow flag remains at a HIGH-level for at least one other audio sample period.

8.4 Clock circuit and oscillator

8.4.1 General description

The chip has a crystal clock oscillator. It can use a crystal at either f_{xtal} = 16.384 MHz = 512 × 32 kHz or f_{xtal} = 18.432 MHz = 576 × 32 kHz in fundamental mode. The block diagram of this Pierce oscillator is shown in Fig.9. The active element needed to compensate for the loss resistance of the crystal is the block Gm. This block is placed between the external pins OSC_IN and OSC_OUT.

The gain of the oscillator is internally controlled by the AGC block. A sine wave with a peak-to-peak voltage close to the oscillator power supply voltage is generated. The AGC block prevents clipping of the sine wave and therefore the higher harmonics are as low as possible. At the same time, the voltage of the sine wave is as high as possible so reducing the jitter going from sine wave to clock signal. The sinusoidal output is converted into a CMOS compatible clock by the comparator.

The second mode of operation shown in Fig.10, is the slave mode which is driven by a master clock directly. The signal to pin OSC_IN can be driven to the power supply voltages V_{DD_OSC} and V_{SS_OSC}.

8.4.2 Supply of the crystal oscillator

The power supply connections of the oscillator are separate from the other supply lines. This is to minimize the feedback from the ground bounce of the chip to the oscillator circuit. Pin V_{SS_OSC} is used as the ground supply and pin V_{DD_OSC} as the positive supply.

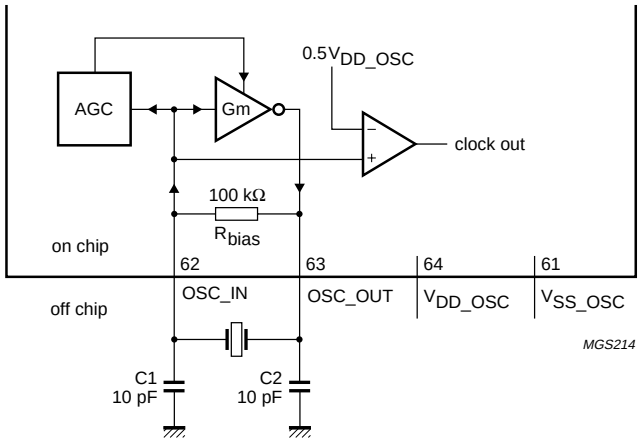


Fig.9 Block diagram of the crystal oscillator circuit.

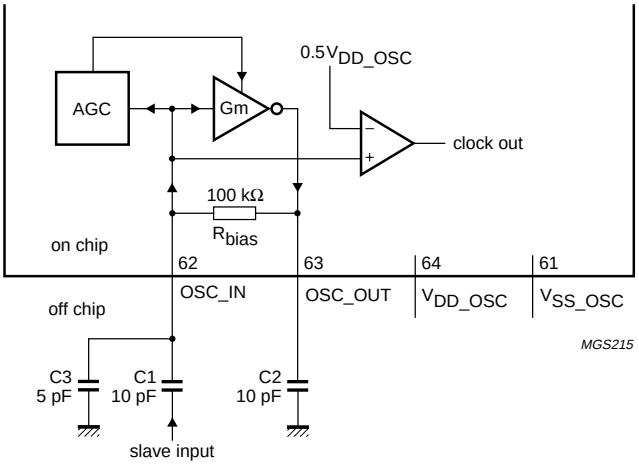


Fig.10 Block diagram of the oscillator in slave mode.

8.5 Programmable phase-locked loop circuit

The clock of the DSP is generated with a programmable PLL.

To select the required DSP clock see Table 6. The N factor (ranging from 93 to 181) can be selected with I²C-bus bits PLL_div(14 to 11), see Table 10. Depending on the crystal and the required DSP clock the I²C-bus bits pll_fs_sel and bits dsp_turbo must be set. The maximum limit of the audio sample frequency is determined by DSP_clock/481 Hz.

Table 6 I²C-bus bits PLL_div and dividing factors N of the programmable DSP clock

PLL_DIV(14 to 11)	N	DSP CLOCK FREQUENCY (MHz)	
		TDA9875[1]	MSP3410D[2]
0000	93 (default)	23.808[3]	26.784
0001	99	25.344[3]	28.512
0010	106	27.136	30.528
0011	113	28.928	32.544
0100	121	30.976	34.848[3]
0101	126	32.256	36.288[3]
0110	132	33.792[3]	38.016[3]
0111	137	35.072[3]	39.456[3]
1000	143	36.608[3]	41.184[3]
1001	148	37.888[3]	42.624[3]
1010	154	39.424[3]	44.352[3]
1011	159	40.704[3]	45.792[3]
1100	165	42.240[3]	47.520[3]
1101	170	43.520[3]	48.960[3]
1110	176	45.056[3]	50.688[3]
1111	181	46.336[3]	52.128[3]

Notes

1. f_{xtal} = 16.384 MHz; pll_fs_sel = 1 and dsp_turbo = 1, see Table 11.
2. f_{xtal} = 18.432 MHz; pll_fs_sel = 1 and dsp_turbo = 1, see Table 11.
3. Usable frequency.

8.6 I²C-bus control

8.6.1 Introduction

A general description of the I²C-bus format can be obtained from Philips Semiconductors, International Marketing and Sales Communications (IMSC).

For the external control of the SAA7712H a fast I²C-bus is implemented. This is a 400 kHz bus which is downward compatible with the standard 100 kHz bus.

There are different types of control instructions:

- Instructions to control the DSP program, program the coefficient RAM and read the values of parameters
- Instructions to control the equalizer, program the equalizer coefficient RAM to be able to change the centre frequency, gain and Q-factor of the equalizer sections
- Instructions to control the source selection and programmable parts, e.g. PLL clock speed.

The detailed description of the I²C-bus and commands is given in the following sections. The description of the different bits in the memory map is given in Section 9.6. The equalizer cannot be used and cannot be programmed if there is no word select and bit clock signal present on a selected digital source input; see audio_source bit in Table 3 (I²S_IN1 and I²S_IN2). The minimum limit of the audio sample frequency is determined by $^{1}/_{18}f_{SCL}$.

8.6.2 Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to V_{DD} via a pull-up resistor when connected to the output stages of a microcontroller. For a 400 kHz I²C-bus the recommendation from Philips Semiconductors must be followed (e.g. up to loads of 200 pF on the bus a pull-up resistor can be used, between 200 to 400 pF a current source or switched resistor must be used). Data transfer can only be initiated when the bus is not busy.

8.6.3 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.11). The maximum clock frequency is 400 kHz. To be able to run on this high frequency all the inputs and outputs connected to this bus must be designed for this high speed I²C-bus according to the Philips specification.

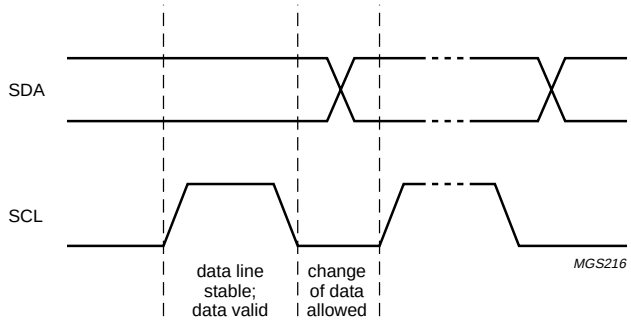


Fig.11 Bit transfer on the I²C-bus.

8.6.4 START AND STOP CONDITIONS

Both data and clock lines will remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as a START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a STOP condition (P) (see Fig.12).

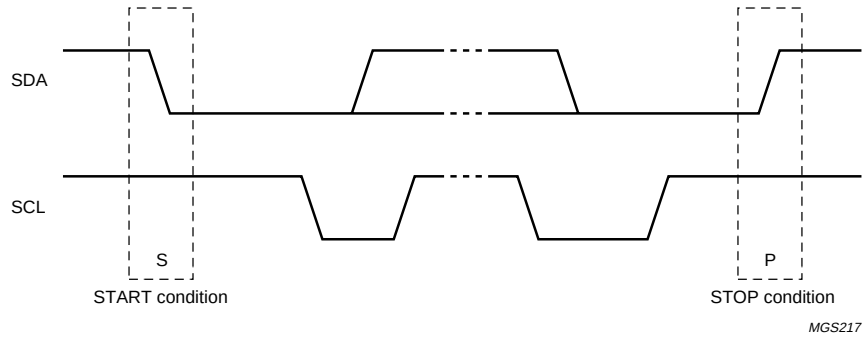


Fig.12 START and STOP conditions.

8.6.5 DATA TRANSFER

A device generating a message is a ‘transmitter’ and a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

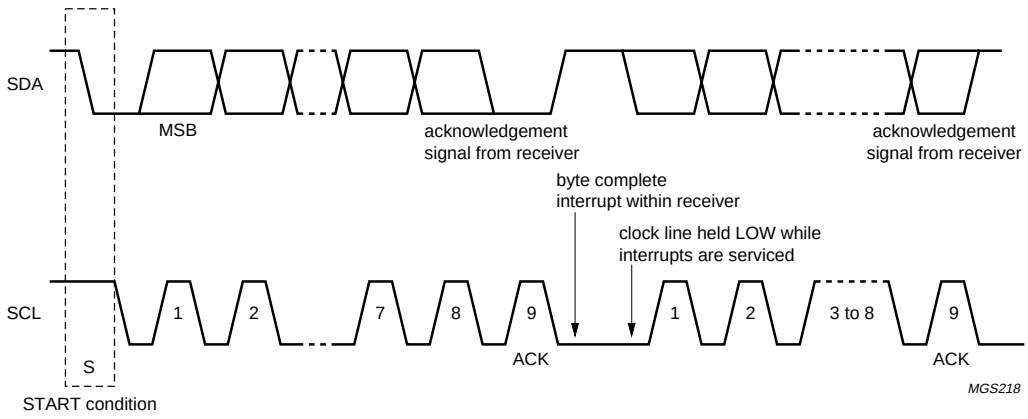


Fig.13 Data transfer on the I^2C-bus.

8.6.6 Acknowledge

The number of data bits transferred between the START and STOP conditions from the transmitter to the receiver is not limited. Each byte of eight bits is followed by one acknowledge bit (see Fig.13). The acknowledge bit is a HIGH-level left on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line (left HIGH by the transmitter) during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition (see Fig.14).

8.6.7 State of the I²C-bus interface during and after Power-on reset

During reset (see Section 8.8), the internal SDA line is kept HIGH and pin SDA is therefore high-impedance. The SDA line remains HIGH until a master pulls it down to initiate communication.

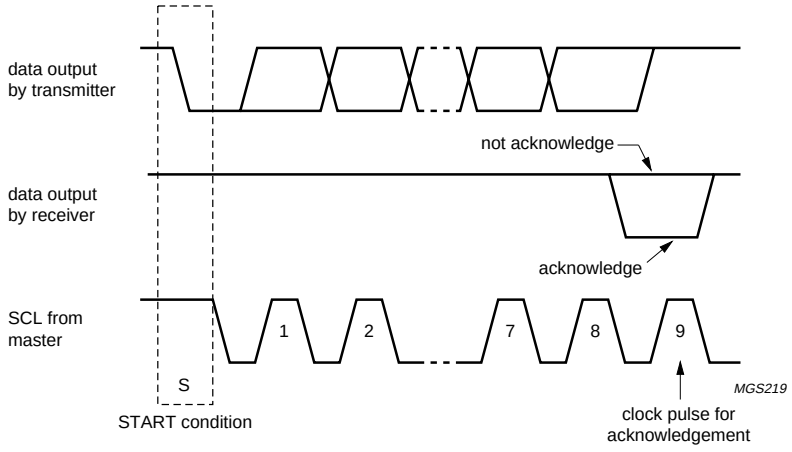


Fig.14 Acknowledge on the I²C-bus.

8.7 External control pins

For external control two input pins are implemented. The status of these pins can be changed by applying a logic level. The status of these pins is recorded in the internal status register. The function of each input pin is determined by the DSP software.

Pin DSP_IN1:

- Logic 0 or left open-circuit means volume coefficients updates are possible (default)
- Logic 1 means no updates of volume coefficients are possible.

Pin DSP_IN2:

- If the 3-band spectrum analyser is used:
  - Logic 1 will reset the band registers of the analyser
  - Logic 0 or left open-circuit means no reset of the band registers will be done (default).
- If the 3-band spectrum analyser is not used:
  - The state of pin DSP_IN2 can be read via an I^2C-bus command.

To control external devices two output pins are implemented. The status of these pins is controlled by the DSP program. The functions of these pins are determined by the DSP software.

Pin DSP_OUT1:

- To drive pin DSP_OUT1 via an I^2C-bus command.

Pin DSP_OUT2:

- To drive pin DSP_OUT2 via an I^2C-bus command.

8.8 Reset pin

The reset signal on pin $\overline{\text{DSP\_RESET}}$ is active LOW and has an internal pull-up resistor. Between this pin and ground a capacitor should be connected to allow a proper switch-on of the supply voltage. The capacitor value is such that the chip is in the reset state as long as the power supply is not stabilized.

A more or less fixed relationship between the $\overline{\text{DSP\_RESET}}$ time constant and the POM time constant is obligatory. The voltage on pin POM determines the current flowing in the DACs. For 0 V on pin POM, the DAC currents are zero and so also the DACs output voltages. When a 3 V supply voltage (V_{DDA2}) is supplied to pin POM, the DAC currents are at their nominal (maximum) value.

Long before the DAC outputs get their nominal output voltages, the DSP must be in normal operating mode to reset the output register. Therefore, the time constant of $\overline{\text{DSP\_RESET}}$ must be shorter than the time constant of POM. For advised capacitors see the application diagram.

The reset has the following function:

- All I^2C-bus registers are reset to their default values
- The DSP algorithm is re-started
- The external control output pins are reset (see Section 8.7)
- Pin SDA is high-impedance.

When the level on the reset pin is HIGH, the DSP algorithm starts to run.

In addition to the reset pin, there is also a software reset; bit PC_reset (bit 15, 0FFDH, see Table 11). This reset has the following function:

- The DSP algorithm is re-started
- The external control output pins are reset (see Section 8.7).

8.9 Power supply connection and EMC

The digital part of the chip has in total 5 positive supply line connections and 8 ground connections. To minimise radiation the chip should be put on a double layer PCB with a large ground plane on one side. The ground supply lines should have a short connection to this ground plane. A coil and capacitor network in the positive supply line can be used as high frequency filter.

8.10 Test mode connections

Pins TSCAN, $\overline{\text{RTCB}}$ and SHTCB are used to put the chip in test mode and to test the internal connections. Each pin has an internal pull-down resistor to ground. In the application these pins can be left open-circuit or connected to ground.

9 I²C-BUS FORMAT

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the START procedure.

9.2 Slave address (pin A0)

The SAA7712H acts as a slave receiver or a slave transmitter. Therefore, the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The slave address is shown in Table 7.

Table 7 Slave address

MSB							**LSB**
0	0	1	1	1	1	A0	R/$\overline{\text{W}}$

The subaddress bit A0 corresponds to the hardware address pin A0 which allows the device to have two addresses. This allows the control of two SAA7712Hs via the same I²C-bus.

9.3 Write cycles

The I²C-bus configuration for a write cycle is shown in Fig.15. The write cycle is used to write the bytes to control the PLL for the DSP clock generation, the format of the I²S-bus and some other settings. More details can be found in the I²C-bus memory map (see Table 8).

The data length is 2 or 3 bytes, depending on the accessed memory. The slave receiver detects the address and adjusts the number of bytes accordingly. For XRAM, the data word length is 18 bits and 3 bytes are sent over the I²C-bus. The upper 6 bits (i.e. bit 7 to bit 2) of the first byte DATA H are don't care. For YRAM, the data word length is 12 bits and 2 bytes are sent over the I²C-bus. The left nibble (i.e. bit 7 to bit 4) of the first byte DATA H is don't care.

9.4 Read cycles

The I²C-bus configuration for a read cycle is shown in Fig.16. The read cycle is used to read the data values from XRAM or YRAM. The master starts with a START condition (S), the SAA7712H address '0011110' and a logic 0 (write) for the read/write bit. This is followed by an acknowledge of the SAA7712H. The master then writes the memory high address and memory low address where the reading of the memory content of the SAA7712H must start. The SAA7712H acknowledges these addresses both.

The master than generates a repeated START and again the SAA7712H address '0011110' but this time followed by a logic 1 (read) of the read/write bit. From this moment on, the SAA7712H will send the memory content in groups of 2 (YRAM) or 3 (XRAM) bytes to the I²C-bus, each time acknowledged by the master. The master stops this cycle by generating a negative acknowledge, then the SAA7712H frees the I²C-bus and the master can generate a STOP condition (P).

S = START condition.
ACK = acknowledge from DSP (SDA LOW).
ADDR H and ADDR L = address DSP register.
DATA H, DATA M and DATA L = data of XRAM or registers.
DATA H and DATA M = data of YRAM.
P = STOP condition.

Fig.15 Master transmitter writes to the DSP registers.

S = START condition.
ACK = acknowledge from DSP (SDA LOW).
ADDR H and ADDR L = address DSP register.
DATA H, DATA M and DATA L = data of XRAM or registers.
DATA H and DATA M = data of YRAM.
P = STOP condition.

Fig.16 Master transmitter reads from the DSP registers.

9.5 I²C-bus memory map summary

The I²C-bus memory map contains all defined I²C-bus bits. The map is split into two different sections: hardware memory registers and the RAM definitions. The preliminary memory map is given in Table 8.

Table 8 I²C-bus memory map

SUBADDRESSES	FUNCTION	SIZE
0FF9H to 0FFFH	various settings (see Table 9**)**	4 × 16 bits
0F80H to 0FA7H	equalizer	40 × 16 bits
0800H to 097FH	YRAM	384 × 12 bits
0000H to 017FH	XRAM	384 × 18 bits

Table 9 I²C-bus memory map: overview of various settings

REGISTER NAME	SUBADDRESS
I²C_DCS_CTR	0FFFH (see Table 10)
I²C_ADDA	0FFDH (see Table 11)
I²C_SEL	0FFAH (see Table 12)
I²C_HOST	0FF9H (see Table 13)

9.6 I²C-bus memory map details

Table 10 I²C_DCS_CTR register (0FFFH)

NAME	SIZE (BITS)	DESCRIPTION	DEFAULT	BIT POSITION
–	10	reserved		9 to 0
loopo_on_off	1	pin SYS_CLK output enable: on (logic 1) or off (logic 0)	off	10
PLL_div	4	PLL clock division factor for DSP_clock (see Table 6)	93	14 to 11
–	1	reserved		15

Table 11 I²C_ADDA register (0FFDH)

NAME	SIZE (BITS)	DESCRIPTION	DEFAULT	BIT POSITION
–	10	reserved		9 to 0
pll_fs_sel	1	divide oscillator by 2 (logic 1)	division	10
dsp_turbo	1	double DSP_clock (logic 1)	doubling	11
two_four	1	2-channel 10-band (logic 1) or 4-channel 5-band (logic 0) equalizer configuration	4-channel 5-band	12
–	2	reserved		14 and 13
pc_reset	1	re-start DSP algorithm (logic 1) or DSP running (logic 0)	DSP running	15

Table 12 I²C_SEL register (0FFAH)

NAME	SIZE (BITS)	DESCRIPTION	DEFAULT	BIT POSITION
–	8	reserved		7 to 0
bypass_pll	1	bypass PLL used for DSP_clock (logic 1) or use PLL for DSP_clock (logic 0)	use PLL	8
–	4	reserved		12 to 9
inv_host_ws	1	inverting (logic 1) or non-inverting (logic 0) word select	non-inverting	13
–	2	reserved		15 and 14

Table 13 I²C_HOST register (0FF9H)

NAME	SIZE (BITS)	DESCRIPTION	DEFAULT	BIT POSITION
–	5	reserved		4 to 0
audio_source	1	input source is I²S_IN1 or I²S_IN2 (see Table 3)	I²S_IN1	5
–	1	reserved		6
audio_format	3	format of selected input source (see Table 2)	standard I²S-bus	9 to 7
host_io_format	2	host input/output data format (see Table 4)	standard I²S-bus	11 and 10
en_host_io	1	enable (logic 1) or disable (logic 0) co-processor I²S-bus	disable	12
cloop_mode	3	cloop mode (see Table 5)	bypass WS	15 to 13

10 LIMITING VALUES

In accordance with the Absolute Maximum Ratings system (IEC 134).

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{DD3V}	supply voltage 3.3 V analog and digital		–0.5	+5	V
V_{DD5V}	supply voltage 5 V periphery	only valid for the voltages in connection with the 5 V I/Os	–0.5	+6.5	V
ΔV_{DD}	voltage difference between two V_{DDx} pins		–	550	mV
$\lvert I_{IK} \rvert$	input clamping diode current	$V_i < -0.5$ V or $V_i > V_{DD} + 0.5$ V	–	10	mA
$\lvert I_{O(sink/source)} \rvert$	output sink or source current, output type 4 mA	-0.5 V $< V_o < V_{DD} + 0.5$ V	–	20	mA
$\lvert I_{DD}, I_{SS} \rvert$	V_{DD} or V_{SS} current per supply pin		–	750	mA
T_{amb}	ambient temperature		0	70	°C
T_{stg}	storage temperature		–65	+150	°C
V_{es}	electrostatic handling voltage for all pins	note 1	–3000	+3000	V
		note 2	–300	+300	V
$I_{lu(prot)}$	latch-up protection	CIC specification/test method	100	–	mA
P/out	power dissipation per output		–	100	mW
P_{tot}	total power dissipation		–	400	mW

Notes

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Machine model: equivalent to discharging a 200 pF capacitor through a 2.5 μH inductance and a 0 Ω series resistor.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	45	K/W

Note

1. Printed-circuit board mounting.

12 DC CHARACTERISTICS

Digital I/O at T_{amb} = 0 to 70 °C; V_{DD5V} = 4.5 to 5.5 V; V_{DD3V} = 3 to 3.6 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD3V}	supply voltage 3.3 V analog and digital	all V_{DD} pins of the type VDD3 and APVVD referenced to V_{SS}	3	3.3	3.6	V
V_{DD5V}	supply voltage 5 V periphery	all V_{DD} pins of the type VDD5 referenced to V_{SS}	4.5	5	5.5	V
			3.0	3.3	3.6	V
I_{DDD3V}	supply current of the 3.3 V digital core part	at f_{DSP18}; maximum activity of the DSP	–	33	80	mA
I_{DDD5V}	supply current of the 5 V digital periphery part	at f_{DSP18}; maximum activity of the DSP	–	2	5	mA
I_{DAC}	supply current of the DACs	at zero input and output signal	–	4	7	mA
I_{DD_OSC}	supply current of the crystal oscillator	at f_{DSP18}; functional mode	–	3.5	3	mA
P_{tot}	total power dissipation	at f_{DSP18}; maximum activity of the DSP	–	135	400	mW
Logic						
V_{IH}	HIGH-level input voltage of all digital inputs and I/Os on pins 24 to 29, 38, 39, 44 to 47, 57 to 60		$0.7V_{DDD5V}$	–	–	V
V_{IL}	LOW-level input voltage of all digital inputs and I/Os on pins 24 to 29, 38, 39, 44 to 47, 57 to 60		–	–	$0.3V_{DDD5V}$	V
V_{hys}	hysteresis voltage on pin 45 (SCL)		1	1.3	–	V
V_{OH}	HIGH-level output voltage of digital outputs on pins 20, 21, 30, 33, 36, 37, 40, 41, 47, 48	I_O = –4 mA	V_{DDD5V} – 0.4	–	–	V
V_{OL}	LOW-level output voltage of digital outputs on pins 20, 21, 30, 33, 36, 37, 40, 41, 47, 48	V_{DDD5V} = 4.5 V; I_O = 4 mA	–	–	0.4	V
		V_{DDD5V} = 3.0 V; I_O = 4 mA	–	–	0.4	V
$V_{OL(I2C)}$	LOW-level output voltage of digital I^2C-bus data output on pin 46 (SDA)	I_O = 4 mA	–	–	0.4	V
$\|I_O\|$	output leakage current 3-state outputs on pins 21, 30, 33, 36, 37, 46 to 48	V_O = 0 or V_{DD}	–	–	5	µA
R_{pu}	internal pull-up resistance to V_{DDD} on pin 57 ($\overline{\text{DSP\_RESET}}$)		23	50	80	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{pd}	internal pull-down resistance to V_{SSD} on pins 24 to 29, 38, 39, 44, 58 to 60		23	50	80	kΩ
$t_{i(r)}$, $t_{i(f)}$	input rise and fall times	V_{DDD5V} = 5.5 V	–	6	200	ns
		V_{DDD5V} = 3.6 V	–	6	200	ns
t_{LH5}	output rise time on pins 20, 21, 30, 33, 36, 37, 40, 41, 47, 48	V_{DDD5V} = 5.5 V; V_{DDD3V} = 3.6 V; T_j = –40 °C; C_L = 60 pF	5	–	–	ns
		V_{DDD5V} = 4.5 V; V_{DDD3V} = 3 V; T_j = 125 °C; C_L = 60 pF	–	–	25	ns
t_{LH3}	output rise time on pins 20, 21, 30, 33, 36, 37, 40, 41, 47, 48	V_{DDD5V} = 3.6 V; V_{DDD3V} = 3.6 V; T_j = –40 °C; C_L = 60 pF	7.5	–	–	ns
		V_{DDD5V} = 3.0 V; V_{DDD3V} = 3 V; T_j = 125 °C; C_L = 60 pF	–	–	30	ns
$t_{LH(I2C5)}$	output rise time on pin 46 (SDA)	C_L and R_{pu} are application specific	–	–	–	ns
$t_{LH(I2C3)}$	output rise time on pin 46 (SDA)	C_L and R_{pu} are application specific	–	–	–	ns
t_{HL5}	output fall time on pins 20, 21, 30, 33, 36, 37, 40, 41, 47, 48	V_{DDD5V} = 5.5 V; V_{DDD3V} = 3.6 V; T_j = –40 °C; C_L = 60 pF	5	–	–	ns
		V_{DDD5V} = 4.5 V; V_{DDD3V} = 3 V; T_j = 125 °C; C_L = 60 pF	–	–	25	ns
t_{HL3}	output fall time on pins 20, 21, 30, 33, 36, 37, 40, 41, 47, 48	V_{DDD5V} = 3.6 V; V_{DDD3V} = 3.6 V; T_j = –40 °C; C_L = 60 pF	7.5	–	–	ns
		V_{DDD5V} = 3.0 V; V_{DDD3V} = 3 V; T_j = 125 °C; C_L = 60 pF	–	–	30	ns
$t_{HL(I2C5)}$	output fall time on pin 46 (SDA)	V_{DDD5V} = 5.5 V; V_{DDD3V} = 3.6 V; T_j = –40 °C; C_L = 200 pF	30	–	–	ns
		V_{DDD5V} = 4.5 V; V_{DDD3V} = 3 V; T_j = 125 °C; C_L = 200 pF	–	–	300	ns
$t_{HL(I2C3)}$	output fall time on pin 46 (SDA)	V_{DDD5V} = 3.6 V; V_{DDD3V} = 3.6 V; T_j = –40 °C; C_L = 200 pF	40	–	–	ns
		V_{DDD5V} = 3.0 V; V_{DDD3V} = 3 V; T_j = 125 °C; C_L = 200 pF	–	–	400	ns

13 ANALOG OUTPUTS CHARACTERISTICS

T_{amb} = 25 °C; V_{DDA2} = 3.3 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{VREFDA}	voltage on pin VREFDA	with respect to $V_{DDA2} - V_{SSA2}$	47	50	53	%
Z_{VREFDA}	impedance on pin VREFDA	with respect to V_{DDA2}	–	37	–	kΩ
		with respect to V_{SSA2}	–	37	–	kΩ
$V_{o(rms)}$	AC output voltage of operational amplifiers (RMS value)	maximum I^2S-bus signal; R_L > 5 kΩ	0.62	0.7	0.82	V
$V_{O(AV)}$	average DC output voltage of operational amplifiers	R_L > 5 kΩ	1.5	1.65	1.8	V
$I_{pu(POML)}$	low pull-up current to V_{DDA2} on pin POM	voltage on pin POM < 0.6 V	3.3	–	5	µA
$I_{pu(POMH)}$	high pull-up current to V_{DDA2} on pin POM	voltage on pin POM > 0.8 V	50	–	75	µA
$PSRR_{DAC}$	power supply ripple rejection DACs (input via I^2S-bus)	f_{ripple} = 1 kHz; V_{ripple} = 100 mV (peak value); C_{VREFDA} = 22 µF	45	60	–	dB
$\lvert\Delta I_{o(max)}\rvert$	maximum deviation in output level (plus or minus) of the 4 DAC current outputs	with respect to the average of the 4 outputs; full-scale output	–	–	0.38	dB
α_{ct}	crosstalk between all outputs in the audio band	one output digital silence, other three maximum volume	–	–	–69	dB
$I_{o(sc)}$	output short-circuit current	output short-circuited to ground	–	–	20	mA
RES_{DAC}	DAC resolution			18		bits
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f = 1 kHz; $V_{o(ref)}$ = 0.72 V (RMS); A-weighted	–	–75	–60	dBA
DR_{DAC}	dynamic range of DAC	$V_{o(ref)}$ = 0.72 V (RMS); f = 1 kHz; –60 dB; A-weighted	90	96	–	dBA
DS_{DAC}	digital silence of DAC	f = 20 Hz – 17 kHz; $V_{o(ref)}$ = 0.72 V (RMS); A-weighted	–	–107	–102	dBA
$V_{n(o)(rms)}$	digital silence noise level at output (RMS value)	A-weighted	–	3	8	µV
d	intermodulation distortion/comparator	f = 60 Hz and 7 kHz, ratio 4 : 1	–	–70	–55	dB
$f_{s(max)}$	maximum sample frequency		48	–	–	kHz
B_{DAC}	bandwidth DAC	at –3 dB	–	$\frac{1}{2}f_s$	–	kHz
$C_{L(DAC)}$	load capacitance on DAC outputs		–	–	2.5	nF
$R_{L(DAC)}$	load resistance on DAC voltage outputs	DC decoupled	5	–	–	kΩ

14 OSCILLATOR CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{xtal}	crystal frequency		10.000	–	19.456	MHz
$\Delta f_{xtal(adj)}$	crystal frequency variation with adjustment	T_{amb} = 25 °C	–30	–	+30	ppm
$\Delta f_{xtal(T)}$	crystal frequency variation with temperature		–30	–	+30	ppm
α_f	spurious frequency attenuation		20	–	–	dB
$V_{xtal(M)}$	voltage across the crystal (absolute peak value)		1.6	2.6	3.6	V
$g_{m(start)}$	transconductance at start-up		10.5	19	32	mS
$g_{m(oper)}$	transconductance when operating		3.6	–	38	mS
C_L	capacitive load of clock output		–	15	–	pF
$N_{cy(start)}$	number of cycles during start-up	depends on quality of the external crystal	–	1000	–	cycles
I_{xtal}	supply current	at start-up	–	7	15	mA
		at oscillation	–	0.6	2	mA
		in slave mode	–	0.65	0.9	mA
P_{xtal}	drive level	at oscillation	–	0.4	0.5	mW
$V_{i(clk)}$	external clock input voltage	in slave mode	3	3.3	3.6	V
R_{xtal}	allowed loss resistance of the crystal	C_p = 5 pF[1]; C1 = 10 pF; C2 = 10 pF; see Fig.9	–	20	100	Ω
R_o	output resistance	at start-up; f_{xtal} = 18.432 MHz; V_{DD_OSC} = 3.3 V	750	1300	2800	Ω

Note

1. C_p is the parasitic parallel capacitance of the crystal.

15 I²S-BUS TIMING CHARACTERISTICS

Timing of the serial digital data inputs and outputs (see Fig.17).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{cy}	bit clock cycle time	70	–	ns
$t_{su(D)}$	data set-up time (host)	32	–	ns
	data set-up time (I²S-bus)	10	–	ns
$t_{h(D)}$	data hold time (host)	5	–	ns
	data hold time (I²S-bus)	10	–	ns
$t_{su(WS)}$	word select set-up time (I²S-bus)	10	–	ns
$t_{h(WS)}$	word select hold time (I²S-bus)	10	–	ns
$t_{d(D)}$	data delay time (host)	–	20	ns
$t_{d(WS)}$	word select delay time (host)	–	15	ns

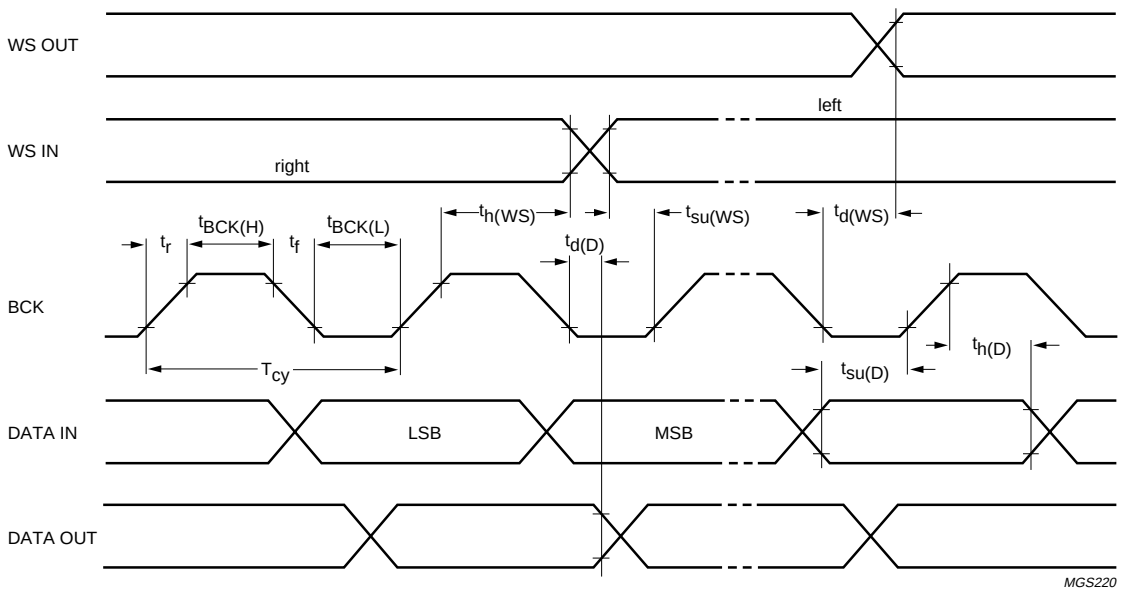


Fig.17 Timing definitions of the serial digital inputs and outputs.

16 I²C-BUS TIMING CHARACTERISTICS

Timing of the I²C-bus (see Fig.18); all values referred to V_{IH} and V_{IL} (see Section 12).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	SCL clock frequency		0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		1.3	–	µs
$t_{HD;STA}$	hold time (repeated) START condition; after this period, the first clock pulse is generated		0.6	–	µs
t_{LOW}	LOW period of the SCL clock		1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	µs
$t_{HD;DAT}$	data hold time		0	0.9	µs
$t_{SU;DAT}$	data set-up time	for standard mode I²C-bus system $t_{SU;DAT}$ > 250 ns	100	–	ns
t_r	rise time of both SDA and SCL signals	f_{SCL} = 400 kHz	$20 + 0.1C_b$[1]	300	ns
		f_{SCL} = 100 kHz	$20 + 0.1C_b$[1]	1000	ns
t_f	fall time of both SDA and SCL signals		$20 + 0.1C_b$[1]	300	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	µs
C_b	capacitive load for each bus line		–	400	pF
t_{SP}	maximum pulse width for spike suppression		–	50	ns

Note

1. C_b is the bus line capacitance in pF.

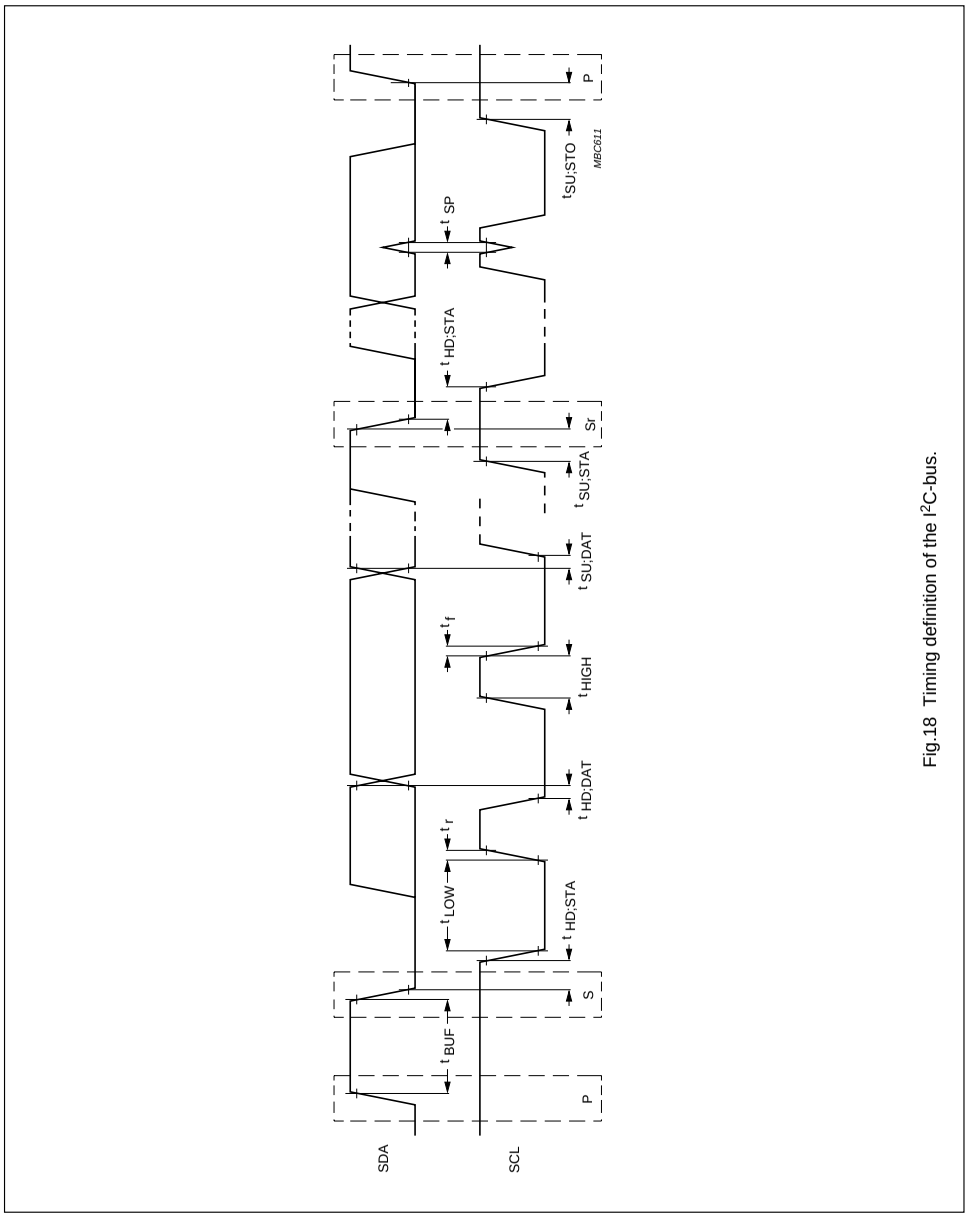


Fig.18 Timing definition of the I²C-bus.

17 APPLICATION INFORMATION

The application diagram (see Fig.19) must be considered as one of the examples of a (limited) application of the chip e.g. in this case the I²S-bus inputs are not used. For the real application set-up the information of the application report and application support by Philips are necessary on issues such as EMC, kappa reduction of the package, DSP programming, etc.

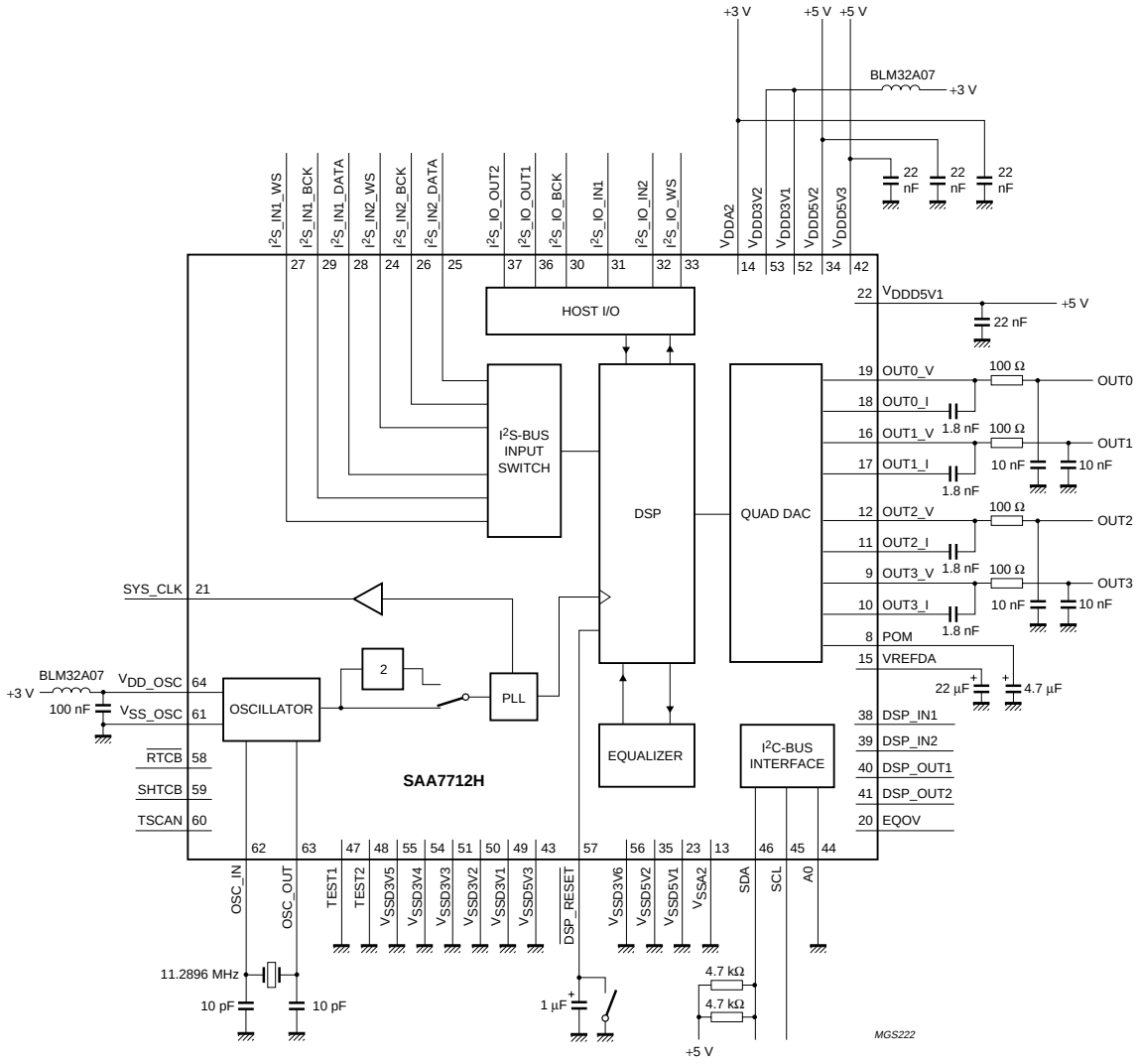
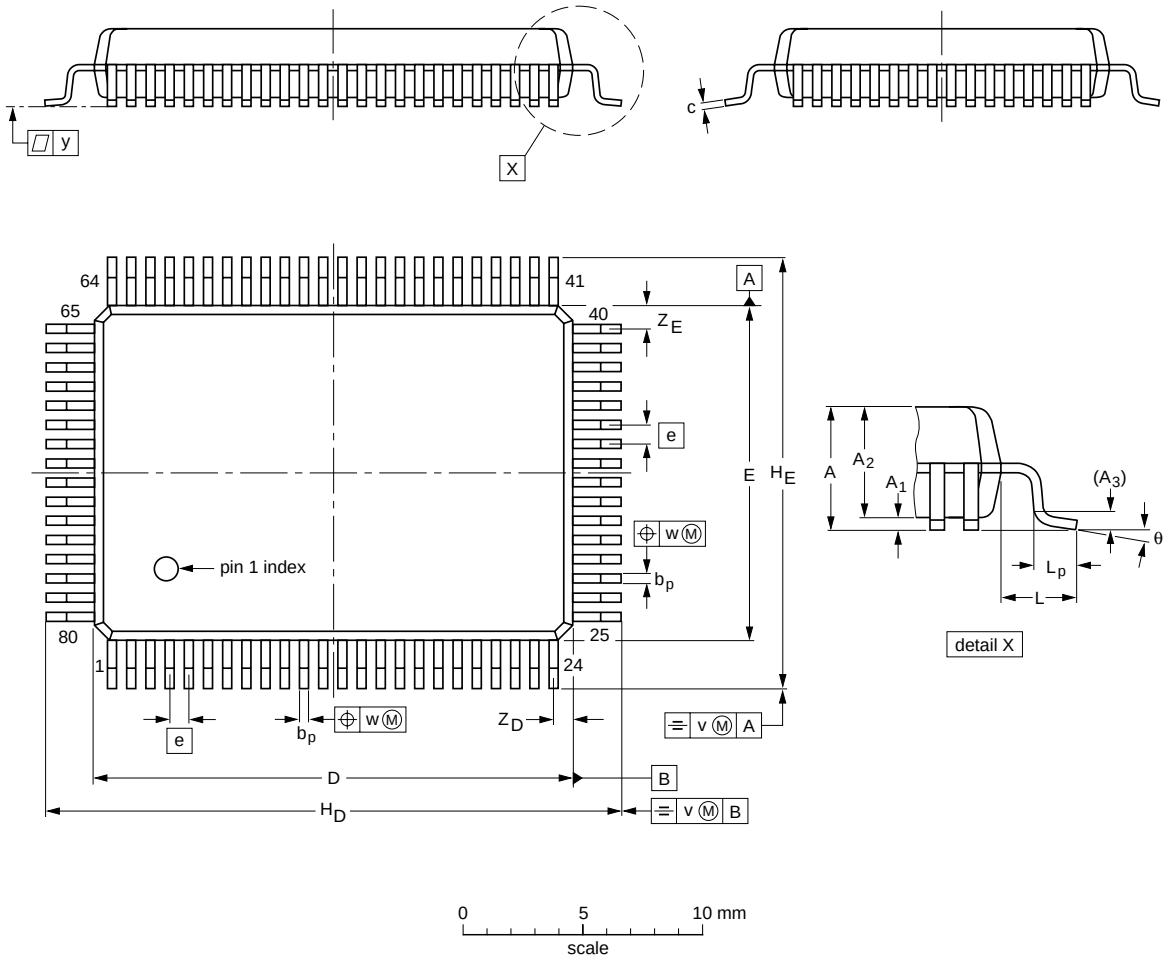


Fig.19 Application diagram.

18 PACKAGE OUTLINE

QFP80: plastic quad flat package;
80 leads (lead length 1.95 mm); body 14 x 20 x 2.7 mm; high stand-off height **SOT318-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.3	0.36 0.10	2.87 2.57	0.25	0.45 0.30	0.25 0.13	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-1						~~95-02-04~~ 97-08-01

19 SOLDERING

19.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

19.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

19.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

19.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

20 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

21 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

22 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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