DATA SHEET

SAA7201
Integrated MPEG2 AVG decoder

Objective specification

File under Integrated Circuits, IC02

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Integrated MPEG2 AVG decoder **SAA7201**

FEATURES

General

- Uses single external Synchronous DRAM (SDRAM) organized as 1M × 16 interfacing at 81 MHz; compatible with the SDRAM 'lite' or 'PC'
- Fast external CPU interface; 16-bit data + 8-bit address
- Dedicated input for audio and video data in PES or ES format; data input rate: ≤9 Mbytes/s in byte mode; ≤20 Mbit/s in bit serial mode; audio and/or video data can also serve as input via CPU interface
- Single 27 MHz external clock for time base reference and internal processing; all required decoding and presentation clocks are generated internally
- Internal system time base at 90 kHz can be synchronized via CPU port
- Flexible memory allocation under control of the external CPU enables optimized partitioning of memory for different tasks
- Boundary scan (JTAG) plus external SDRAM self test implemented
- Supply voltage 3.3 V
- Package 160 QFP.

CPU relation

- 16-bit data, 8-bit address, or 16-bit multiplexed bus; Motorola and Intel mode supported
- Support for fast DMA transfer to either internal registers or external SDRAM
- Maximum sustained rate to the external SDRAM is 9 Mbytes/s.

MPEG2 system

- Parsing of MPEG2 PES and MPEG1 packet streams
- Double System Time Clock (STC) counters for discontinuity handling
- Time stamps or CPU controlled audio/video synchronization
- Support for seamless time base change (edition)
- Processing of errors flagged by channel decoding or demux section
- Support for retrieval of PES header and PES private data.

MPEG2 audio

- Decoding of 2 channel, layer I and II MPEG audio; support for mono, stereo, intensity stereo and dual channel mode
- Constant and variable bit rates up to 448 kbit/s
- Audio sampling frequencies: 48, 44.1, 32, 24, 22.05 and 16 kHz
- CRC error detection
- Selectable output channel in dual channel mode
- Independent volume control for both channels and programmable inter-channel crosstalk control through a baseband audio processing unit
- Storage ancillary data up to 54 bytes
- Dynamic range control at output
- Muting possibility via external controller; automatic muting in case of errors
- Generation of 'beeps' with programmable tone height, duration and amplitude
- Serial two channel digital audio output with 16, 18, 20 or 22 bits per sample, compatible with either I^{2}S or Japanese formats
- Serial SPDIF audio output
- Clock output 256 or 384 × f_s for external D/A converter
- Audio input buffer in external SDRAM with programmable size (default is 64 kbit)
- Programmable processing delay compensation
- Software controlled stop, pause, restricted skip, and restart functions.

MPEG2 video

- Decoding of MPEG2 video up to main level, main profile
- Nominal video input buffer size equals 2.6 Mbit for Video Main Profile and Main Level (MP@ML)
- Output picture format: CCIR-601 4 : 2 : 2 interlaced pictures; picture format 720 × 576 at 50 Hz or 720 × 480 at 60 Hz
- 3 : 2 pull-down supported with 24 and 30 Hz sequences
- Support of constant and variable bit rates up to 15 Mbit/s
- Output interface at 8-bit wide, 27 MHz UYVY multiplexed bus
- Horizontal and vertical pan and scan allows the extraction of a window from the coded picture

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- Flexible horizontal continuous scaling from 0.5 up to 4 allows easy aspect ratio conversion including support for 2.21 : 1 aspect ratio movies

- Vertical scaling with fixed factors 0.5, 1 or 2 to support picture scaling and up-sampling

- Scaling of incoming pictures to 25% of their original size with anti-aliasing filtering to free screen space for graphics applications like electronic program guides

- Non-full screen MPEG pictures will be displayed in a box of which position and background colour are adjustable by the external CPU

- Video output may be slaved to internally (master) generated or externally (slave) supplied HV synchronization signals; the position of active video is programmable; MPEG timebase changes do not affected the display phase

- Video output direct connectable to SAA718X encoder family

- Various trick modes under control of external CPU:
  - Freeze I or P pictures; restart on I picture
  - Freeze on B pictures; restart at any moment
  - Scanning and decoding of I or I and P pictures
  - Single step mode
  - Repeat/Skip field for time base correction.

Graphics

- Graphics is region based and presented in boxes independent of video format

- Screen arrangement of boxes is determined by display list mechanism which allows for multiple boxes, background loading, fast switching, scrolling and fading of regions

- Support of 2, 4, 8 bits/pixel bit-maps in fixed bit-maps or coded in accordance to the DVB variable/run length standard for region bases graphics

- Optimized memory control in MPEG video decoding allows for storage of graphical bit-maps up to 1.2 Mbit in 50 Hz and 2.0 Mbit in 60 Hz systems

- VL/RL encoding enables full screen graphics at 8 bit/pixel in 50 Hz

- Fast CPU access enables full bit-map updates within a display field period

- Display colours are obtained via colour look-up tables; CLUT output is YUVT at 8-bit for each signal component thus enabling 16M different colours and 6-bit for T (transparency) which gives 64 mixing levels with video

- Bit-map table mechanism to specify a sub-set of entries if the CLUT is larger than required by the coded bit pattern; supported bit-map tables are 16 to 256, 4 to 256 and 4 to 16

- Graphics boxes may not overlap vertically; if 256 entry CLUT has to be down loaded, a vertical separation of 1 field line is mandatory

- Internal support for fast block moves in the external SDRAM during MPEG decoding

- Graphics mechanism can be used for signal generation in the vertical blanking interval; useful for teletext, wide screen signalling, closed caption etc.

- Support for a single down-loadable cursor of 1 kpixel with programmable shape; supported shapes are 8×128, 16×64, 32×32, 64×16 and 128×8

- Cursor colours are determined via a 4-entry CLUT with YUVT at 6, 4, 4 respectively 2 bits; mixing of cursor with video + graphics in 4 levels

- Cursor can be moved freely across the screen without overlapping restrictions.

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GENERAL DESCRIPTION

The SAA7201 is an MPEG2 decoder which combines audio decoding and video decoding. Additionally to these basic MPEG functions it also provides means for enhanced graphics and/or on-screen display.

Due to an optimized architecture for audio and video decoding, maximum capacity in the external memory and processing power from the external CPU is available for the support for graphics.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	functional supply voltage	3.0	3.3	3.6	V
V_{CC}	pad supply voltage	3.0	3.3	3.6	V
$I_{DD(tot)}$	total supply current at V_{DD} = 3.3 V	–	tbf	–	mA
f_{CLK}	clock frequency	–	27.0	–	MHz
Δf_{CLK}	frequency deviation	-30×10^{-6}	–	$+30 \times 10^{-6}$	

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7201H	QFP160	plastic quad flat package; 160 leads (lead length 1.95 mm); body 28 × 28 × 3.4 mm; high stand-off height	SOT322-4

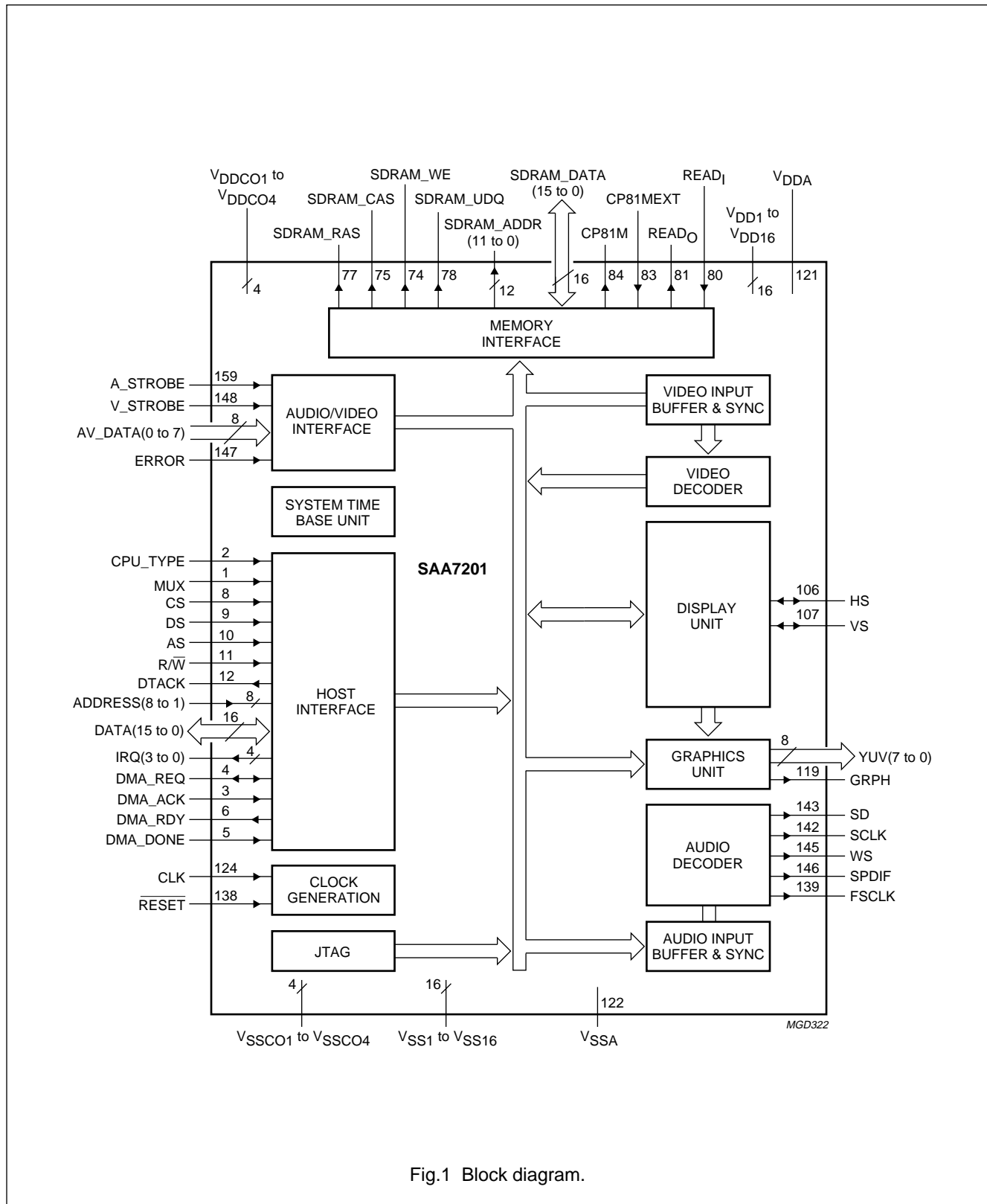# Integrated MPEG2 AVG decoder   SAA7201

BLOCK DIAGRAM

Fig.1 Block diagram.

Integrated MPEG2 AVG decoder

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PINNING

SYMBOL	PIN	DESCRIPTION	V	I/O
MUX	1	multiplexed/non-multiplexed (active LOW) bus input	5.0	I
CPU_TYPE	2	Intel/Motorola (active LOW) selection input	5.0	I
DMA_ACK	3	DMA acknowledge input	3.3	I
DMA_REQ	4	DMA request input and output	3.3	I/O
DMA_DONE	5	DMA end input	3.3	I
DMA_RDY	6	DMA ready output	3.3	O/Z
V_{SS1}	7	ground for pad ring	3.3	–
CS	8	chip select input	5.0	I
DS	9	data strobe input	5.0	I
AS	10	address strobe input	5.0	I
R/$\overline{W}$	11	read/write (active LOW) input	5.0	I
DTACK	12	data acknowledge output	5.0	O/Z
V_{DD1}	13	supply for pad ring	3.3	–
IRQ0	14	individually maskable interrupts	3.3	O/Z
IRQ1	15	individually maskable interrupts	3.3	O/Z
IRQ2	16	individually maskable interrupts	3.3	O/Z
IRQ3	17	individually maskable interrupts	3.3	O/Z
V_{SS2}	18	ground for pad ring	–	–
V_{SSCO1}	19	ground for core logic	–	–
V_{DDCO1}	20	supply for core logic	3.3	–
DATA0	21	CPU data interface	5.0	I/O
DATA1	22	CPU data interface	5.0	I/O
DATA2	23	CPU data interface	5.0	I/O
DATA3	24	CPU data interface	5.0	I/O
V_{DD2}	25	supply for pad ring	3.3	–
DATA4	26	CPU data interface	5.0	I/O
DATA5	27	CPU data interface	5.0	I/O
DATA6	28	CPU data interface	5.0	I/O
DATA7	29	CPU data interface	5.0	I/O
V_{SS3}	30	ground for pad ring	–	–
DATA8	31	CPU data interface	5.0	I/O
DATA9	32	CPU data interface	5.0	I/O
DATA10	33	CPU data interface	5.0	I/O
DATA11	34	CPU data interface	5.0	I/O
V_{DD3}	35	supply for pad ring	–	–
DATA12	36	CPU data interface	5.0	I/O
DATA13	37	CPU data interface	5.0	I/O
DATA14	38	CPU data interface	5.0	I/O
DATA15	39	CPU data interface	5.0	I/O
V_{SS4}	40	ground for pad ring	–	–

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SYMBOL	PIN	DESCRIPTION	V	I/O
ADDRESS1	41	CPU address interface	5.0	I
ADDRESS2	42	CPU address interface	5.0	I
ADDRESS3	43	CPU address interface	5.0	I
ADDRESS4	44	CPU address interface	5.0	I
V_{DD4}	45	supply for pad ring	3.3	–
ADDRESS5	46	CPU address interface	5.0	I
ADDRESS6	47	CPU address interface	5.0	I
ADDRESS7	48	CPU address interface	5.0	I
ADDRESS8	49	CPU address interface	5.0	I
V_{SS5}	50	ground for pad ring	–	–
V_{SSCO2}	51	ground for core logic	–	–
V_{DDCO2}	52	supply for core logic	3.3	–
SDRAM_DATA0	53	memory data interface	3.3	I/O
SDRAM_DATA15	54	memory data interface	3.3	I/O
SDRAM_DATA1	55	memory data interface	3.3	I/O
V_{DD5}	56	supply for pad ring	3.3	–
SDRAM_DATA14	57	memory data interface	3.3	I/O
SDRAM_DATA2	58	memory data interface	3.3	I/O
SDRAM_DATA13	59	memory data interface	3.3	I/O
V_{SS6}	60	ground for pad ring	–	–
SDRAM_DATA3	61	memory data interface	3.3	I/O
SDRAM_DATA12	62	memory data interface	3.3	I/O
SDRAM_DATA4	63	memory data interface	3.3	I/O
V_{DD6}	64	supply for pad ring	3.3	–
SDRAM_DATA11	65	memory data interface	3.3	I/O
SDRAM_DATA5	66	memory data interface	3.3	I/O
SDRAM_DATA10	67	memory data interface	3.3	I/O
V_{SS7}	68	ground for pad ring	–	–
SDRAM_DATA6	69	memory data interface	3.3	I/O
SDRAM_DATA9	70	memory data interface	3.3	I/O
SDRAM_DATA7	71	memory data interface	3.3	I/O
V_{DD7}	72	supply for pad ring	3.3	–
SDRAM_DATA8	73	memory data interface	3.3	I/O
SDRAM_WE	74	SDRAM write enable output	3.3	O
SDRAM_CAS	75	SDRAM column address strobe output	3.3	O
V_{SS8}	76	ground for pad ring	–	–
SDRAM_RAS	77	SDRAM row address strobe output	3.3	O
SDRAM_UDQ	78	SDRAM write mask output	3.3	O
V_{DD8}	79	supply for pad ring	3.3	–
READ$_I$	80	read command input	3.3	I

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SYMBOL	PIN	DESCRIPTION	V	I/O
READ$_O$	81	read command output	3.3	O
V$_{SS9}$	82	ground for pad ring	–	–
CP81MEXT	83	81 MHz clock return path input	3.3	I
CP81M	84	81 MHz memory clock output	3.3	O
V$_{DD9}$	85	supply for pad ring	3.3	–
SDRAM_ADDR8	86	memory address	3.3	O
SDRAM_ADDR9	87	memory address	3.3	O
SDRAM_ADDR11	88	memory address	3.3	O
V$_{SS10}$	89	ground for pad ring	–	–
SDRAM_ADDR7	90	memory address	3.3	O
SDRAM_ADDR10	91	memory address	3.3	O
SDRAM_ADDR6	92	memory address	3.3	O
V$_{DD10}$	93	supply for pad ring	3.3	–
SDRAM_ADDR0	94	memory address	3.3	O
SDRAM_ADDR5	95	memory address	3.3	O
SDRAM_ADDR1	96	memory address	3.3	O
V$_{SS11}$	97	ground for pad ring	–	–
SDRAM_ADDR4	98	memory address	3.3	O
SDRAM_ADDR2	99	memory address	3.3	O
SDRAM_ADDR3	100	memory address	3.3	O
V$_{SSCO3}$	101	ground for core logic	–	–
V$_{DDCO3}$	102	supply for core logic	3.3	–
V$_{DD11}$	103	supply for pad ring	3.3	–
TEST8	104	IC test interface	3.3	I/O
TEST7	105	IC test interface	3.3	I/O
HS	106	horizontal synchronization input and output	3.3	I/O
VS	107	vertical synchronization input and output	3.3	I/O
V$_{SS12}$	108	ground for pad ring	–	–
YUV0	109	YUV video output at 27 MHz	3.3	O/Z
YUV1	110	YUV video output at 27 MHz	3.3	O/Z
YUV2	111	YUV video output at 27 MHz	3.3	O/Z
YUV3	112	YUV video output at 27 MHz	3.3	O/Z
V$_{DD12}$	113	supply for pad ring	3.3	–
YUV4	114	YUV video output at 27 MHz	3.3	O/Z
YUV5	115	YUV video output at 27 MHz	3.3	O/Z
YUV6	116	YUV video output at 27 MHz	3.3	O/Z
YUV7	117	YUV video output at 27 MHz	3.3	O/Z
TEST6	118	IC test interface	3.3	I/O
GRPH	119	indicator for graphics information output	3.3	O
TEST5	120	IC test interface	3.3	I/O

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SYMBOL	PIN	DESCRIPTION	V	I/O
V_{DDA}	121	supply for analogue blocks	3.3	–
V_{SSA}	122	ground for analogue blocks	–	–
V_{SS13}	123	ground for pad ring	–	–
CLK	124	27 MHz clock input	3.3	I
V_{SS14}	125	ground for pad ring	–	–
TCLK	126	boundary scan test clock input	3.3	I
TRST	127	boundary scan test reset input	3.3	I
TMS	128	boundary scan test mode select input	3.3	I
TD_O	129	boundary scan test data output	3.3	O
TD_I	130	boundary scan test data input	3.3	I
V_{DD13}	131	supply for pad ring	3.3	–
TEST4	132	IC test interface	3.3	I/O
TEST3	133	IC test interface	3.3	I/O
TEST2	134	IC test interface	3.3	I/O
TEST1	135	IC test interface	3.3	I/O
TEST0	136	IC test interface	3.3	I/O
V_{DD14}	137	supply for pad ring	3.3	–
$\overline{RESET}$	138	hard reset input (active LOW)	3.3	I
FSCLK	139	256 or 384 f_s (audio sampling) output	3.3	O/Z
V_{DDCO4}	140	supply for core logic	3.3	–
V_{SSCO4}	141	ground for core logic	–	–
SCLK	142	serial audio clock output	3.3	O/Z
SD	143	serial audio data output	3.3	O/Z
V_{SS15}	144	ground for pad ring	–	–
WS	145	word select output	3.3	O/Z
SPDIF	146	digital audio output	3.3	O/Z
ERROR	147	flag for bitstream error input	5.0	I
V_STROBE	148	video strobe input	5.0	I
V_{DD15}	149	supply for pad ring	3.3	–
AV_DATA0	150	MPEG input port for PES data	5.0	I
AV_DATA1	151	MPEG input port for PES data	5.0	I
AV_DATA2	152	MPEG input port for PES data	5.0	I
AV_DATA3	153	MPEG input port for PES data	5.0	I
V_{SS16}	154	ground for pad ring	–	–
AV_DATA4	155	MPEG input port for PES data	5.0	I
AV_DATA5	156	MPEG input port for PES data	5.0	I
AV_DATA6	157	MPEG input port for PES data	5.0	I
AV_DATA7	158	MPEG input port for PES data	5.0	I
A_STROBE	159	audio strobe input	5.0	I
V_{DD16}	160	supply for pad ring	3.3	–

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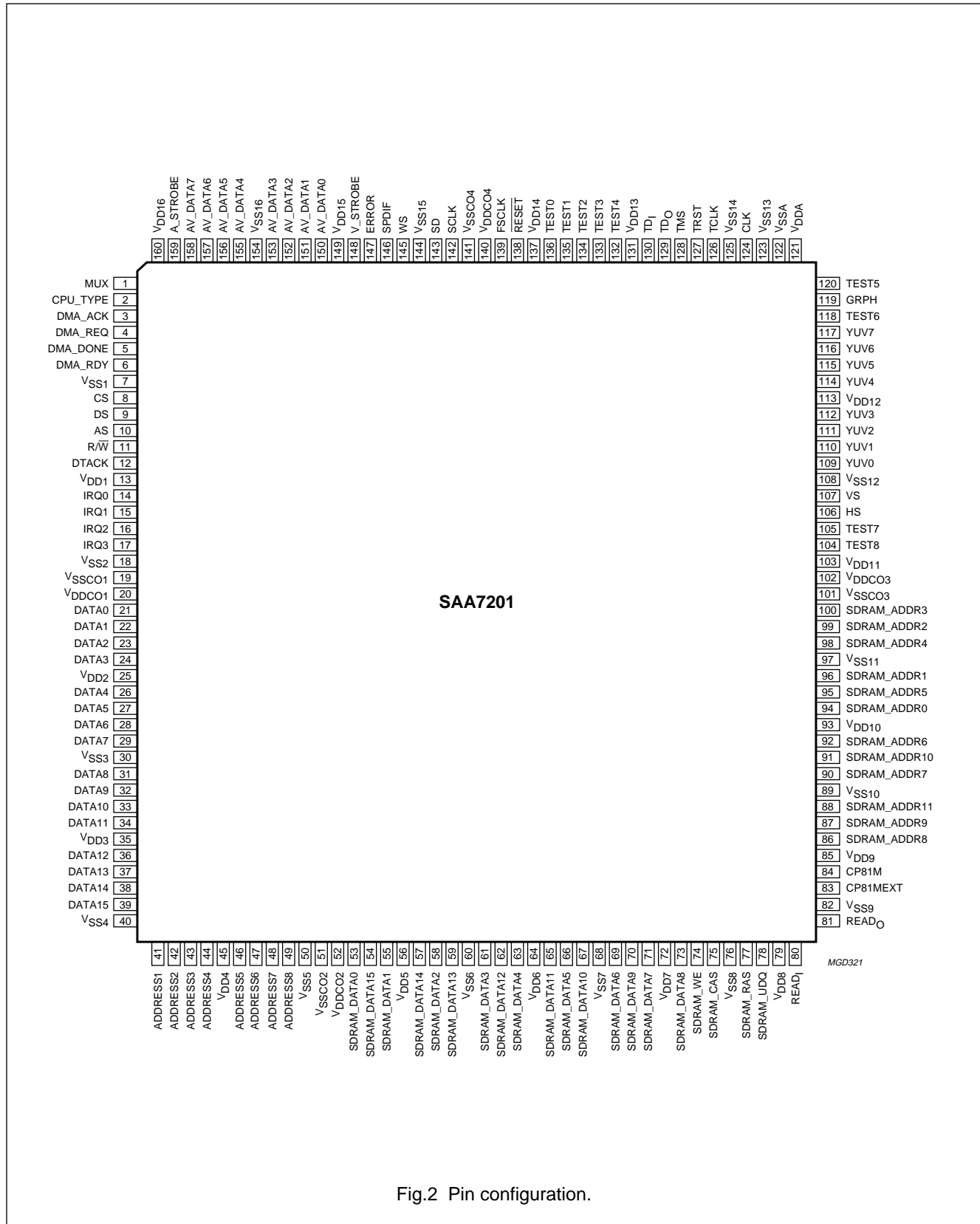

Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

General

The SAA7201 is an MPEG2 decoder which combines audio decoding, video decoding and enhanced region based graphics. The decoder operates with a single 16 Mbit external synchronous dynamic random access memory (SDRAM) and runs from a single external 27 MHz clock. Due to the optimized memory control for MPEG2 decoding, more than 1 Mbit is available for graphics in 50 Hz systems.

MPEG2 data can be accepted up to 9 Mbytes/s through a dedicated byte wide interface. The data on this interface can be either in PES (Packetized Elementary Stream), MPEG1 packet or ES (Elementary Stream) format as described in Chapter "References". Two additional strobe signals distinguish between audio and video data.

The internal video decoder is capable of decoding all MPEG compliant streams up to main level main profile as specified in Chapter "References". The audio decoder implements 2 channel audio decoding according to the standards in Chapter "References".

All real time audio/video decoding and synchronization tasks are performed autonomously, so the external microcontroller only needs to perform high-level tasks like initialization, status monitoring and trick mode control.

The main support task of the external microcontroller concerns the control of the graphical unit. This unit should be supplied with bit-maps, determining the contents of the graphical regions and by a simple set of instructions determining the appearance of the graphical data on the screen. Most graphical information should be stored in the external memory which implies multiple data transfers between CPU and the external memory. By performing these data transfers on a direct memory access (DMA) basis, full bit-maps can be transferred within one video frame period.

The video output, containing a mix of MPEG video and graphical data, is at a YUV multiplexed format which can be directly connected to an external composite video encoder. The audio output, containing a mix of MPEG audio and programmable 'beeps', is in a serial, I^2S or Japanese format which can be directly supplied to most commercially available up-sampling audio DA converters.

A functional block diagram of the decoder is given in Fig.1. Its application environment is depicted in Fig.24. In the following sections, a brief description of the individual internal blocks of the MPEG2 decoder will be given.

Audio/video interface

In a basic set-top box application the SAA7201 receives audio and video PES data in a byte wide format at rates up to 9 Mbytes/s. A timing diagram is shown in Fig.3. Next to the 8-bit wide data bus an audio and video strobe is expected at the input. Erroneous data may be flagged via the error indicator.
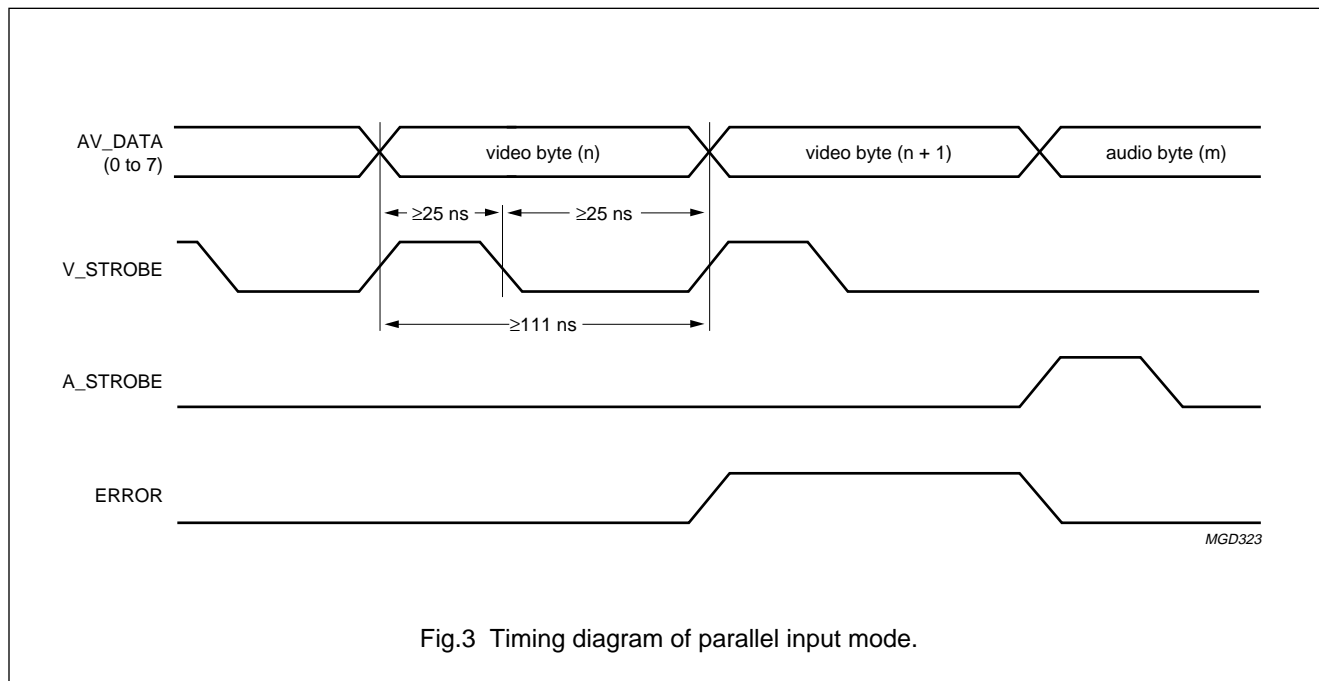
Fig.3 Timing diagram of parallel input mode.

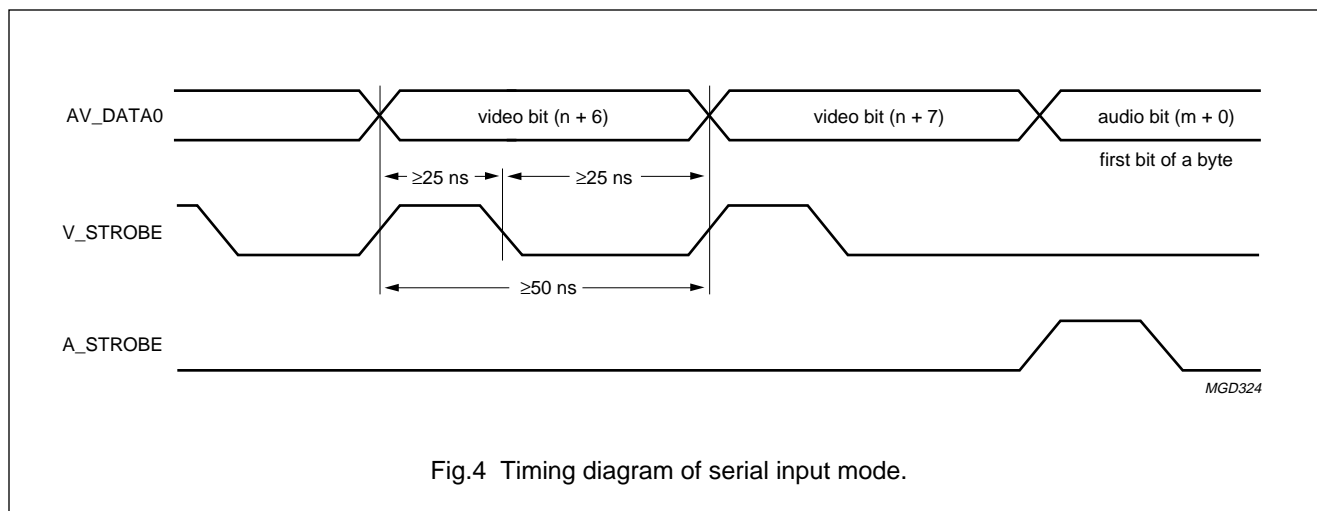# Integrated MPEG2 AVG decoder

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Fig.4 Timing diagram of serial input mode.

Alternatively data can be received in a 1-bit serial format at rates up to 20 Mbit/s. In this mode, data is input at the LSB input of the AV_DATA bus. Audio and video data must be input in multiples of 8 bits. The first bit after switching from audio to video (or the other way around) must be the first bit of a byte since this transition will be used for the internal bit-to-byte conversion.

Audio/video data can also be received via the CPU interface in 8 or 16-bit mode. The peak rate is 27 Mbytes/s in bursts of ≤128 bytes with a sustained rate up to 9 Mbytes/s. However, the MPEG bit rate is still limited to 15 Mbit/s for video and 448 kbit/s for audio.

Independent of the input mode all audio and video input data are stored sequentially in the audio or video input buffer area of the external memory. The audio and video data can be either in MPEG2 PES, MPEG1 packet or ES format.

Memory interface unit

The memory interface takes care of addressing and control of the 16-Mbit external SDRAM. The SDRAM should be either JEDEC compliant either the 'lite/PC' version.

Due to memory communication requirements this interface runs at 81 MHz. The SDRAM types used with the SAA7201 should be organized as 1M × 16, split internally in two banks, each having 2048 pages of 256 words of 16 bits.

The target SDRAM type is NEC μPD 4516161G5-A12-7FJ (83 MHz JEDEC version) or NEC μPD 4516421G5-A83-7FJ-PC (83 Mhz PC version).

Clock generation

The clock generation unit generates all the internal processing clocks, the clock for the system time base counter and the audio oversampling clock for the audio DAC. For this purpose a non-integer divider plus a PLL is implemented. In order to get reliable audio and video decoding the 27 MHz input clock should be locked externally to the MPEG time base.

Host interface system

The host interface system handles the communication between on one side the SAA7201 plus SDRAM and on the other side the external CPU. The interface consists of a 16-bit wide data bus plus 8 address lines. It is compatible with both Motorola's 68xxx and Intel's x86 family. An optimized interface with the SAA7208 is also supported. Via this interface a fast direct access to a large number of internal status and data registers can be achieved. Moreover, the external SDRAM can be accessed via a specific register in combination with an internally implemented auto increment counter. The access to the external SDRAM is guaranteed up to a sustained data rate of 9 Mbyte per second. However, in practice the achievable data rate can be much higher.

Next to the data and address lines, 4 interrupt lines are part of the host interface bus. Each interrupt line can monitor up to 32 internal events which all can be masked individually. Examples of internal events are audio/video bit stream information, decoder status, internal error conditions and input buffer occupation. The latter may be very useful in interactive applications to serve as input data request line.

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System time base unit

The system time base unit serves as a timing master for all internal processes. It consists of two 24-bit wide System Time Clock (STC) counters, running at 90 kHz. The STCs will be used as internal synchronization reference for audio and video.The contents of the STC can be loaded by the external CPU which should insure that the phase of the SAA7201 internal STC is identical to the main system time clock in the system demultiplexer. The CPU should correct for possible latency problems.

Because two counters are implemented, the previous time base reference which might still be required as reference for some time in case of time base discontinuity, can be maintained. Thus all information for audio/video synchronization is available in the decoder chip and only minor support of the external controller is required.

The synchronization of graphics for e.g. subtitling, should be controlled by the external CPU.

Video input buffer and synchronization control

The size and position of the video input buffer in the external SDRAM is programmable. By default 2.6 Mbit/s are reserved for the video input buffer but in principle any other value can be programmed. The current fullness of the video input buffer can be monitored by the CPU and an internal interrupt will be generated is case of either near over- or near underflow.

Data retrieval from the input buffer can be controlled by DTS time stamps parsed from the PES or MPEG1 packet stream. For those frames where no DTS time stamp is present in the video bitstream a DTS is emulated by the SAA7201.

Obviously this emulation mode can also be used when the input stream is a video elementary stream (ES). The latter case should be handled by start and stop decode commands from the CPU.

The external CPU can select to retrieve the video PES header and/or video PES private data for further software processing.

Audio input buffer and synchronization control

The audio input buffer and synchronization control basically behaves identical to its video counter part. The default buffer size is 64 kbit in this case. Synchronization will be controlled by PTS time stamps in the audio Packetized Elementary Stream. Also in this case an PTS emulation or a free running start/stop controlled mode are supported.

Audio decoder

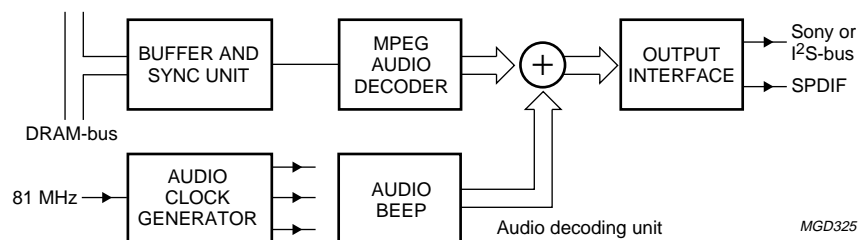A functional block diagram for the audio decoding part is depicted in Fig.5.

Fig.5 Audio decoding unit.

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Audio decoding will be performed at a clock locked to the video decoding clock and only the output interface is running on the audio oversampling clock.

The audio decoder unit performs the decoding of the selected MPEG audio stream in a range from 8 up to 448 kbit/s in a fixed or variable bit rate format. Decoding is restricted to 2 channel, layer I, II MPEG audio at sampling frequency of 48.0, 44.1, 32.0, 24.0, 22.05 or 16.0 kHz.

The audio decoder support the stop, mute, and skip function to support insertion

Apart from basic MPEG processing the audio decoder core contain also:

- Support for: stop, mute and skip function.

- Fully parameterized dynamic range compression unit to decrease the dynamic range of the output signal on audio frame basis. Depending on the power level a programmable amplification and offset may be applied.

- Fully programmable base band audio processing unit to control the gain in both output channels independently and/or to mix both channels.

- MPEG de-emphasis filtering on the output data, thus avoiding the need of external analog de-emphasis filter circuitry.

- Storage buffer for the last 54 bytes of each audio frame. The CPU can retrieve eventual ancillary data from this buffer.

The output of the audio decoder unit can be mixed with square waveform audio signals which are generated by a beep generator. Programmable parameters for the beep generator are amplitude, frequency and duration.

The audio output interface module produces stereo base band output samples on two different outputs at the same time:

- Serial digital audio in I^2S-bus or in Japanese format in 16, 18, 20 or 22-bit

- SPDIF (Sony/Philips Digital Interface).

Any of the two outputs may be enabled or set to high impedance mode. The I^2S-bus format with 18-bit sample precision is shown in Fig.6.

The difference between I^2S-bus and the Japanese format is that I^2S-bus is MSB aligned whereas the Japanese format is LSB aligned.

The 1-bit serial interface SPDIF contains 64-bit per audio sample period. Complete frames must be transmitted at the audio sample rate. Not only left/right information but also validity flags, channel status, user data and parity information is contained in an SPDIF frame (see Chapter "References").
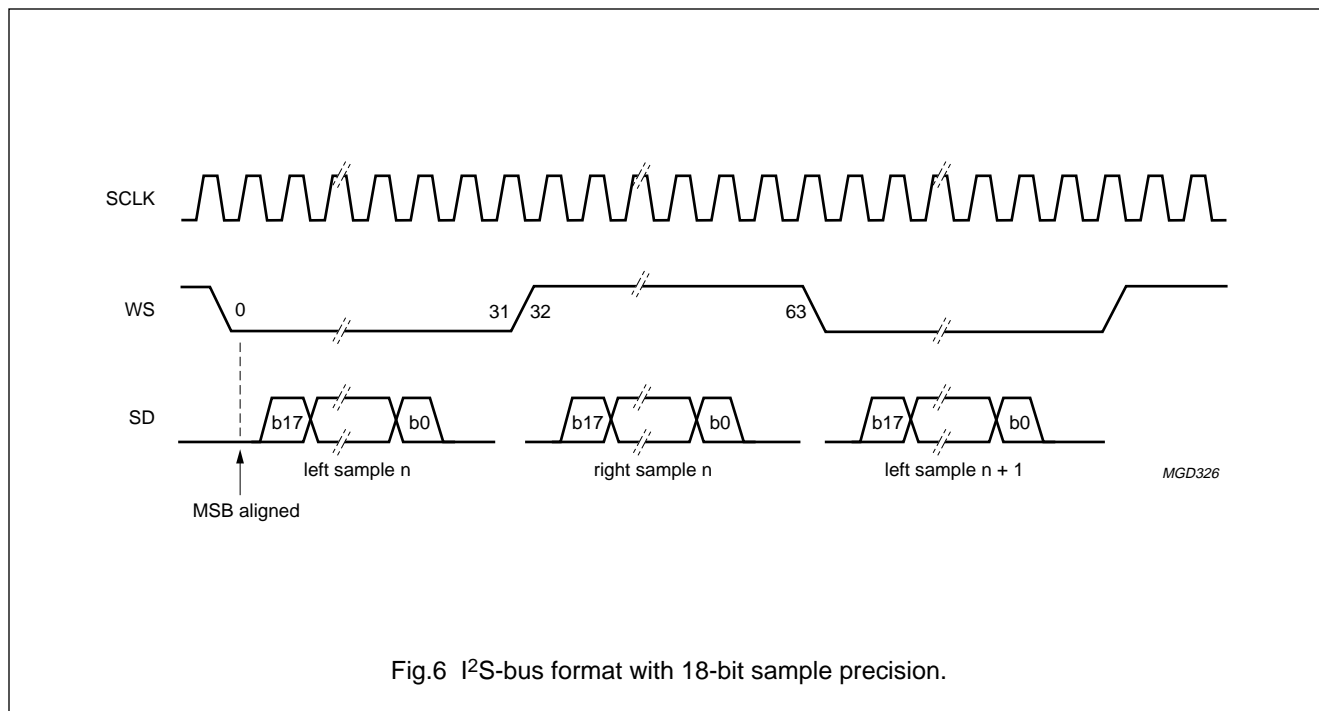

Fig.6 I^2S-bus format with 18-bit sample precision.

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Video decoder

The video decoding unit provides all actions required for compliant decoding of MPEG2 main level, main profile coded video bit streams. The decoding process consists of fixed and variable length decoding, run length decoding, inverse quantization, inverse discrete cosine transformation, motion compensation and interpolation.

In general the arithmetic decoding result is stored as reference picture in the external memory.
Decoded B-frames are only stored for the conversion from the frame coded macro block (MB) to the scanning line format. In many cases a field storage is sufficient for this conversion but in some cases the user might decide to use a full frame storage to enable chroma frame up-conversion or full performance 3 : 2 pull-down in 60 Hz systems. Obviously when using less memory for the video decoding process more memory is available for non-video decoding tasks.

The Frame Buffer Management unit (FBM) manages the allocation of frame buffers in external SDRAM for both video decoding and display unit and can be programmed to use less memory in not fully MP@ML bitstreams: smaller pictures (e.g. 544×576), simple profile, etc.

Apart from decoding compliant MPEG video streams the decoder deals with some trick modes. Supported are field or frame freeze at I or P pictures or freeze field on B-pictures. In the latter case decoding will continue as a background process and the output can be restarted at any moment. When receiving non-compliant MPEG streams the decoder can be switched to a scanning mode in which only I or I + P frames are decoded while skipping all other pictures. In the single step mode, the decoder decodes just one frame and awaits a next step command.

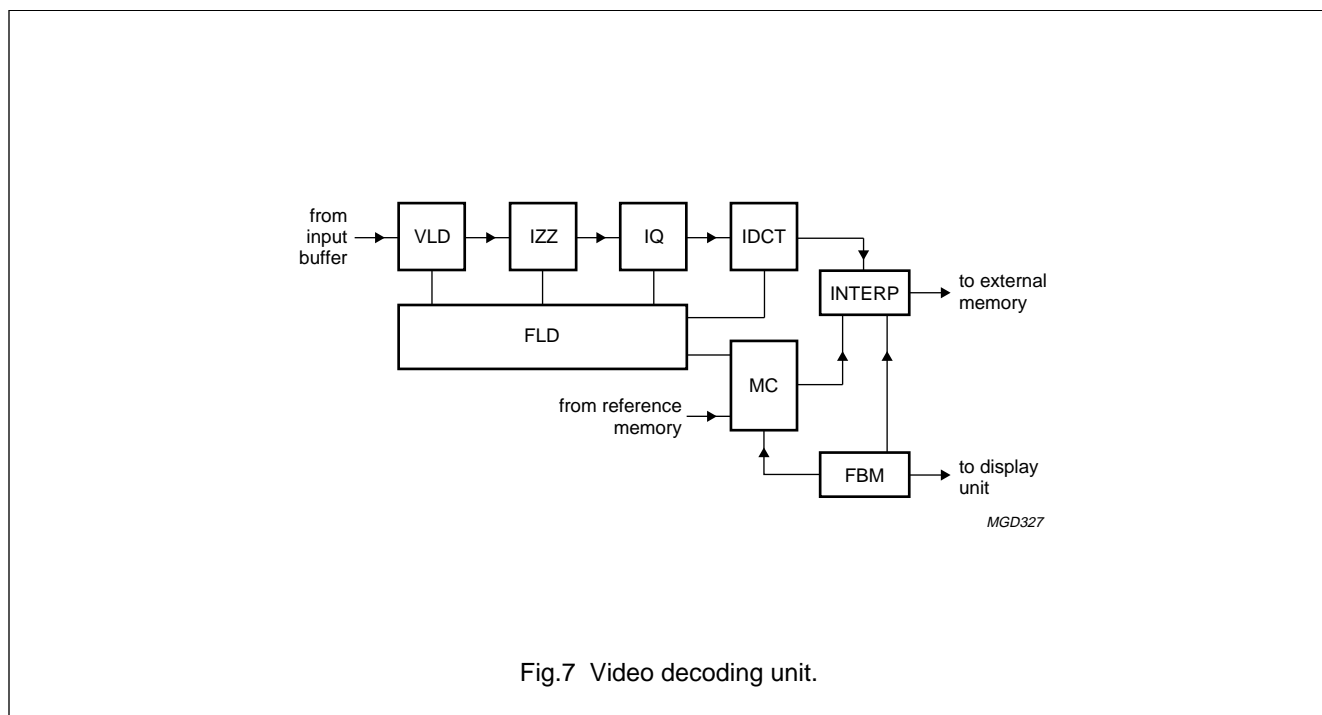The functional diagram of the video decoding unit is shown in Fig.7.

Fig.7 Video decoding unit.

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Graphics unit

The SAA7201 incorporates the display support for pixel based graphics. Possible applications are the user interface, logos and subtitling. Graphical data should be grouped logically in regions and will be displayed in boxes at the screen.

The definition of each region in the decoder consists of four parts being a region descriptor, a top-field descriptor, a bottom-field descriptor and a table-data descriptor:

- The region descriptor contains information relevant for the full region like format, size, position and pointers to the other descriptors.

- The top-field and bottom-field descriptor contain a pixel based bit-map for the contents of that region for both fields independently. The bit-maps can be stored in either straight forward or in a compressed bit-map format.

- The table-data descriptor defines the tables to be used for the transformation of bit-maps to display colours.

All descriptors should be loaded under control of the external CPU in the external memory.

The appearance of graphical data at the display is determined by the assembly of region descriptors in a so called display list. An example of such a display list for the 4 regions example is shown in Fig.9.
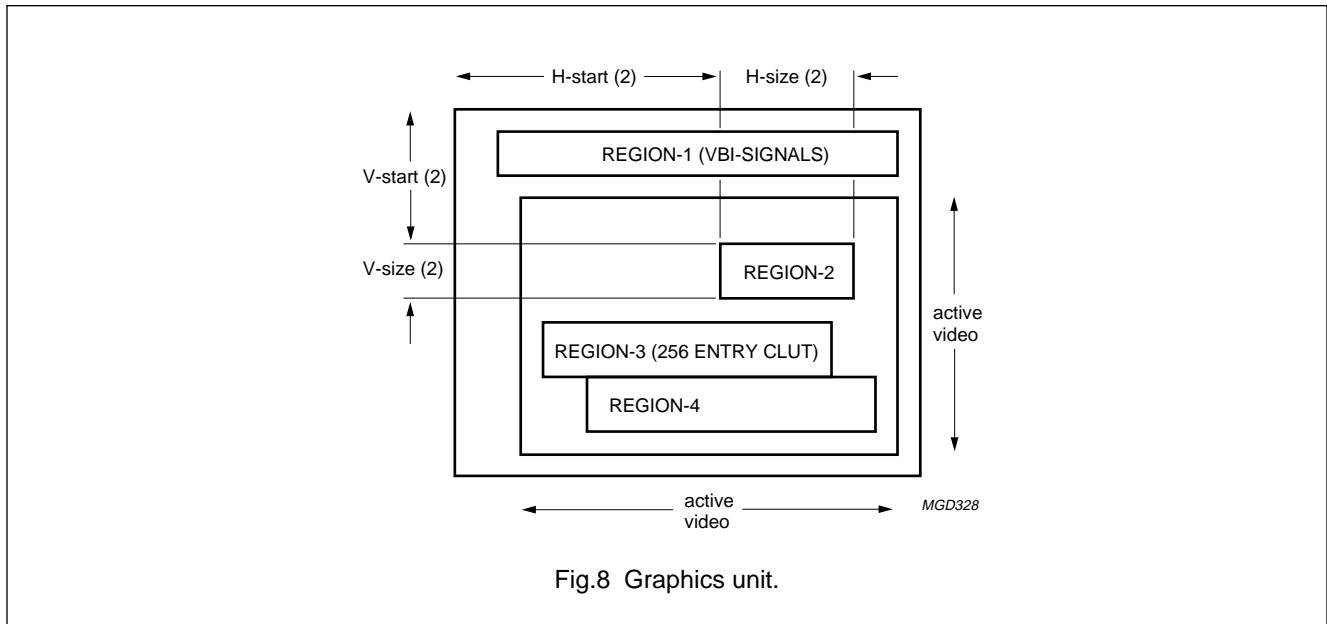
Fig.8 Graphics unit.
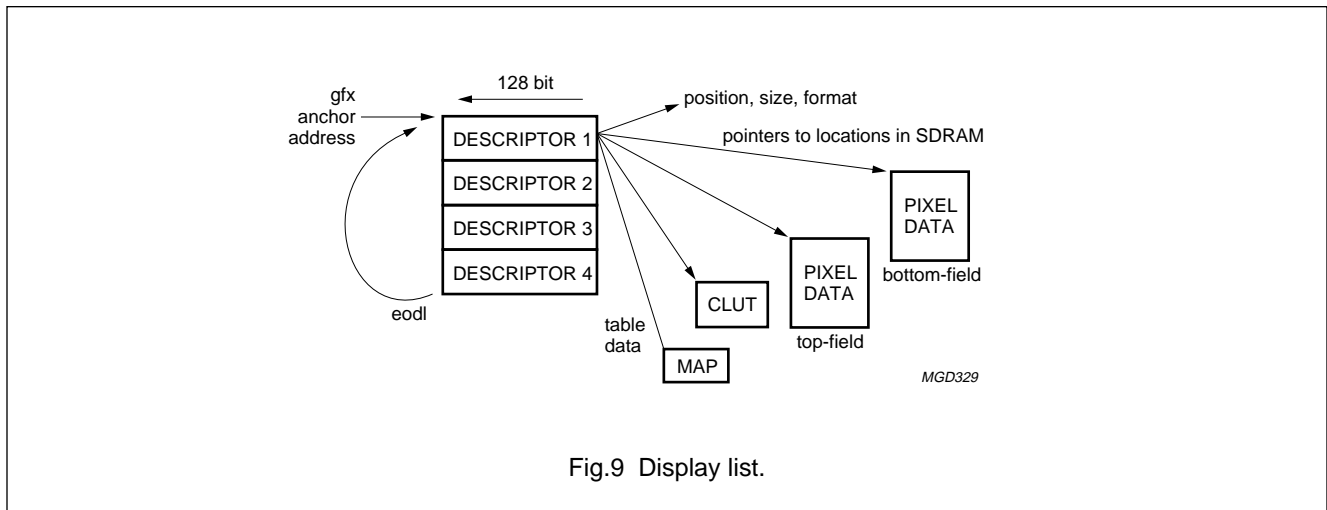
Fig.9 Display list.

Basically there is no restriction on the number of different regions but because regions may not vertically overlap the practical limit will be the number of lines within a field. However, one should realize that each region requires its own 128-bit region descriptor.

The display list will be scanned twice per frame, once for each display field. The region descriptors should be ordered properly in the external SDRAM, starting from the graphics anchor address. The last descriptor in the list must have the end of display list indicator set.

Multiple pixel bit-maps, CLUTs and map tables may be stored in the external memory but per region only two bit-maps (one for each fields) and two tables (CLUT + map table) may be used. Obviously bit-maps and tables may be shared by multiple regions.

Pixel data bit-maps can be described in 2, 4 or 8 bit/pixel in either a direct bit-map or coded in a one-dimensional (H) variable and run length encoded format according the pixel-data-sub-block syntax as specified in Chapter "References" and illustrated in Chapter "Appendix". The actual coding format is specified in the region descriptor for each region thus allowing different coding schemes within a picture.

During display the 2, 4 and 8 bit/pixel bit-maps will be transformed, eventually with run length decoding, via a table look-up mechanism into a 4, 16 or 256 different YUV colours with 8-bit resolution for each component plus a factor T for mixing of graphics and MPEG video.

In order to obtain maximum flexibility two cascaded tables are active in this bit-map to pixel conversion as indicated in Fig.10.

The tables are retrieved from the external memory just before the region is going to be displayed. One table per region can be updated and for small tables this occurs during the horizontal blanking interval. However, updating a 256 entry CLUT may take about one line period which means that a spatial separation of one line with the previous region is mandatory in this case. If the required tables for a certain region are already stored in the local memory, the table down load action can be skipped.

Additionally some special bits can be set in the region descriptor.

- Transparency shift: this parameter overrules the pixel based transparency in order to support fading of the entire graphical region.
- Zoom: this parameter initiates horizontal pixel repetition. It should be noted that a copy of pixels in vertical direction can be achieved by pointing to a single bit-map for both fields.

Regions can also be defined in the vertical blanking interval. In combination with 8 bit/pixel coding, arbitrary test signals on 13.5 MHz grid can be programmed. Possible application areas are teletext, closed caption, wide screen signalling bits, Video Programming Signals (VPS) and Vertical Interval Test Signals (VITS).

As indicated above multiple regions can be specified in a display list which will be scanned sequentially every frame. In case of stationary graphics no updates of the display list are required, but the external CPU can update it dynamically to achieve scrolling and/or fading of one or more graphical boxes. The display list mechanism also allows for non real time transfer of large bit-maps by keeping that region out of the display list during loading.
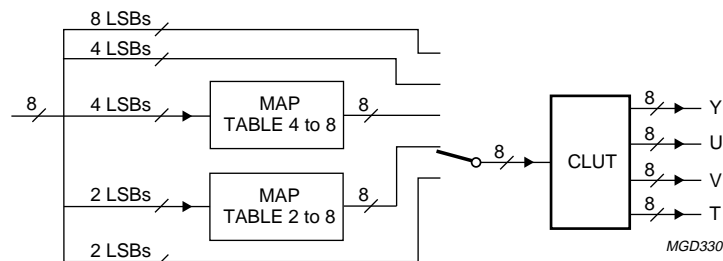

Fig.10 Bit-map to pixel conversion.

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CURSOR PROCESSING

Additionally to the above defined graphics boxes one cursor can be activated on the screen. Since the cursor data is fully stored locally, no overlapping restriction apply to this box so the cursor can moved over the entire screen. The cursor can be as large as 1 kpixel with a 2 bits/pixel colour depth. Obviously data transfer can be done on DMA basis and need only be performed when a cursor is required or when its contents must be modified.

The cursor XY dimensions (where the Y dimension refers to frame lines) can be selected between 8×128, 16×64, 32×32, 64×16 and 128×8. On top of these shapes, a zoom with a factor 2 can be applied in both directions independently.

The cursor pixels will be translated via a 4-entry CLUT to YUV colours and a transparency factor T. The resolution of the YUV parameters is 6, 4, 4 bits respectively. The T parameter is coded in 2 bits to enable the mixing with video and graphics in 4 steps being 100% (cursor only), 50%, 25% and 0% (fully transparent cursor).

Display unit

Before feeding the MPEG decoded and graphical data to the output, a display unit re-formats the MPEG specific 4 : 2 : 0 format to CCIR-601 4 : 2 : 2 format and performs a mixing between video and graphics where required. The output picture can be up to 720×576 pixels at 50 Hz or 720×480 pixels at 60 Hz.

A schematic representation of this unit is shown in Fig.11.

- In a first step a selected window can be retrieved from the decoded MPEG data. This might be useful for e.g. pan and scan operations for aspect ratio conversion.

- In case the resulting number of pixels per line does not match the 720 pixels/line output format a horizontal scaler can be activated. This scaling unit can transform any number of bits below 720 to the required output format. Internally a poly-phase filter is used which performs a 64 phases interpolation. Not only up-conversion but also down-conversion is supported up to a scaling by a factor 2. Thus horizontal scaling can be performed in a range from 0.5 up to 64. In practice the maximum up-conversion factor will be less or equal to 4.

- In vertical direction the picture can be expanded or scaled down, in both cases by a factor 2. Expansion with a factor 2 might be relevant for the up-conversion of SIF resolution pictures to full screen. The factor 2 scaling, if combined with the appropriate horizontal scaling, results is $\frac{1}{4}$ picture thus freeing-up a large screen area for graphics. This might be very useful for electronic program guide applications. It should be noted that in case of picture compression an anti-aliasing filter can be activated.

- Shifting: when the resulting MPEG picture is smaller than the 720×576 (480) display format, this picture can be located anywhere on the display screen. Moreover, the non-covered area can be given any background colour.

- Clipping: the amplitude of the MPEG decoded and re-scaled video signal is kept within the range 16 to 235 for luminance and 16 to 240 for both chrominance components.
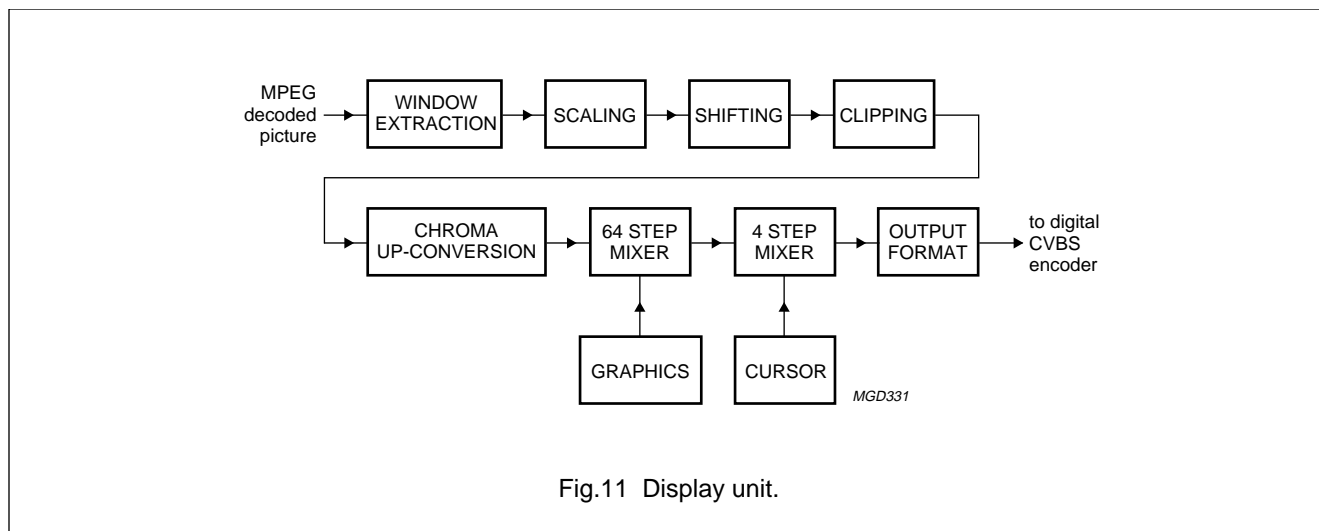

Fig.11 Display unit.

- The chroma up-conversion unit converts the MPEG 4 : 2 : 0 format into the at the output required 4 : 2 : 2 format. This vertical up-conversion is performed by a simple 8-phase interpolation between two adjacent lines.

- The mixer units combine MPEG video with graphics and cursor information in two steps. In a first step the MPEG decoded information is mixed with graphical information. Mixing can be done at pixel basis in 64 steps and is controlled by the internally implemented colour look up table. In a second step, the video plus graphics can be mixed in 4 steps with the internally generated cursor.

- The output formatting unit performs two main tasks, i.e. synchronization and formatting. Synchronization is characterized by three signals being horizontal (H), vertical (V) and field parity (FP), all having programmable length and polarity.

Since the decoder can operate in master or slave mode, the synchronization signals can be generated by the decoder or should be delivered by an external device. In both cases the length and polarity should be programmed internally.

The video output samples are supplied in a multiplexed YUV format to the output. Next to this byte wide YUV stream, which can directly be supplied to most commercially available composite video encoder ICs, three additional signals are delivered at the output. HREF indicates all active samples; CREF can flag any combination of pixels: U, V, Y_{odd} and/or Y_{even}; GRPH flags all the pixels inside a graphical box.

Additionally the full YUV bus can be set to a HIGH impedance state under control of the signal YUV_ENA. This might be useful for multiplexing the MPEG decoder output with any other signal source on static basis.
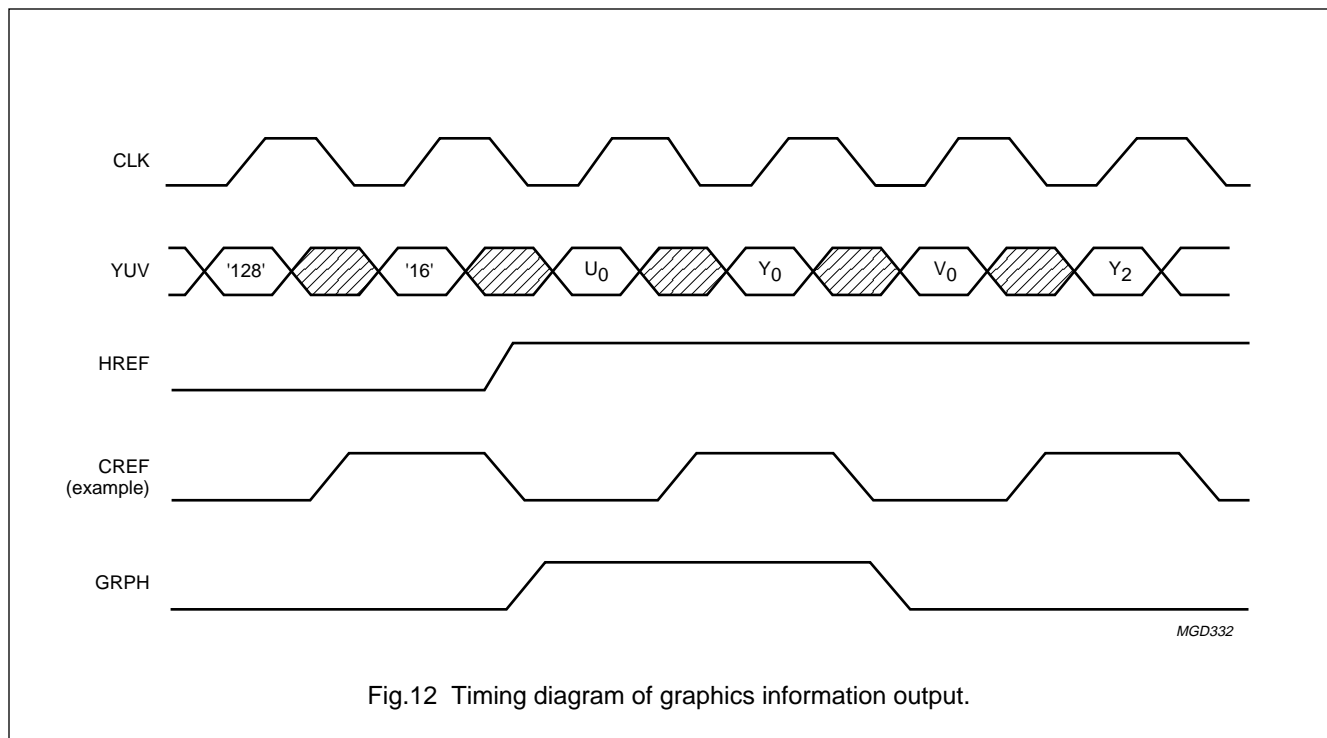

MGD332

Fig.12 Timing diagram of graphics information output.

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JTAG

The SAA7201 supports the standard Boundary Scan test instructions: bypass, extest, sample, intest, runbist, idcode.

Memory requirements

As indicated before the MPEG source decoder operates with 16 Mbit of external memory. Several processes require access to the external memory, mostly being the video decoding process. In normal main level, main profile video applications about 1.2 Mbit of memory space is free for non-video processes. In practice most of this capacity will be used for graphics. In combination with the internal variable length decoding, full screen graphics at 8-bit per pixel is feasible. Moreover, by having introduced a flexible memory allocation procedure the available memory capacity for graphics may be enlarged when decoding lower resolution MPEG pictures or when the input bit rate is less than 15 Mbit/s.

Obviously for graphics-only applications all 16 Mbit can be used for the storage of bit-maps and look-up tables.

In Table 1 an overview is given of the required memory capacity for some user defined modes.

In 50 Hz systems memory capacity can be saved by restricting the chroma vertical interpolation to field interpolation. This mode would only bring some extra chroma resolution in case the input stream contains progressive coded pictures.

In 60 Hz systems the reduction of storage capacity for B-frames to field capacity has not only consequences for the chroma vertical interpolation but also for the 3 : 2 pull-down operation mode. The operation repeat-first-field is not possible in all cases and a modified 3 : 2 pull-down is performed under the control of the SAA7201. The user may decide to use this modified 3 : 2 pull-down mode in order to have more memory available for OSD or graphics.

Table 1 Required memory capacity for some user defined modes

System	50 Hz			60 Hz		
Bit rate (R)	15 Mbit/s			15 Mbit/s		9 Mbit/s
Chroma interpolation	frame	field	field	frame	field	field
3 : 2 pull-down	n.a.	n.a.	n.a.	full MPEG	modified	modified
Picture format	720×576	720×576	544×576	720×480	720×480	720×480
Audio input buffer	64 kbit	64 kbit	64 kbit	64 kbit	64 kbit	64 kbit
Video input buffer	1835 kbit	1835 kbit	1835 kbit	1835 kbit	1835 kbit	1835 kbit
Video implementation buffer (R/P)	600 kbit	600 kbit	400 kbit	500 kbit	500 kbit	300 kbit
Slave synchronization buffer (R/2P)	300 kbit	300 kbit	200 kbit	250 kbit	250 kbit	150 kbit
Reference and decoded picture	13456 kbit	12719 kbit	9609 kbit	12441 kbit	10634 kbit	8042 kbit
Total for video + audio	16255 kbit	15518 kbit	12108 kbit	15090 kbit	13292 kbit	10391 kbit
Remains for OSDG (2^{24} = 16777 kbit)	522 kbit	1259 kbit	4669 kbit	1687 kbit	3485 kbit	6386 kbit

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (on all supply pins)		3.0	3.6	V
V_{max}	maximum voltage on all pins		0	5.5	V
P_{tot}	total power dissipation	$T_{amb} = 25\ °C$	–	tbf	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	30	K/W

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CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_{DD}	supply voltage	3.0	3.3	3.6	V
I_{DD}	supply current	–	tbf	–	mA
Inputs					
V_{IH}	HIGH level input voltage	2.0	–	$V_{DD} + 2.0$	V
V_{IL}	LOW level input voltage	–0.5	–	0.8	V
I_{LI}	leakage current	–	–	20	mA
C_i	input capacitance	0	–	10	pF
Outputs					
V_{OH}	HIGH level output voltage	2.4	–	–	V
V_{OL}	LOW level output voltage	–	–	0.4	V
CLK timing					
T_C	cycle time	37.036	37.037	37.038	ns
δ	duty factor	40	–	60	%
t_r	rise time	2	–	4	ns
t_f	fall time	2	–	4	ns
Input timing with respect to CLK rising edge					
t_{su}	set-up time	8	–	–	ns
t_h	hold time	0	–	–	ns
Timing (see Figs. 13, 14, 15, 16, 17, 18, 19, 20, 21, 21 and 21)					
$t_{su(A\text{-}CS)}$	address/CS set-up time	20	–	–	ns
$t_{h(A\text{-}CS)}$	address/CS hold time	75	–	–	ns
$t_{su(D\text{-}W)}$	data write set-up time	20	–	–	ns
$t_{su(D\text{-}R)}$	data read set-up time	20	–	–	ns
$t_{rel(D)}$	data release time	0	–	10	ns
$t_{h(CT)}$	control signal hold time	0	–	–	ns
$t_{W(ACK)}$	acknowledge pulse width	25	–	–	ns
$t_{rel(ACK)}$	acknowledge release time	0	–	10	ns
$t_{d(ACK\text{-}R)}$	delay time for acknowledge read	96	–	125	ns
$t_{d(ACK\text{-}W)}$	delay time for acknowledge write	48	–	75	ns
$t_{W(RW)}$	write/read pulse width	25	–	–	ns
Output timing with respect to CLK rising edge					
t_h	hold time	3	–	t_d	ns
t_d	delay time	t_h	–	20	ns
C_L	load capacitance	10	–	30	pF

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Fig.13 Motorola write timing (non-multiplexed).

Fig.14 Motorola read timing (non-multiplexed).
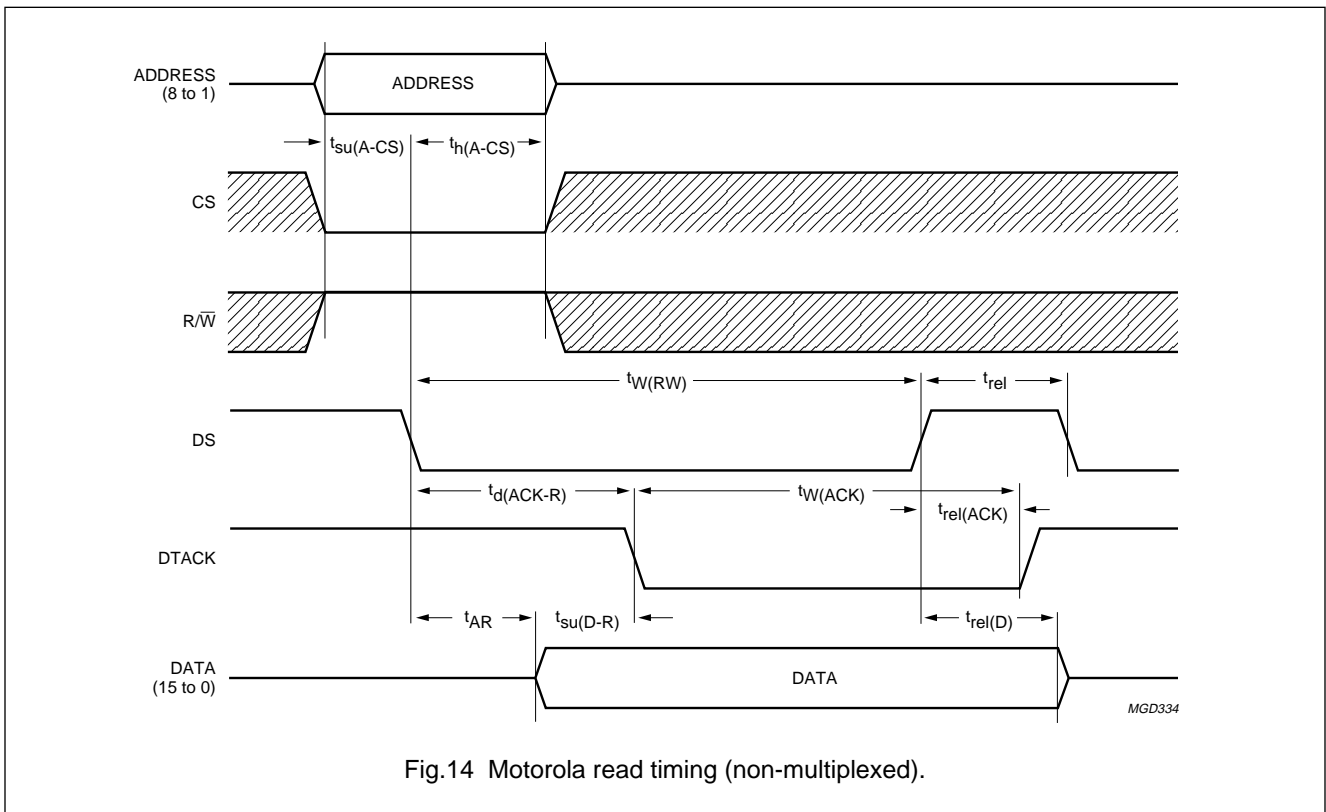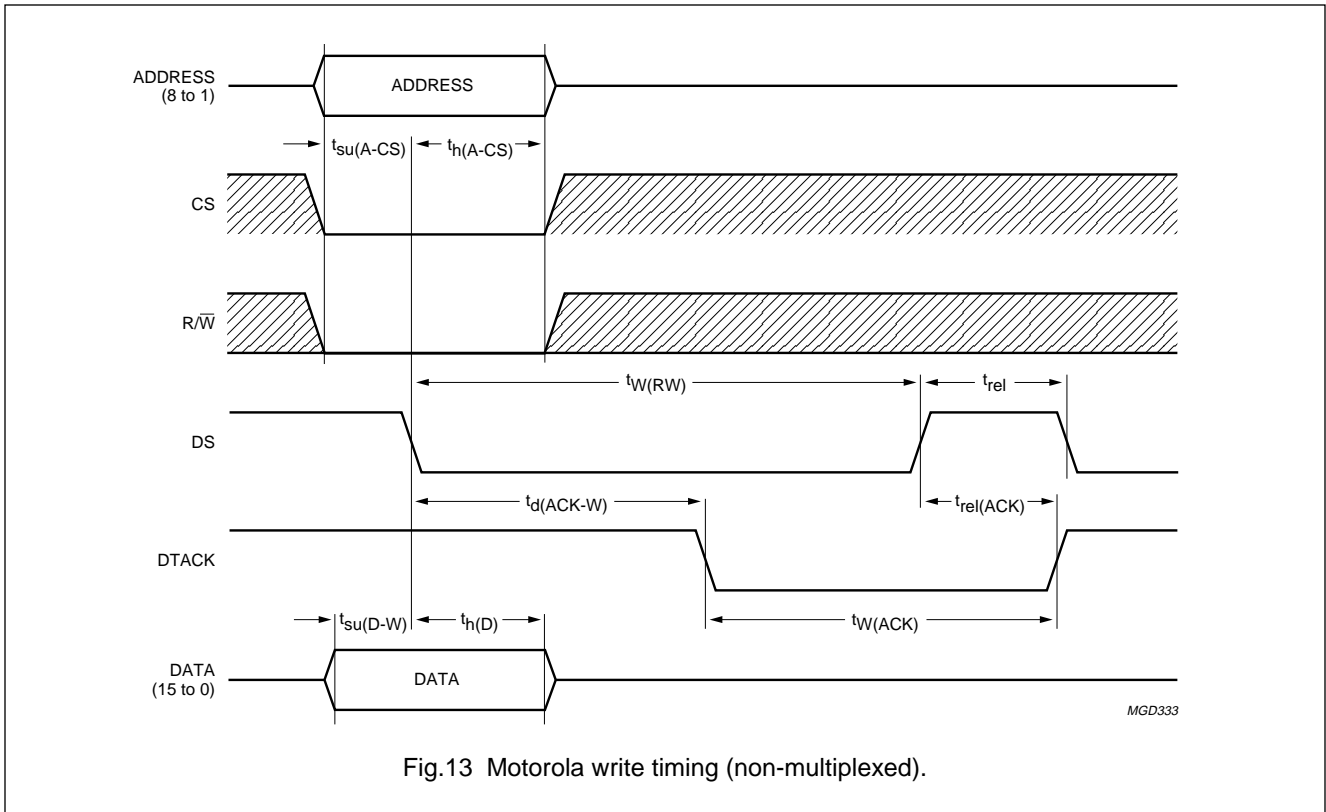
Integrated MPEG2 AVG decoder
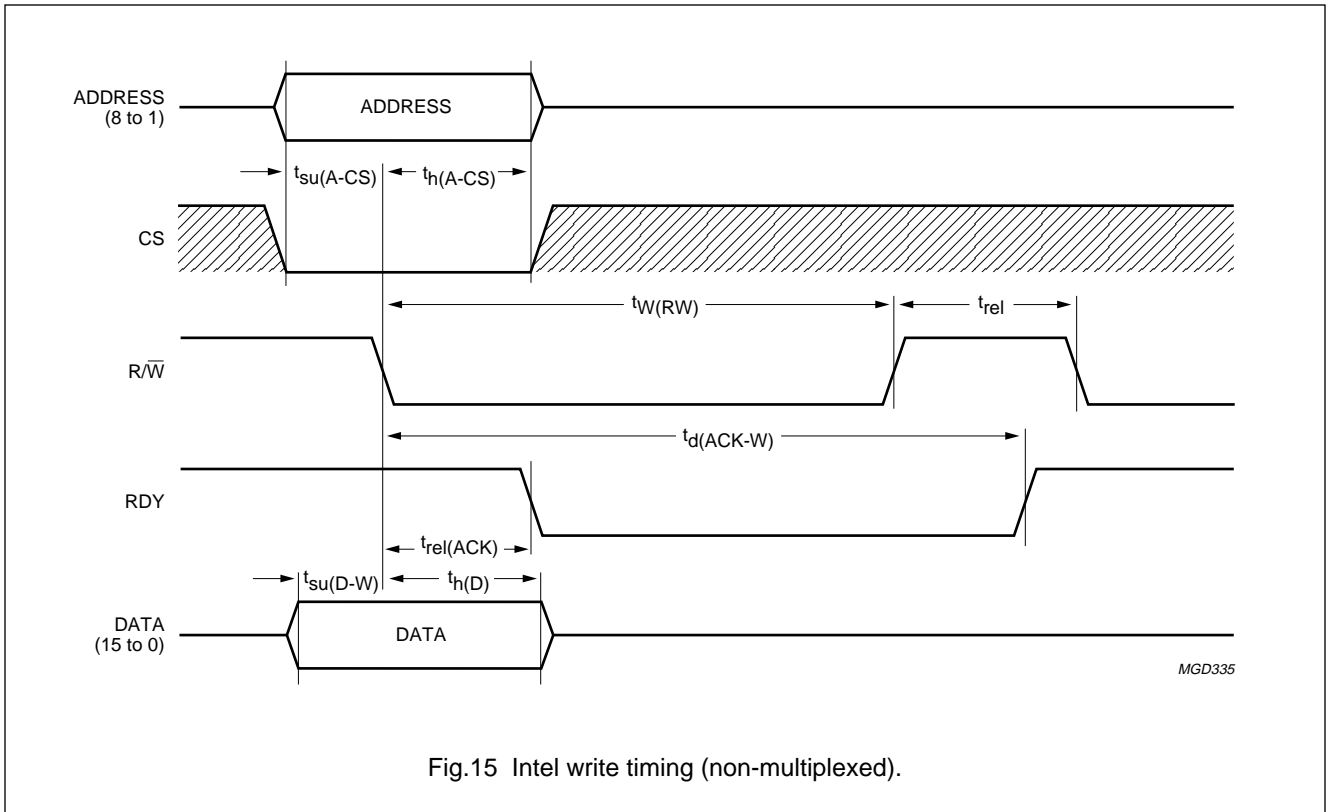
SAA7201

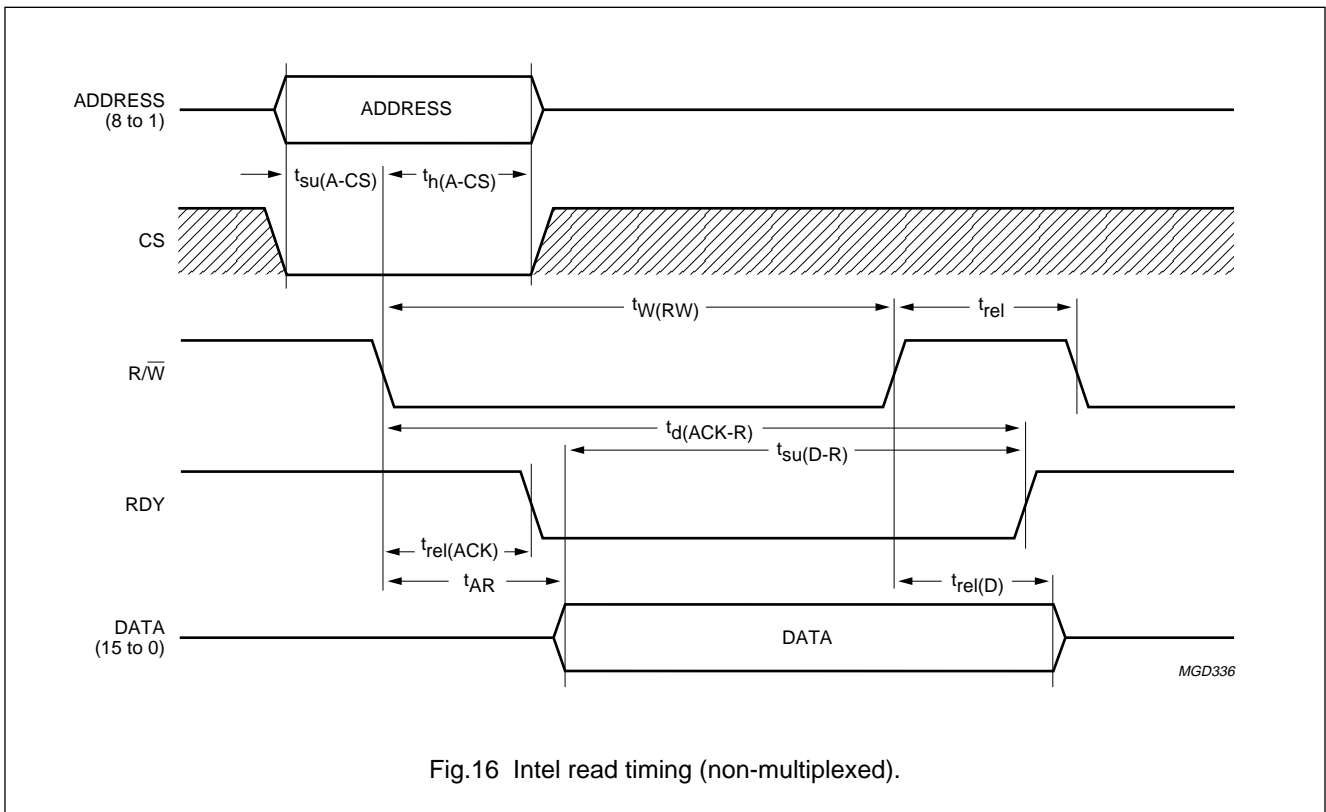Fig.15 Intel write timing (non-multiplexed).

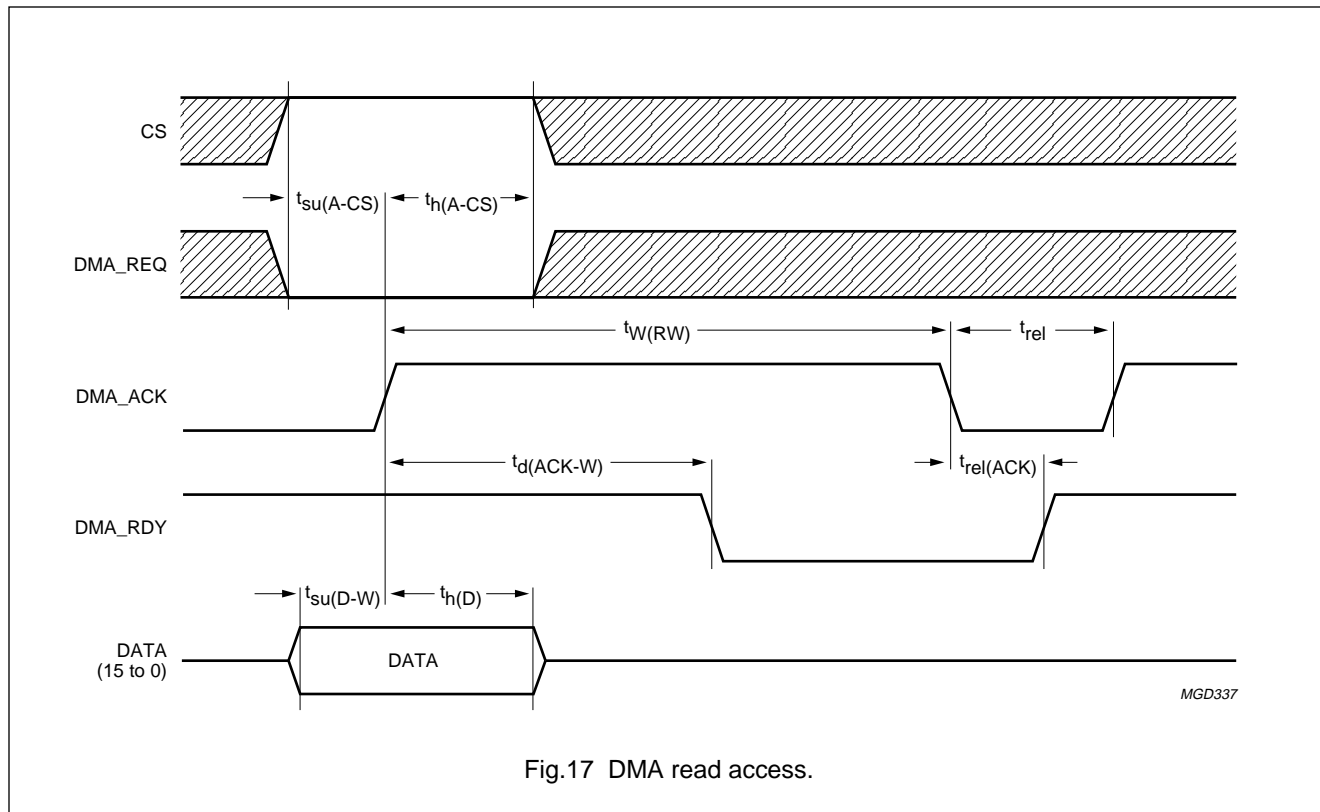Fig.16 Intel read timing (non-multiplexed).

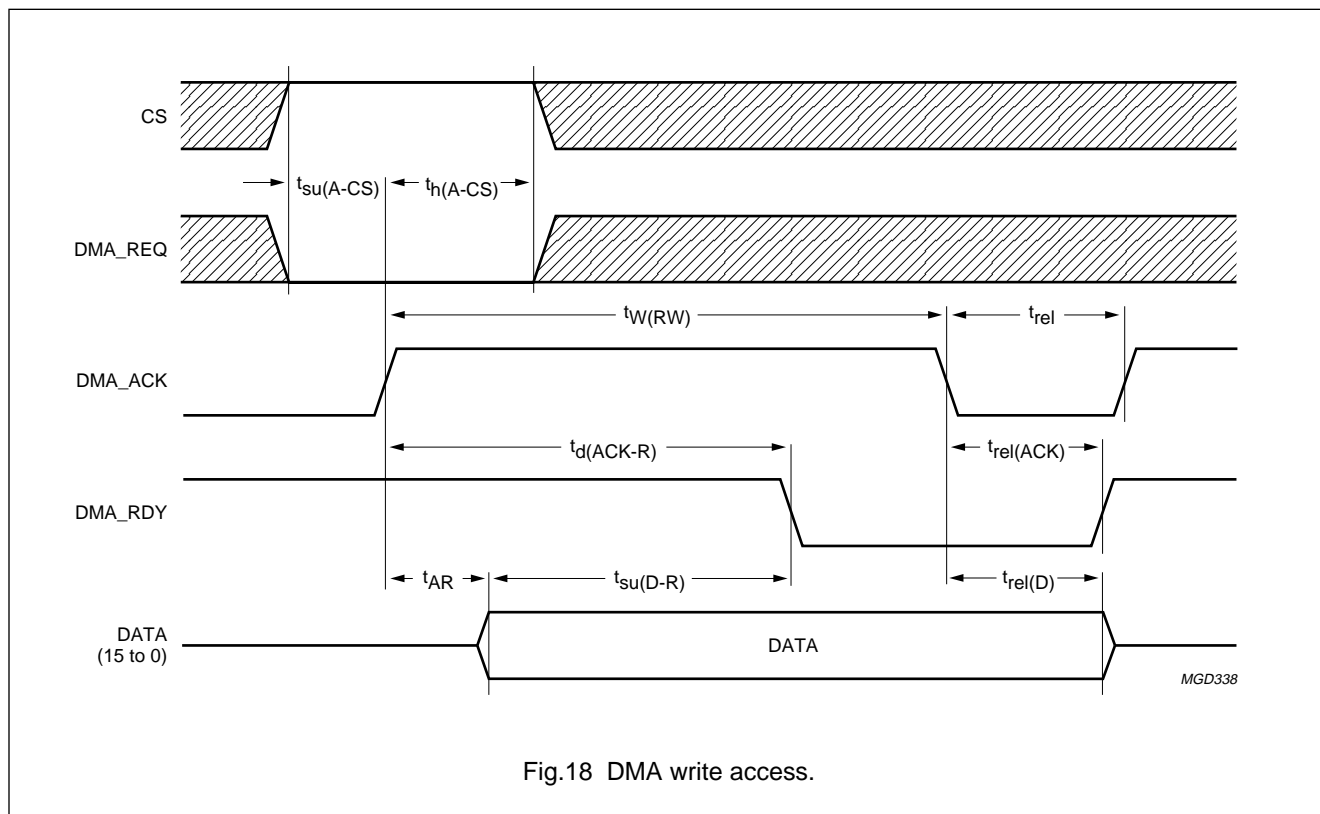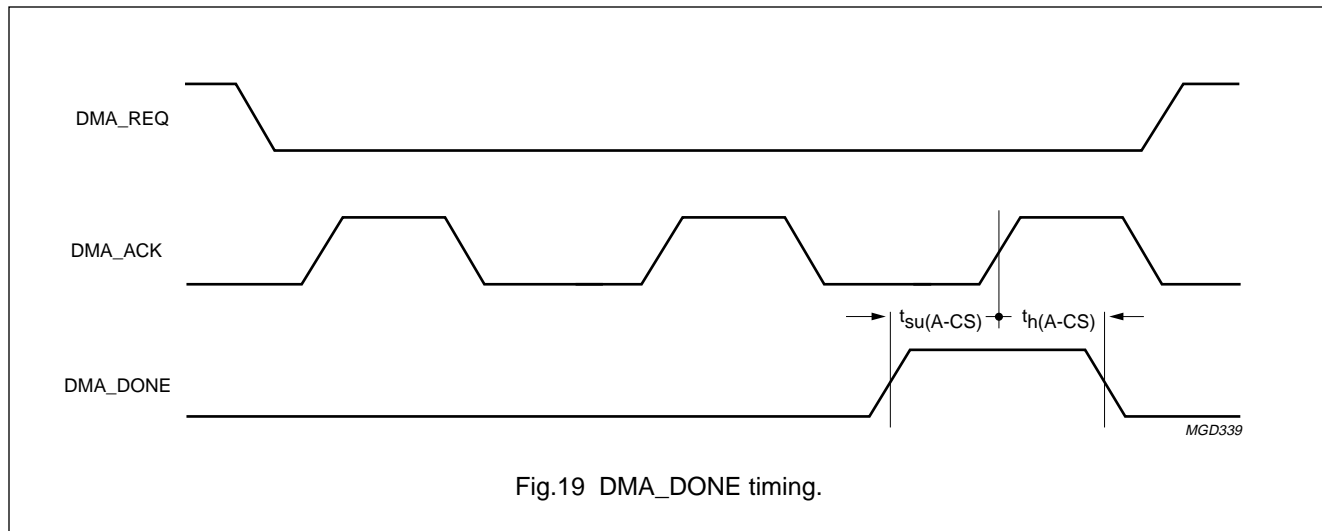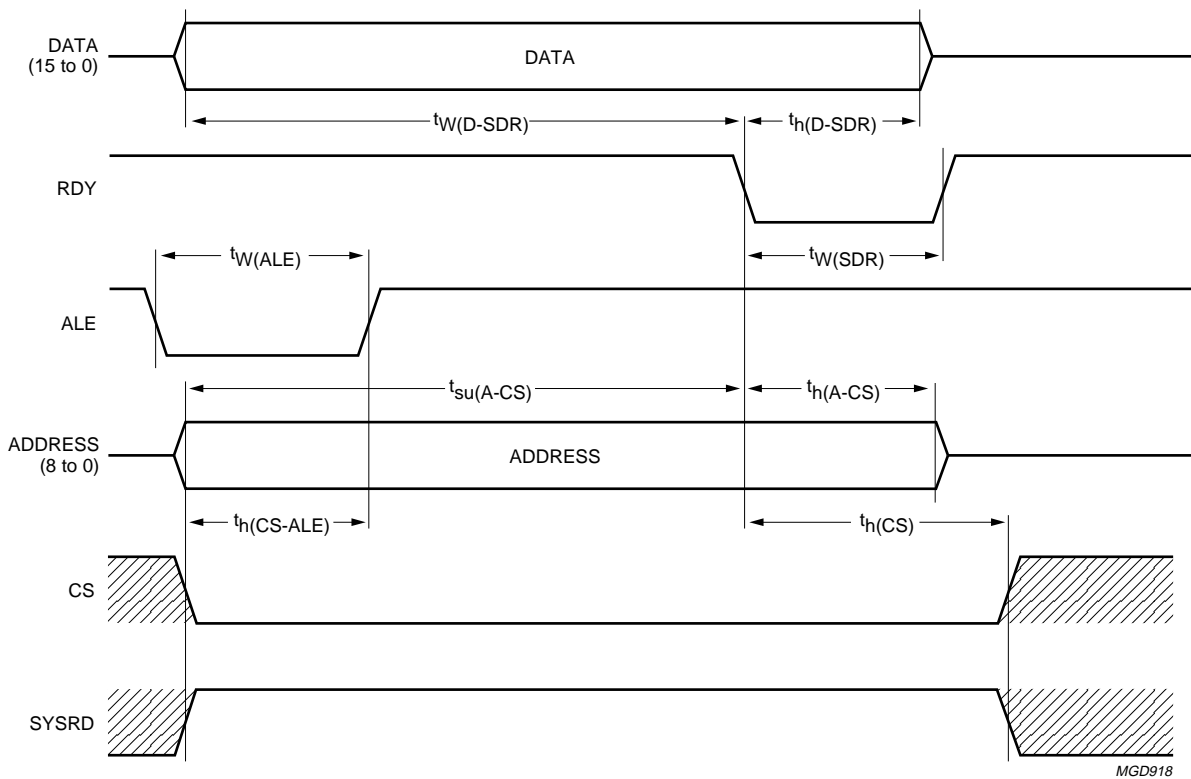# Integrated MPEG2 AVG decoder

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Fig.17 DMA read access.

Fig.18 DMA write access.

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Fig.19 DMA_DONE timing.
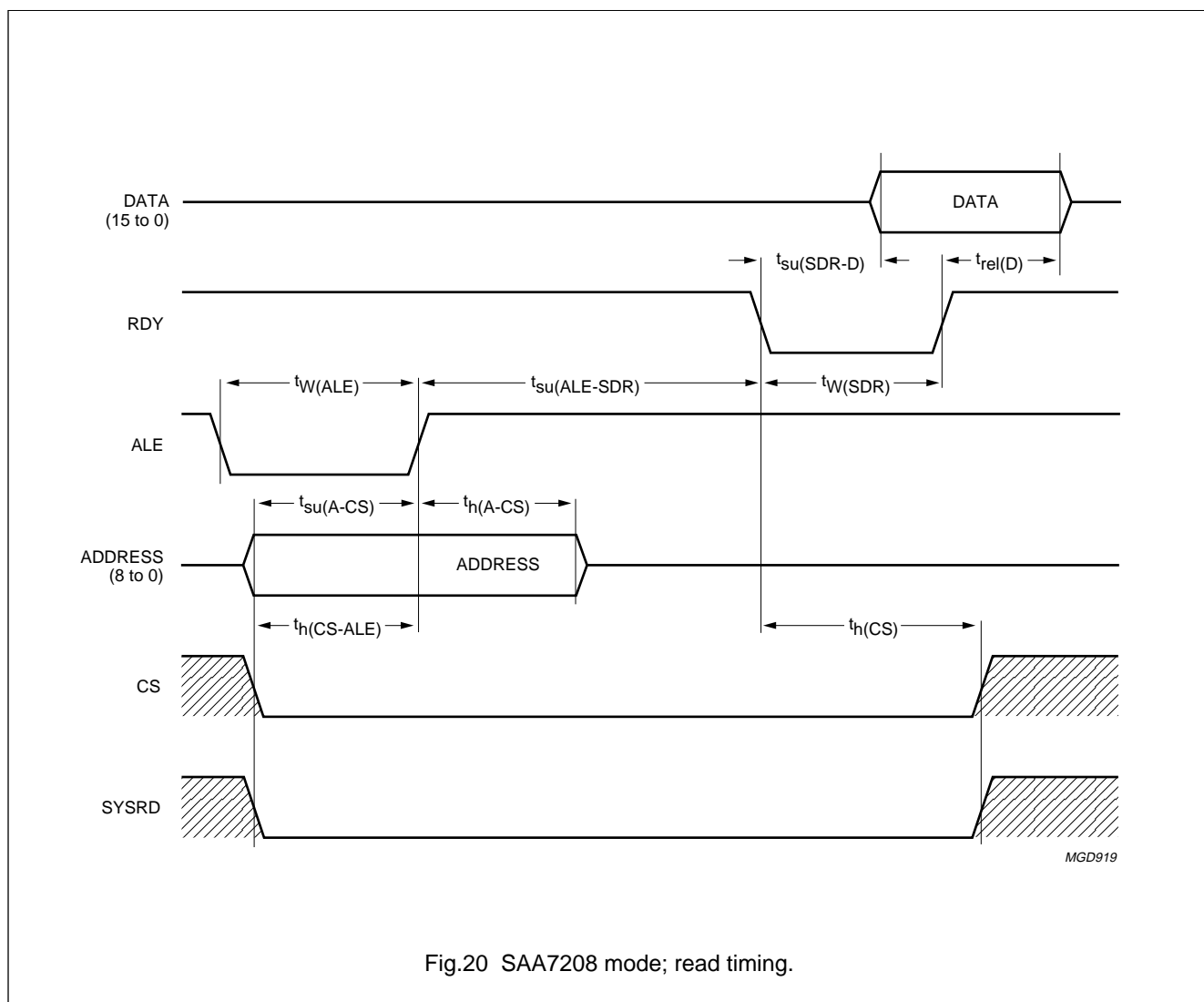
Fig.20 SAA7208 mode; read timing.

Fig.21 SAA7208 mode; write timing.

Fig.22 SAA7208 mode; burst write timing.

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SAA7201
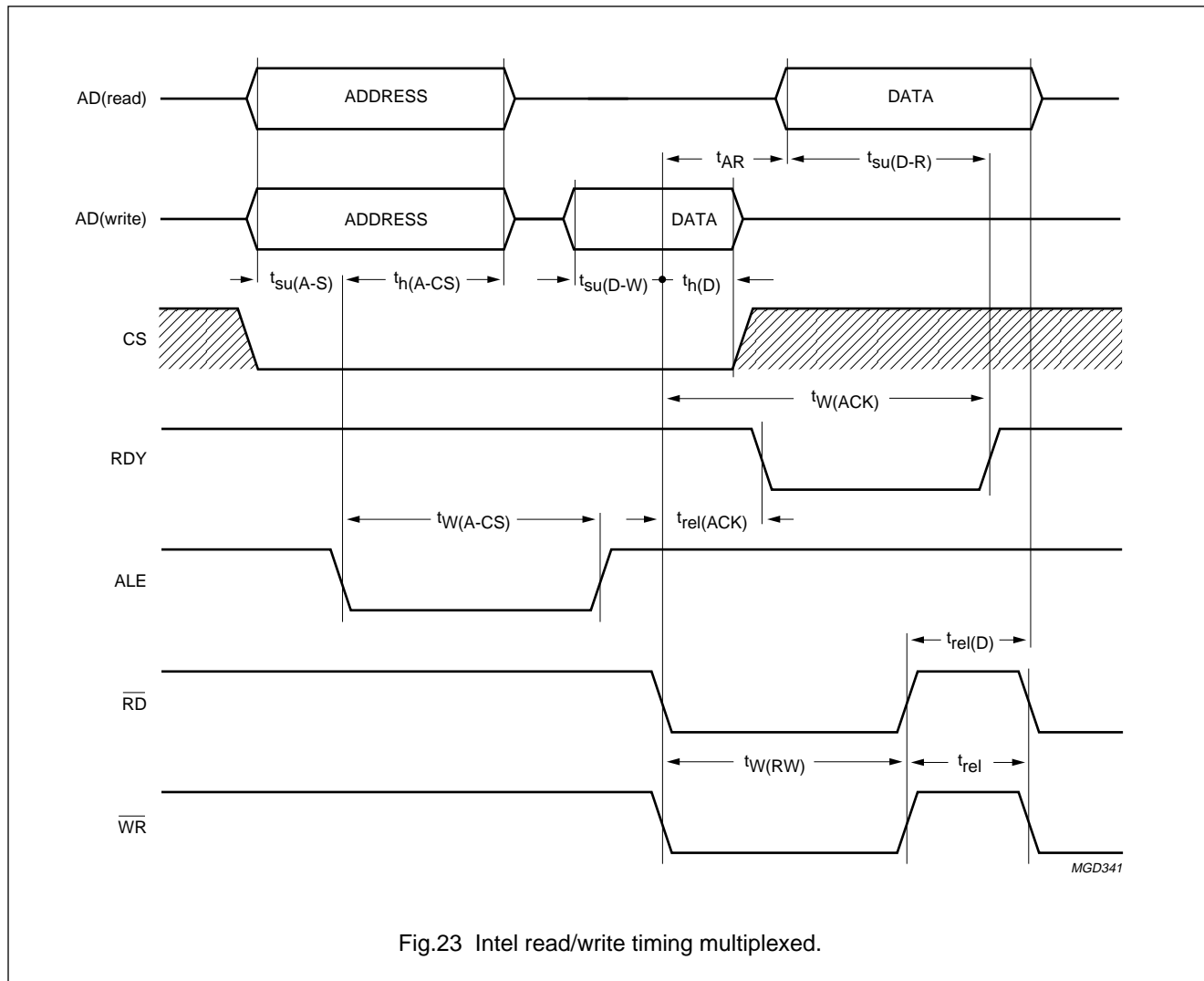
Fig.23 Intel read/write timing multiplexed.

REFERENCES

1. *MPEG ISO/IEC 11172-1 International standard; MPEG-1 systems.*

2. *MPEG ISO/IEC 13818-1 International standard; MPEG-2 systems.*

3. *MPEG ISO/IEC 11172-2 International standard; MPEG-1 Video.*

4. *MPEG ISO/IEC 13818-2 International standard; MPEG-2 Video.*

5. *MPEG ISO/IEC 11172-3 International standard; MPEG-1 Audio.*

6. *MPEG ISO/IEC 13818-3 International standard; MPEG-2 Audio.*

7. *DVB subtitling system; working draft 2.0; TM 1398 rev 2.*

APPLICATION INFORMATION
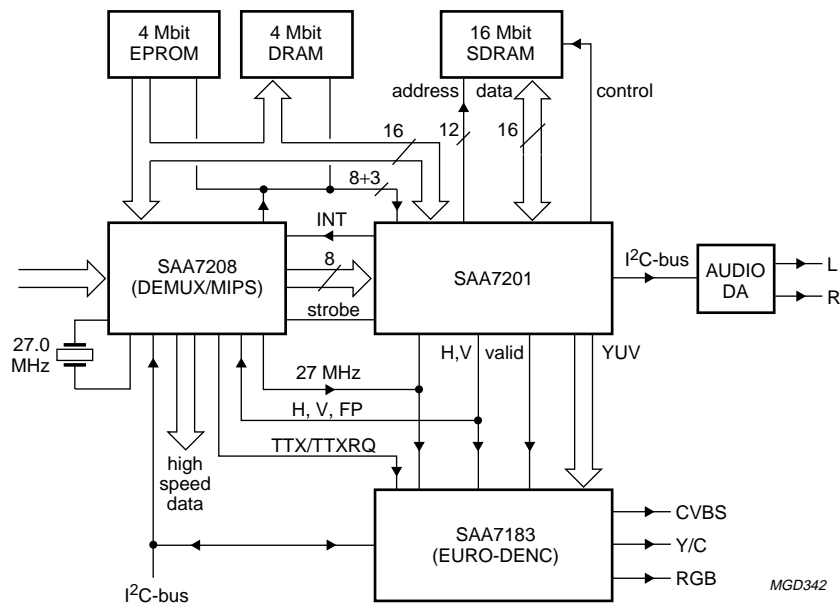
Fig.24 Application diagram.

APPENDIX

Syntax of pixel-data-sub-block

data type	pixel-code-string of N-coded words		end of string
2 bit/pixel	01	1 pixel in colour 1	
	10	1 pixel in colour 2	
0001 0000	11	1 pixel in colour 3	00 00 00
	00 01	1 pixel in colour 0	
	00 00 01	2 pixels in colour 0	
	00 1L LL CC	L pixels (3 to 10) in colour C	
	00 00 10 LL LL CC	L pixels (12 to 27) in colour C	
	00 00 11 LL LL LL LL CC	L pixels (29 to 284) in colour C	
4 bit/pixel	0001	1 pixel in colour 1	
↓	↓	↓	↓
0001 0001	1111	1 pixel in colour 15	0000 0000
	0000 1100	1 pixel in colour 0	
	0000 1101	2 pixels in colour 0	
	0000 0LLL (L>0)	L pixels (3 to 9) in colour 0	
	0000 10LL CCCC	L pixels (4 to 7) in colour C	
	0000 1110 LLLL CCCC	L pixels (9 to 24) in colour C	
	0000 1111 LLLL LL11 CCCC	L pixels (25 to 280) in colour C	
8 bit/pixel	00000001	1 pixel in colour 1	00000000-- --00000000
↓	↓	↓	↓
0001 0010	11111111	1 pixel in colour 255	
	00000000 0LLLLLLL	L pixels (1 to 127) in colour 0	
	00000000 1LLLLLLL CCCCCCCC	L pixels (3 to 127) in colour C	

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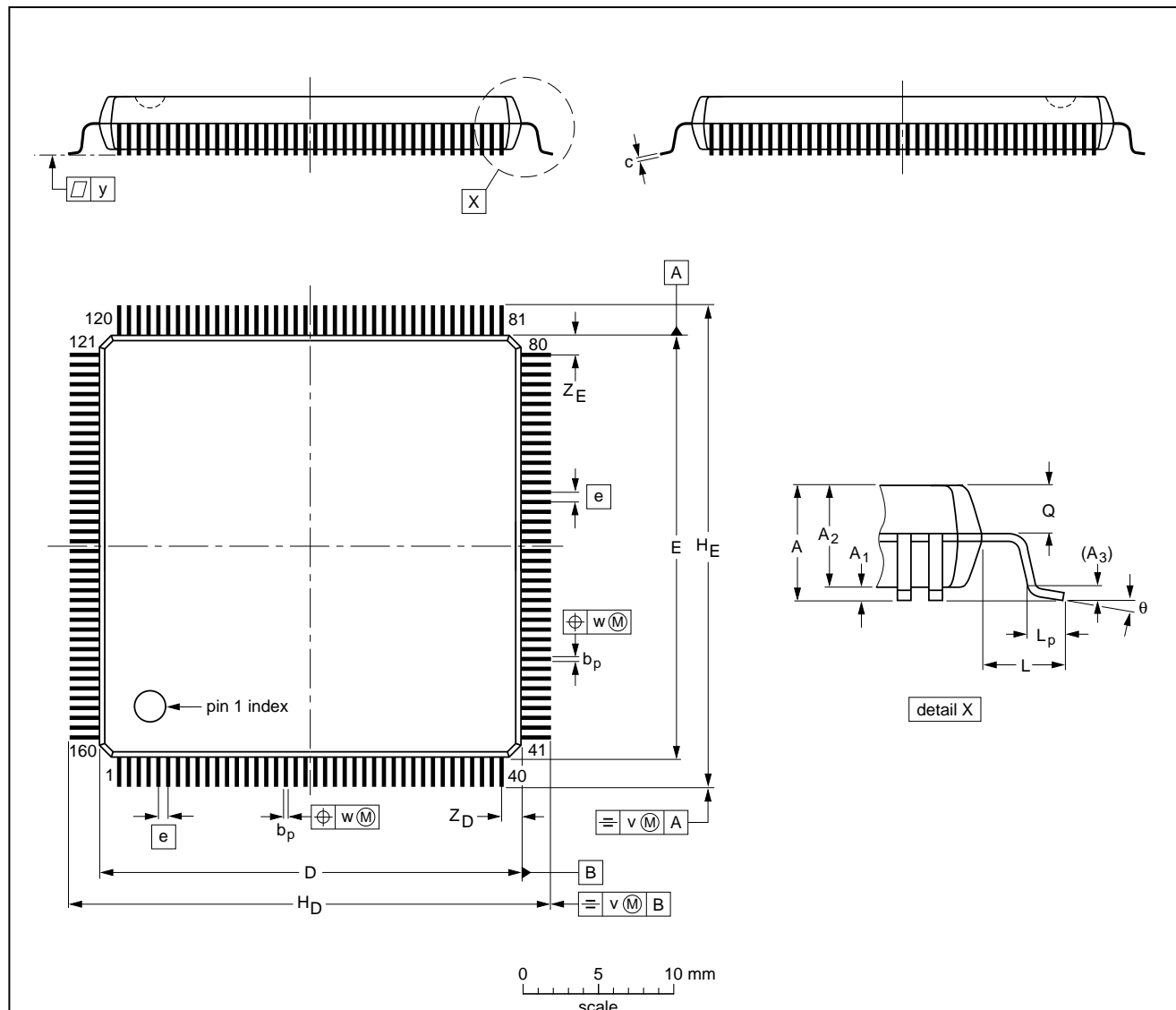
PACKAGE OUTLINE

QFP160: plastic quad flat package;
160 leads (lead length 1.95 mm); body 28 x 28 x 3.4 mm; high stand-off height   **SOT322-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D⁽¹⁾	E⁽¹⁾	e	H_D	H_E	L	Lₚ	Q	v	w	y	Z_D⁽¹⁾	Z_E⁽¹⁾	θ
mm	3.95	0.40 0.25	3.70 3.15	0.25	0.40 0.25	0.23 0.13	28.1 27.9	28.1 27.9	0.65	32.2 31.6	32.2 31.6	1.95	1.1 0.7	1.70 1.55	0.3	0.15	0.1	1.5 1.1	1.5 1.1	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT322-1		MO112DD1				~~93-08-25~~ 95-02-04

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SAA7201

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**

- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Integrated MPEG2 AVG decoder

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

1997 Jan 29

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NOTES

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