Section I. MAX II Device Family Data Sheet

This section provides designers with the data sheet specifications for MAX® II devices. The chapters contain feature definitions of the internal architecture, Joint Test Action Group (JTAG) and in-system programmability (ISP) information, DC operating conditions, AC timing parameters, and ordering information for MAX II devices.

This section includes the following chapters:

Revision History

The table below shows the revision history for Chapters 1 through 6.

Chapter(s)	Date/Version	Changes Made
1	December 2004, v1.2	Updated timing numbers in Table 1.
	June 2004, v1.1	Updated timing numbers in Table 1.
2	December 2004, v1.2	Added a paragraph to page 2-15.
	June 2004, v1.1	Added CFM acronym. Corrected Figure 2-19.
3	December 2004, v1.2	Updated text on pages 3-5 to 3-8.
	June 2004, v1.1	Corrected Figure 3-1. Added CFM acronym.
4	December 2004, v1.2	Added content to Power-Up Characteristics section. Updated Figure 4-5.
	June 2004, v1.1	Corrected Figure 4-2.
5	December 2004, v1.2	Updated timing tables 5-2, 5-4, 5-12, and tables 15-14 through 5-34. Table 5-31 is new.
	June 2004, v1.1	Updated timing tables 5-15 through 5-32.
6	March 2004, v1.0	Initial Release.

Chapter 1. Introduction

MII51001-1.2

Introduction

The MAX® II family of instant-on, non-volatile CPLDs is based on a 0.18-µm, 6-layer-metal-flash process, with densities from 240 to 2,210 logic elements (LEs) (128 to 2,210 equivalent macrocells) and non-volatile storage of 8 Kbits. MAX II devices offer high I/O counts, fast performance, and reliable fitting versus other CPLD architectures. Featuring MultiVolt™ core, a user flash memory (UFM) block, and enhanced in-system programmability (ISP), MAX II devices are designed to reduce cost and power while providing programmable solutions for applications such as bus bridging, I/O expansion, power-on reset (POR) and sequencing control, and device configuration control.

The following shows the main sections of the MAX II CPLD Family Data Sheet:

Features

- Low-cost, low-power CPLD
- Instant-on, non-volatile architecture
- Standby current as low as 2 mA
- Provides fast propagation delay and clock-to-output times
- Provides four global clocks with two clocks available per logic array block (LAB)
- UFM block up to 8 Kbits for non-volatile storage
- MultiVolt core enabling external supply voltages to the device of either 3.3 V/2.5 V or 1.8 V
- MultiVolt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, and 1.5-V logic levels
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors
- Schmitt triggers enabling noise tolerant inputs (programmable per pin)
- Fully compliant with the Peripheral Component Interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 MHz
- Supports hot-socketing
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990
- ISP circuitry compliant with IEEE Std. 1532

Table 1–1 shows MAX II device features.

Table 1–1. MAX II Device Features

Feature	EPM240	EPM570	EPM1270	EPM2210
LEs	240	570	1,270	2,210
Typical Equivalent Macrocells	192	440	980	1,700
Equivalent Macrocell Range	128 to 240	240 to 570	570 to 1,270	1,270 to 2,210
UFM Size (bits)	8,192	8,192	8,192	8,192
Maximum User I/O pins	80	160	212	272
t_{PD1} (ns) *(1)*	4.7	5.5	6.3	7.1
f_{CNT} (MHz) *(2)*	304	304	304	304
t_{SU} (ns)	2.0	1.8	1.8	1.8
t_{CO} (ns)	4.4	4.5	4.6	4.7

Notes to Table 1–1:

(1) t_{PD1} represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.

(2) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.

For more information on equivalent macrocells, refer to the *MAX II Logic Element to Macrocell Conversion Methodology* white paper.

MAX II devices are available in three speed grades: -3, -4, -5 with -3 being the fastest. These speed grades represent overall relative performance, not any specific timing parameter. For propagation delay timing numbers within each speed grade and density, see the chapter on *DC & Switching Characteristics*. Table 1–2 shows MAX II device speed-grade offerings.

Table 1–2. MAX II Speed Grades

Device	Speed Grade		
	-3	-4	-5
EPM240	✓	✓	✓
EPM570	✓	✓	✓
EPM1270	✓	✓	✓
EPM2210	✓	✓	✓

MAX II devices are available in space-saving FineLine BGA® and thin quad flat pack (TQFP) packages (see Tables 1–3 and 1–4). MAX II devices support vertical migration within the same package (e.g., you can migrate between the EPM570, EPM1270, and EPM2210 devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must layout for the largest planned density in a package to provide the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross reference and place all pins for you when given a device migration list.

Table 1–3. MAX II Packages & User I/O Pins

Device	100-Pin TQFP	144-Pin TQFP	256-Pin FineLine BGA	324-Pin FineLine BGA
EPM240	80			
EPM570	76	116	160	
EPM1270		116	212	
EPM2210			204	272

Table 1–4. MAX II TQPF & FineLine BGA Package Sizes				
Package	**100-Pin TQFP**	**144-Pin TQFP**	**256-Pin FineLine BGA**	**324-Pin FineLine BGA**
Pitch (mm)	0.5	0.5	1	1
Area (mm2)	256	484	289	361
Length x width (mm x mm)	16 × 16	22 × 22	17 × 17	19 × 19

MAX II devices have an internal linear voltage regulator which supports external supply voltages of 3.3 V or 2.5 V, regulating the supply down to the internal operating voltage of 1.8 V. MAX IIG devices only accept 1.8 V as an external supply voltage. Table 1–5 shows the external supply voltages supported by the MAX II family.

Table 1–5. MAX II External Supply Voltages		
Devices	**EPM240 EPM570 EPM1270 EPM2210**	**EPM240G EPM570G EPM1270G EPM2210G *(1)***
MultiVolt core external supply voltage (V_{CCINT}) *(2)*	3.3 V, 2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	1.5 V, 1.8 V, 2.5 V, 3.3 V	1.5 V, 1.8 V, 2.5 V, 3.3 V

Notes to Table 1–5:

(1) MAX IIG devices do not have an internal voltage regulator and only accept 1.8 V on their `VCCINT` pins. Contact Altera for availability on these devices.

(2) MAX II devices operate internally at 1.8 V.

Chapter 2. MAX II Architecture

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Functional Description

MAX® II devices contain a two-dimensional row- and column-based architecture to implement custom logic. Column and row interconnect provide signal interconnects between the logic array blocks (LABs).

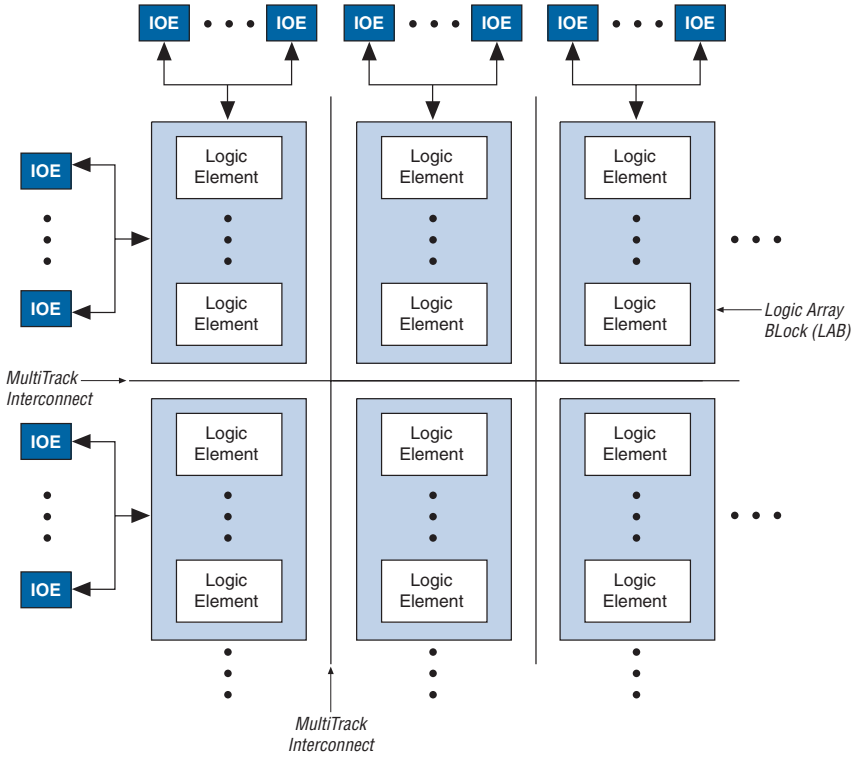
The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. The MultiTrack™ interconnect provides fast granular timing delays between LABs. The fast routing between LEs provides minimum timing delay for added levels of logic versus globally routed interconnect structures.

The MAX II device I/O pins are fed by an I/O element (IOE) located at the ends of LAB rows and columns around the periphery of the device. Each IOE contains a bidirectional I/O buffer with several advanced features. I/O pins support Schmitt trigger inputs and various single-ended standards, such as 33-MHz, 32-bit PCI and LVTTL.

MAX II devices provide a global clock network. The global clock network consists of four global clock lines that drive throughout the entire device, providing clocks for all resources within the device. The global clock lines can also be used for control signals such as clear, preset, or output enable.

Figure 2–1 shows a functional block diagram of the MAX II device.

Figure 2–1. MAX II Device Block Diagram



Each MAX II device contains a flash memory block within its floorplan. On the EPM240 device, this block is located on the left side of the device. For the EPM570, EPM1270, and EPM2210 devices, the flash memory block is located on the bottom-left area of the device. The majority of this flash memory storage is partitioned as the dedicated configuration flash memory (CFM) block. The CFM block provides the non-volatile storage for all of the SRAM configuration information. The CFM automatically downloads and configures the logic and I/O at power-up providing instant-on operation.

See *Hot Socketing & Power-On Reset in MAX II Devices* for more information on configuration upon power-up.

A portion of the flash memory within the MAX II device is partitioned into a small block for user data. This user flash memory (UFM) block provides 8,192 bits of general-purpose user storage. The UFM provides programmable port connections to the logic array for reading and for writing. There are three LAB rows adjacent to this block, with column numbers varying by device.

Table 2–1 shows the number of LAB rows and columns in each device as well as the number of LAB rows and columns adjacent to the flash memory area in the EPM570, EPM1270, and EPM2210 devices. The long LAB rows are full LAB rows that extend from one side of row I/O blocks to the other. The short LAB rows are adjacent to the UFM block; their length is shown as width in LAB columns.

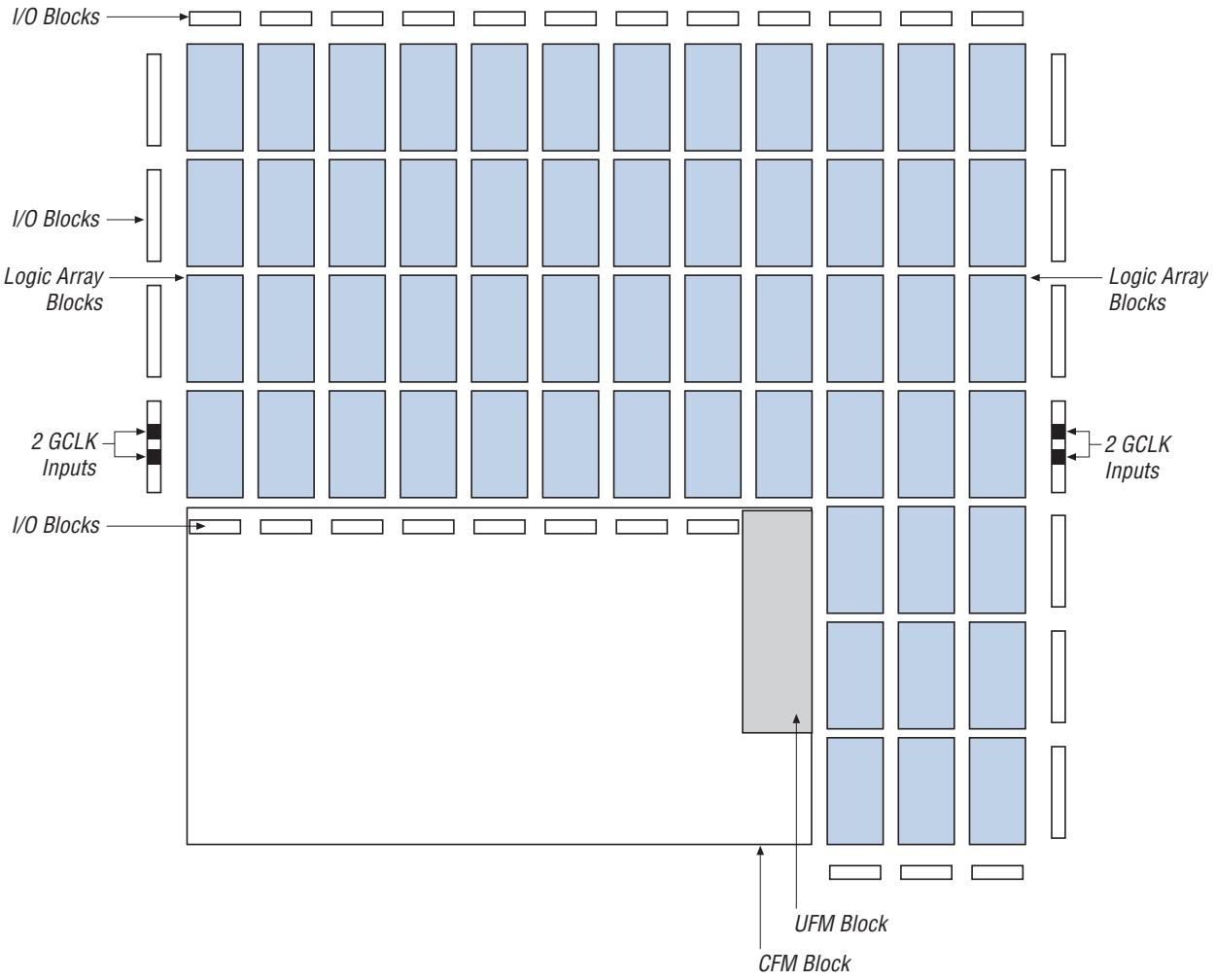
Table 2–1. MAX II Device Resources

Devices	UFM Blocks	LAB Columns	LAB Rows		Total LABs
			Long LAB Rows	Short LAB Rows (Width) *(1)*	
EPM240	1	6	4	-	24
EPM570	1	12	4	3 (3)	57
EPM1270	1	16	7	3 (5)	127
EPM2210	1	20	10	3 (7)	221

Note to Table 2–1:
(1) The width is the number of LAB columns in length.

Figure 2–2 shows a floorplan of a MAX II device.

Figure 2–2. MAX II Device Floorplan *Note (1)*



Note to Figure 2–2:

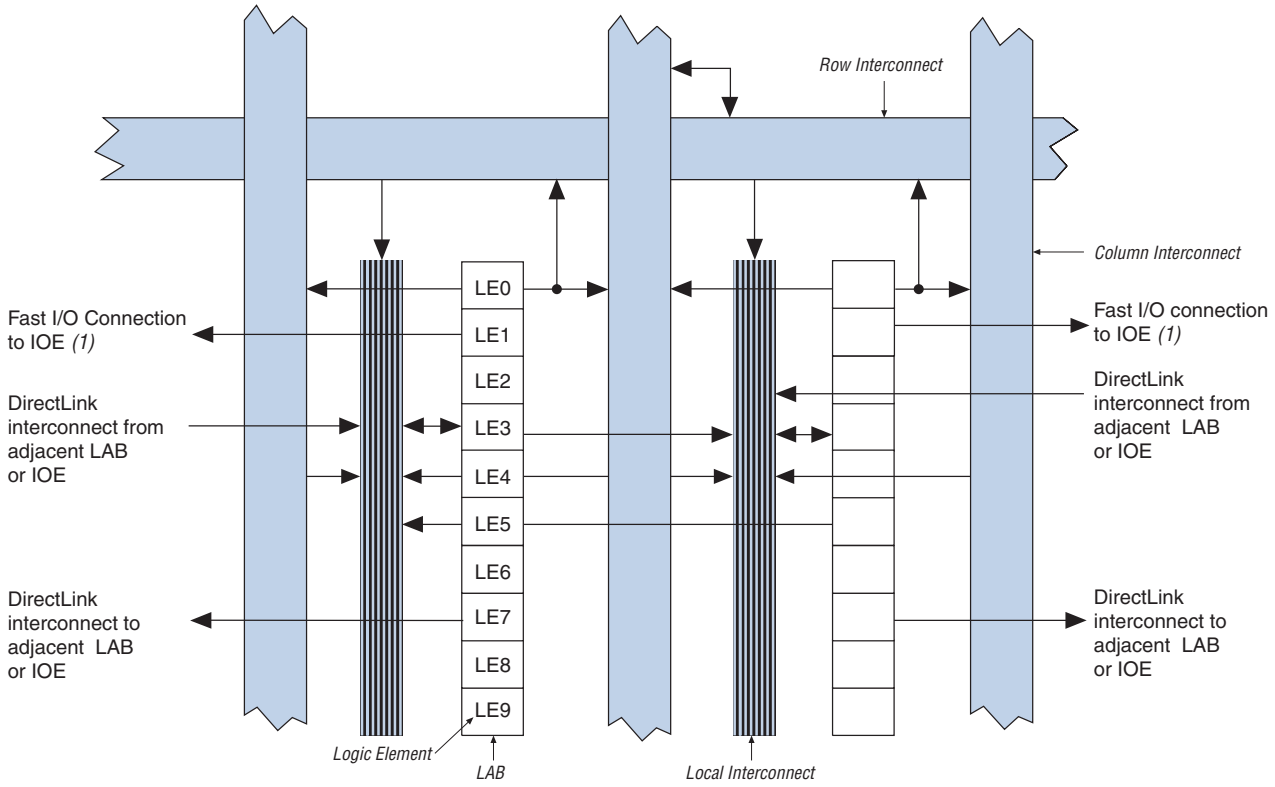
(1) The device shown is an EPM570 device. EPM1270 and EPM2210 devices have a similar floorplan with more LABs. For the EPM240 devices, the CFM and UFM block is rotated left 90 degrees covering the left side of the device.

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, a look-up table (LUT) chain, and register chain connection lines. There are 26 possible unique inputs into an LAB, with an additional 10 local feedback input lines fed by LE outputs in the same LAB. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II software places associated logic

within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–3 shows the MAX II LAB.

Figure 2–3. MAX II LAB Structure

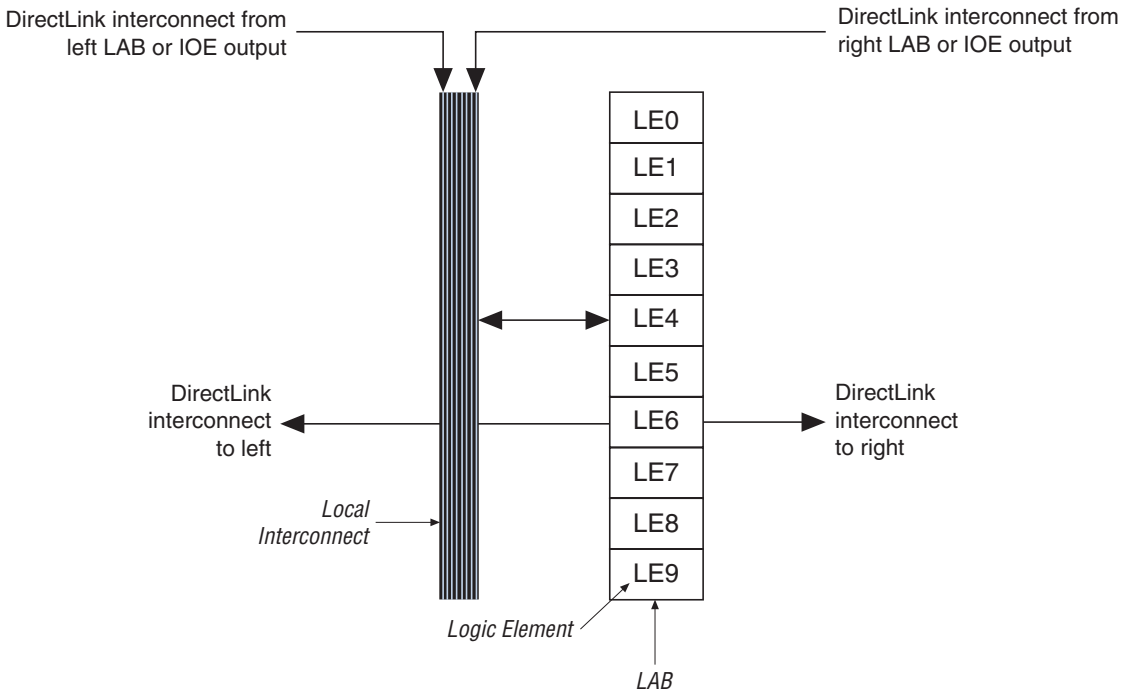


Note to Figure 2–3:
(1) Only from LABs adjacent to IOEs.

LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, from the left and right can also drive an LAB's local interconnect through the DirectLink connection. The DirectLink connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and DirectLink interconnects. Figure 2–4 shows the DirectLink connection.

Figure 2–4. DirectLink Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, a synchronous clear, an asynchronous preset/load, a synchronous load, and add/subtract control signals, providing a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

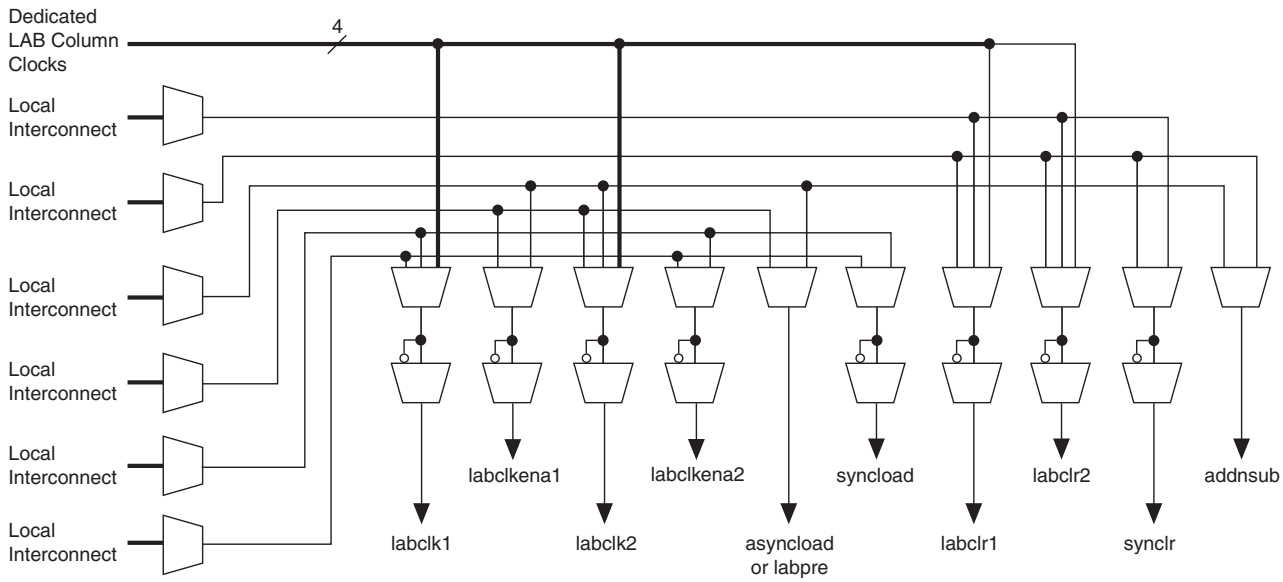
Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. De-asserting the clock enable signal turns off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high.

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB column clocks [3..0], driven by the global clock network, and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect structure drives the LAB local interconnect for non-global control signal generation. The MultiTrack interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–5 shows the LAB control signal generation circuit.

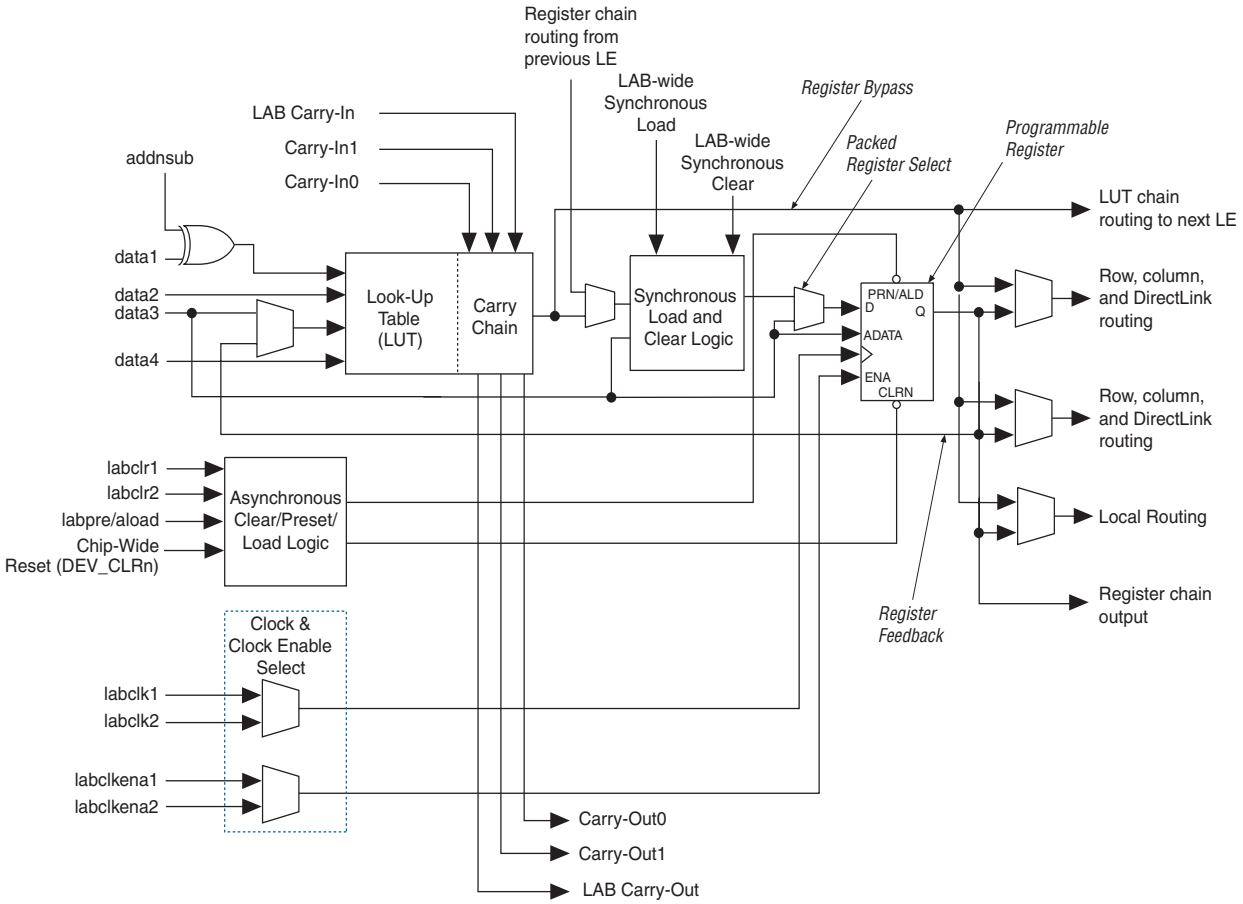
Figure 2–5. LAB-Wide Control Signals



Logic Elements

The smallest unit of logic in the MAX II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and DirectLink interconnects. See Figure 2–6.

Figure 2–6. MAX II LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any LE can drive the register's clock and clear control signals. Either general-purpose I/O pins or LEs can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the `data3` input of the LE. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and DirectLink routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This register packing feature improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into

the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain & Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. See "MultiTrack Interconnect" on page 2–15 for more information on LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either A + B or A – B. The LUT computes addition; subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in to 1, which adds one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The MAX II LE can operate in one of the following modes:

- Normal mode
- Dynamic arithmetic mode

Each mode uses LE resources differently. In each mode, eight available inputs to the LE, the four data inputs from the LAB local interconnect, `carry-in0` and `carry-in1` from the previous LE, the LAB carry-in from the previous carry-chain LAB, and the register chain connection are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous

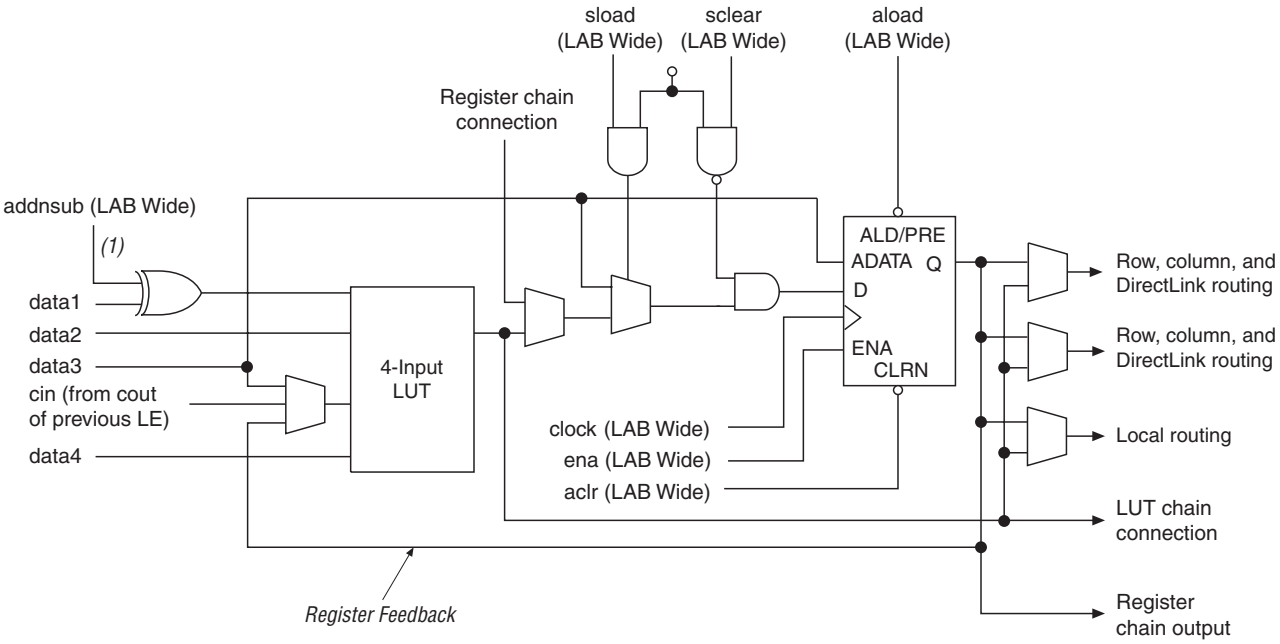
preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–7). The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinational output directly to the next LE in the LAB. Asynchronous load data for the register comes from the `data3` input of the LE. LEs in normal mode support packed registers.

Figure 2–7. LE in Normal Mode



Note to Figure 2–7:
(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry select circuitry. As shown in Figure 2–8, the LAB carry-in signal selects either the `carry-in0` or `carry-in1` chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinational or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

```
data1 + data2 + carry in0
```

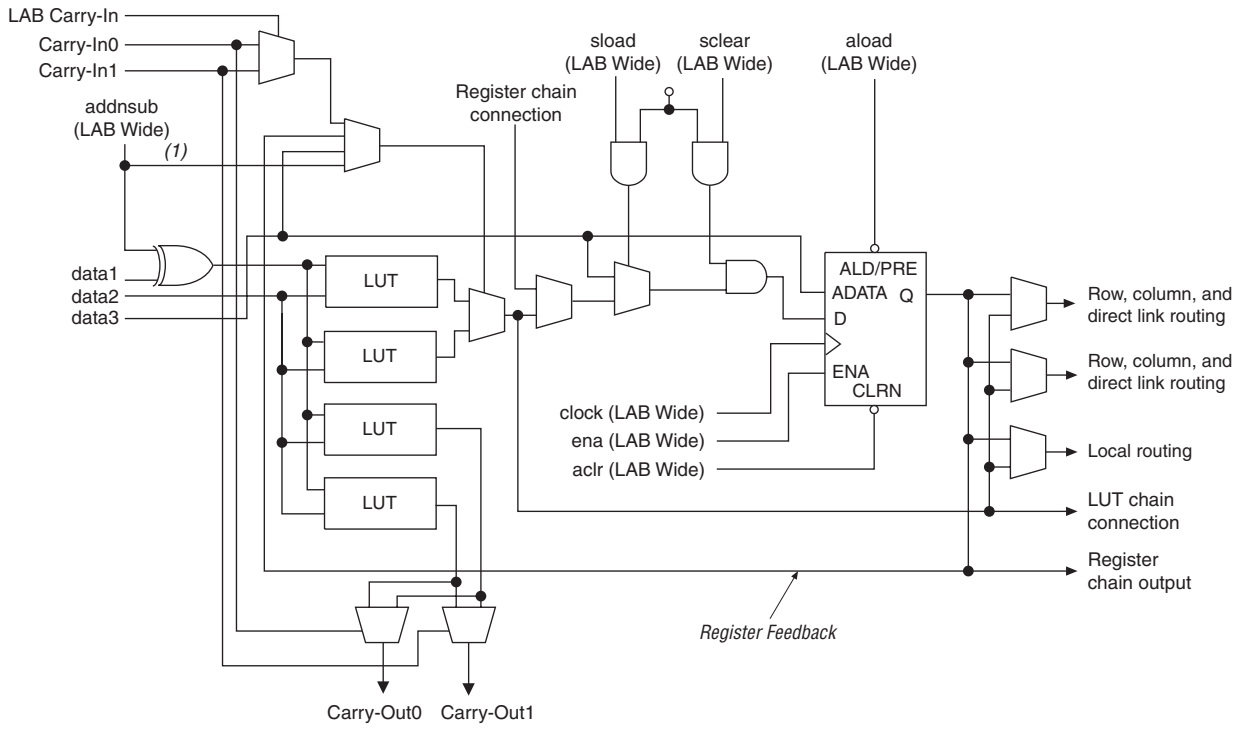
or

```
data1 + data2 + carry-in1
```

The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals: one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry select for the `carry-out0` output and `carry-in1` acts as the carry select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The `addnsub` LAB-wide signal controls whether the LE acts as an adder or subtractor.

Figure 2–8. LE in Dynamic Arithmetic Mode



Note to Figure 2–8:
(1) The `addnsub` signal is tied to the carry input for the first LE of a carry chain only.

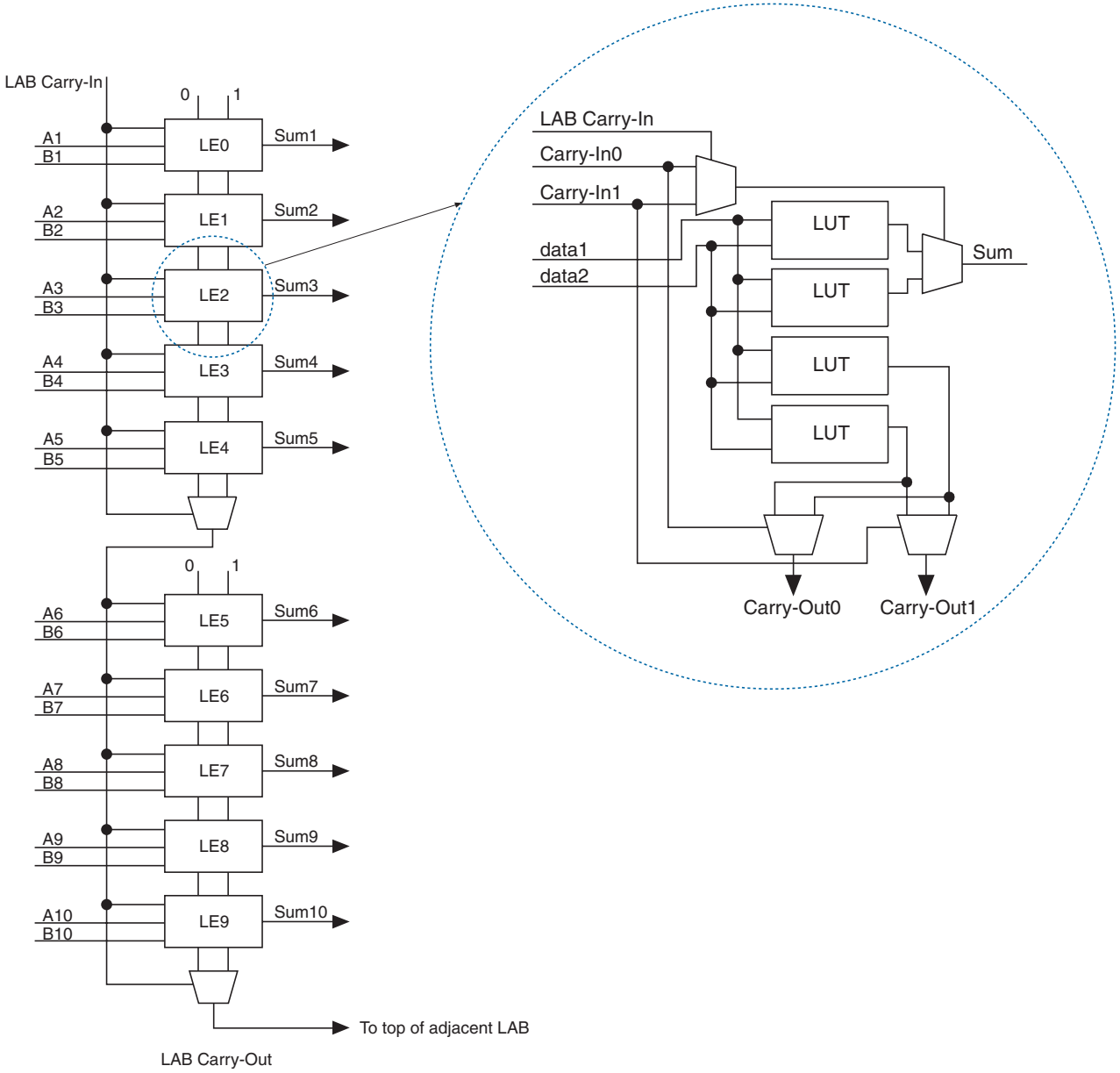
Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in dynamic arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 0 and carry-in of 1 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delays between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the MAX II architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 2–9 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry-in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, `carry-in0` or `carry-in1`, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

Figure 2–9. Carry Select Chain



The Quartus II software automatically creates carry chain logic during design processing, or the designer can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II software creates carry chains longer than 10 LEs by linking adjacent LABs within the same row together automatically. A carry chain can extend horizontally up to one full LAB row, but they do not extend between LAB rows.

Clear & Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. MAX II devices support simultaneous preset/asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, MAX II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals and uses its own dedicated routing resources (i.e., it does not use any of the four global resources). Driving this signal low before or during power-up prevents user mode from releasing clears within the design. This allows you to control when clear is released on a device that has just been powered-up. If not set for its chip-wide reset function, the DEV_CLRn pin is a regular I/O pin.

Upon power-up, each register in a MAX II device may be set to either a high or low state. This power-up state is specified at design entry. By default, all registers are set to power up low.

MultiTrack Interconnect

In the MAX II architecture, connections between LEs, the UFM, and device I/O pins are provided by the MultiTrack interconnect structure. The MultiTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

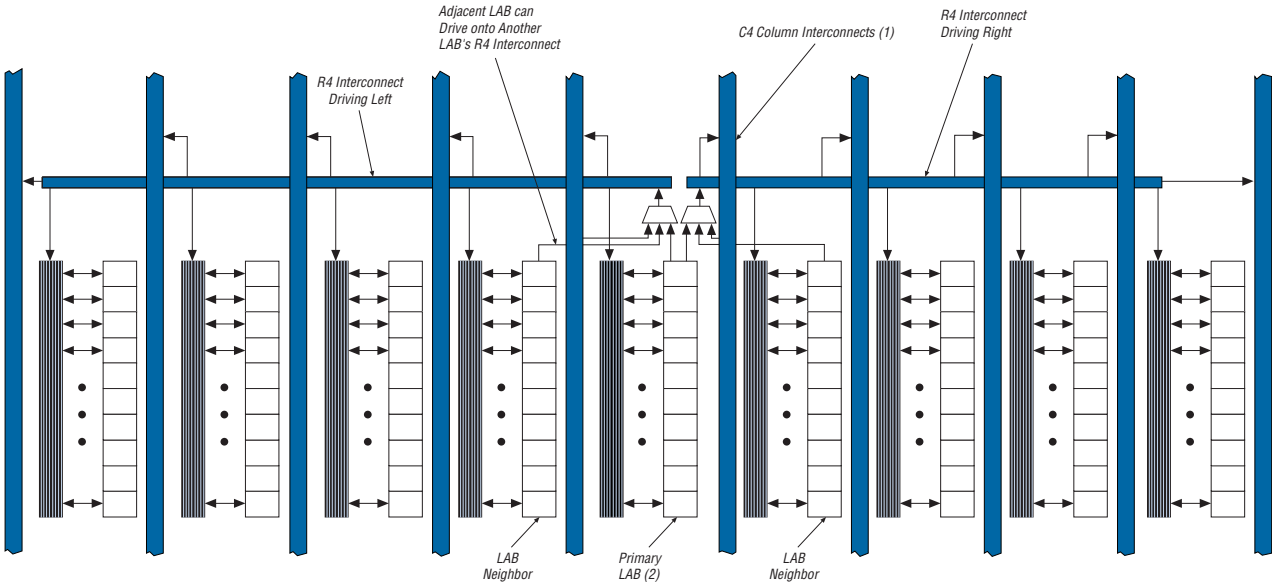
The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and short delays between logic levels instead of large delays associated with global or long routing lines. Dedicated row interconnects route signals to and from LABs within the same row. These row resources include:

- DirectLink interconnects between LABs
- R4 interconnects traversing four LABs to the right or left

The DirectLink interconnect allows an LAB to drive into the local interconnect of its left and right neighbors. The DirectLink interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs and are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–10 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by row IOEs. For LAB interfacing, a primary LAB or horizontal LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 interconnects for connections from one row to another.

Figure 2–10. R4 Interconnect Connections



Notes to Figure 2–10:

(1) C4 interconnects can drive R4 interconnects.

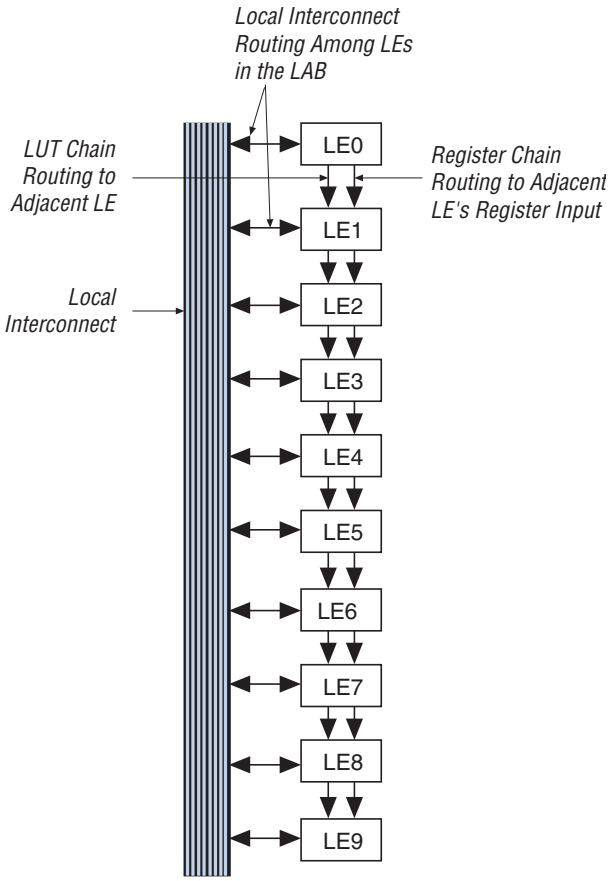
(2) This pattern is repeated for every LAB in the LAB row.

The column interconnect operates similarly to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs and row and column IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four LABs in an up and down direction

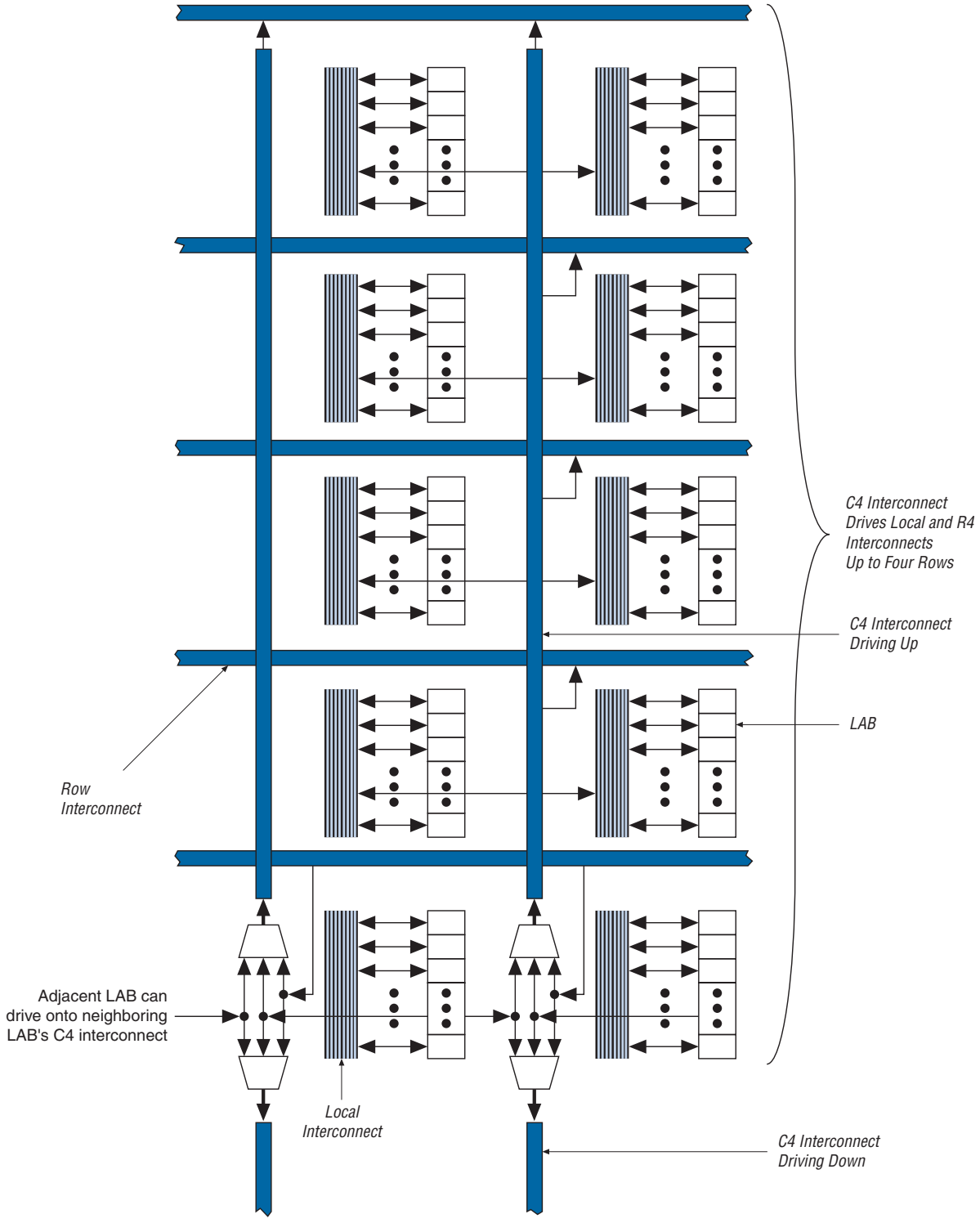
MAX II devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinational output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–11 shows the LUT chain and register chain interconnects.

Figure 2–11. LUT Chain & Register Chain Interconnects



The C4 interconnects span four LABs up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–12 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by column and row IOEs. For LAB interconnection, a primary LAB or its vertical LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–12. C4 Interconnect Connections *Note (1)*



Note to Figure 2–12:

(1) Each C4 interconnect can drive either up or down four rows.

The UFM block communicates with the logic array similar to LAB-to-LAB interfaces. The UFM block connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. This block also has DirectLink interconnects for fast connections to and from a neighboring LAB. For more information on the UFM interface to the logic array, see "User Flash Memory Block" on page 2–23.

Table 2–2 shows the MAX II device's routing scheme.

Table 2–2. MAX II Device Routing Scheme

Source	Destination										
	LUT Chain	Register Chain	Local (1)	DirectLink (1)	R4 (1)	C4 (1)	LE	UFM Block	Column IOE	Row IOE	Fast I/O (1)
LUT Chain							✓				
Register Chain							✓				
Local Interconnect							✓	✓	✓	✓	
DirectLink Interconnect			✓								
R4 Interconnect			✓		✓	✓					
C4 Interconnect			✓		✓	✓					
LE	✓	✓	✓	✓	✓	✓			✓	✓	✓
UFM Block			✓	✓	✓	✓					
Column IOE						✓					
Row IOE				✓	✓	✓					

Note to Table 2–2:
(1) These categories are interconnects.

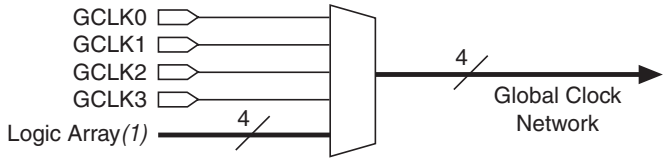
Global Signals

Each MAX II device has four dual-purpose dedicated clock pins (`GCLK[3..0]`, two pins on the left side and two pins on the right side) that drive the global clock network for clocking, as shown in Figure 2–13. These four pins can also be used as general-purpose I/O if they are not used to drive the global clock network.

The four global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, LAB local interconnect, IOEs, and the UFM block. The global clock lines can also be used for global

control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, or protocol control signals such as TRDY and IRDY for PCI. Internal logic can drive the global clock network for internally- generated global clocks and control signals. Figure 2–13 shows the various sources that drive the global clock network.

Figure 2–13. Global Clock Generation

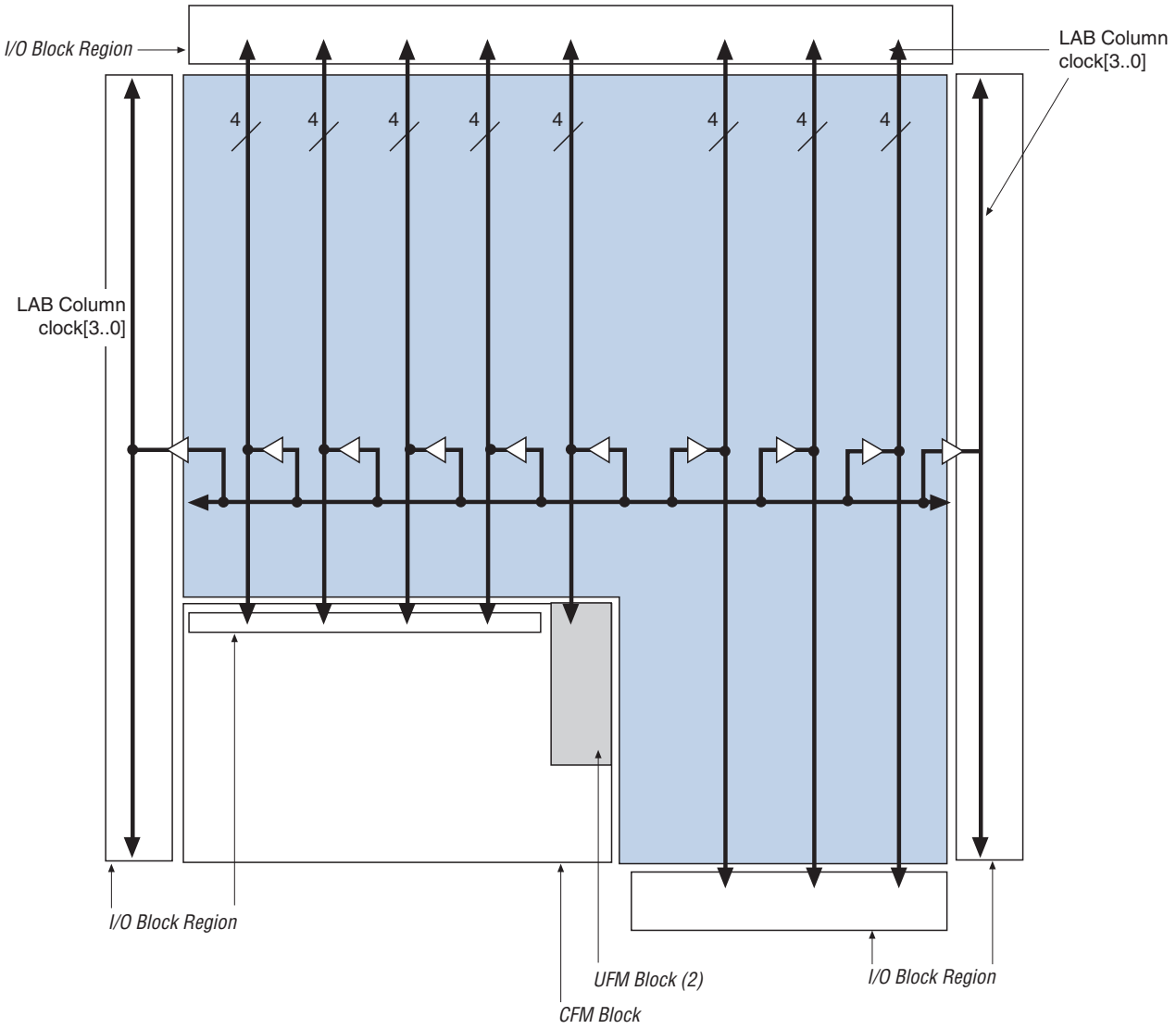


Note to Figure 2–13:

(1) Any I/O pin can use a MultiTrack interconnect to route as a logic array-generated global clock signal.

The global clock network drives to individual LAB column signals, LAB column clocks [3..0], that span an entire LAB column from the top to bottom of the device. Unused global clocks or control signals in a LAB column are turned off at the LAB column clock buffers shown in Figure 2–14. The LAB column clocks [3..0] are multiplexed down to two LAB clock signals and one LAB clear signal. Other control signal types route from the global clock network into the LAB local interconnect. See "LAB Control Signals" on page 2–6 for more information.

Figure 2–14. Global Clock Network *Note (1)*



Notes to Figure 2–14:

(1) LAB column clocks in I/O block regions provide high fan-out output enable signals.

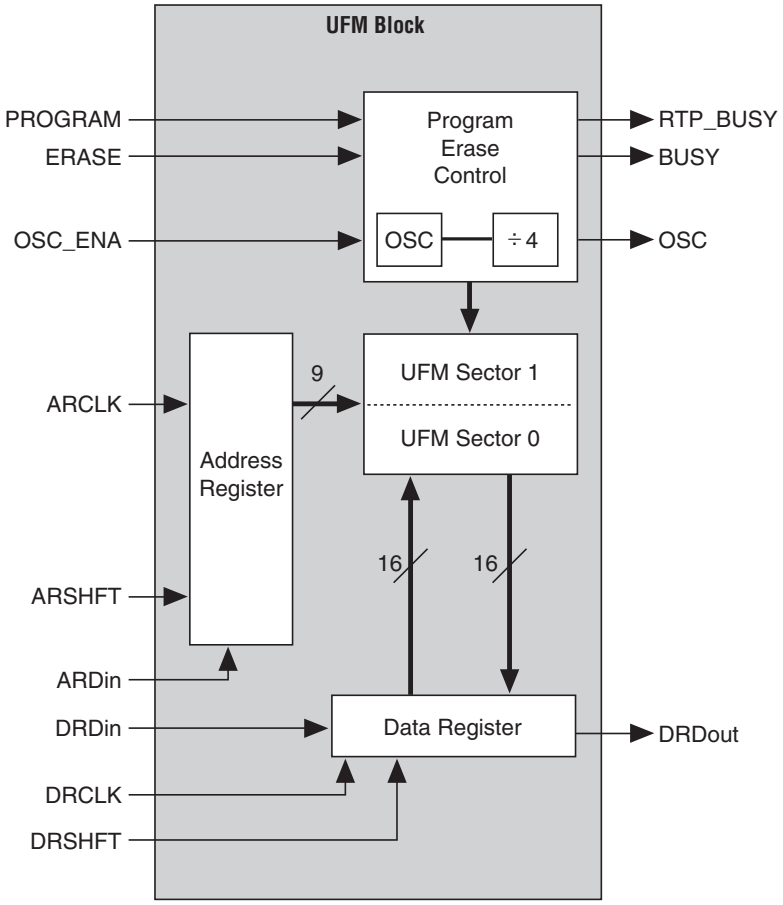
(2) LAB column clocks drive to the UFM block.

User Flash Memory Block

MAX II devices feature a single UFM block, which can be used like a serial EEPROM for storing non-volatile information up to 8,192 bits. The UFM block connects to the logic array through the MultiTrack interconnect, allowing any LE to interface to the UFM block. Figure 2–15 shows the UFM block and interface signals. The logic array is used to create customer interface or protocol logic to interface the UFM block data outside of the device. The UFM block offers the following features:

- Non-volatile storage up to 16-bit wide and 8,192 total bits
- Two sectors for partitioned sector erase
- Built-in internal oscillator that optionally drives logic array
- Program, erase, and busy signals
- Auto-increment addressing
- Serial interface to logic array with programmable interface

Figure 2–15. UFM Block & Interface Signals



UFM Storage

Each device stores up to 8,192 bits of data in the UFM block. Table 2–3 shows the data size, sector, and address sizes for the UFM block.

Table 2–3. UFM Array Size

Device	Total Bits	Sectors	Address Bits	Data Width
EPM240 EPM570 EPM1270 EPM2210	8,192	2 (4,096 bits/sector)	9	16

There are 512 locations with 9-bit addressing ranging from `000h` to `1FFh`. Sector 0 address space is `000h` to `0FFh` and Sector 1 address space is from `100h` to `1FFh`. The data width is up to 16 bits of data. The Quartus II software automatically creates logic to accommodate smaller read or program data widths. Erasure of the UFM involves individual sector erasing (i.e., one erase of sector 0 and one erase of sector 1 is required to erase the entire UFM block). Since sector erase is required before a program or write, having two sectors enables a sector size of data to be left untouched while the other sector is erased and programmed with new data.

Internal Oscillator

As shown in Figure 2–15, the dedicated circuitry within the UFM block contains an oscillator. The dedicated circuitry uses this internally for its read and program operations. This oscillator's divide by 4 output can be driven out of the UFM block to the logic array for interface logic clock source or for general-purpose logic clocking. The `OSC` output signal frequency ranges from 3.3 to 5.5 MHz (preliminary), and its exact frequency of operation is not programmable.

Program, Erase & Busy Signals

The UFM block's dedicated circuitry automatically generates the necessary internal program and erase algorithm once the `PROGRAM` or `ERASE` input signals have been asserted. The `PROGRAM` or `ERASE` signal must be asserted until the `busy` signal deasserts, indicating the UFM internal program or erase operation has completed. The UFM block also supports JTAG as the interface for programming and/or reading.

For more information on programming and erasing the UFM block, see the chapter on *Using User Flash Memory in MAX II Devices*.

Auto-Increment Addressing

The UFM block supports standard read or stream read operations. The stream read is supported with a auto-increment address feature. De-asserting the ARSHIFT signal while clocking the ARCLK signal increments the address register value to read consecutive locations from the UFM array.

Serial Interface

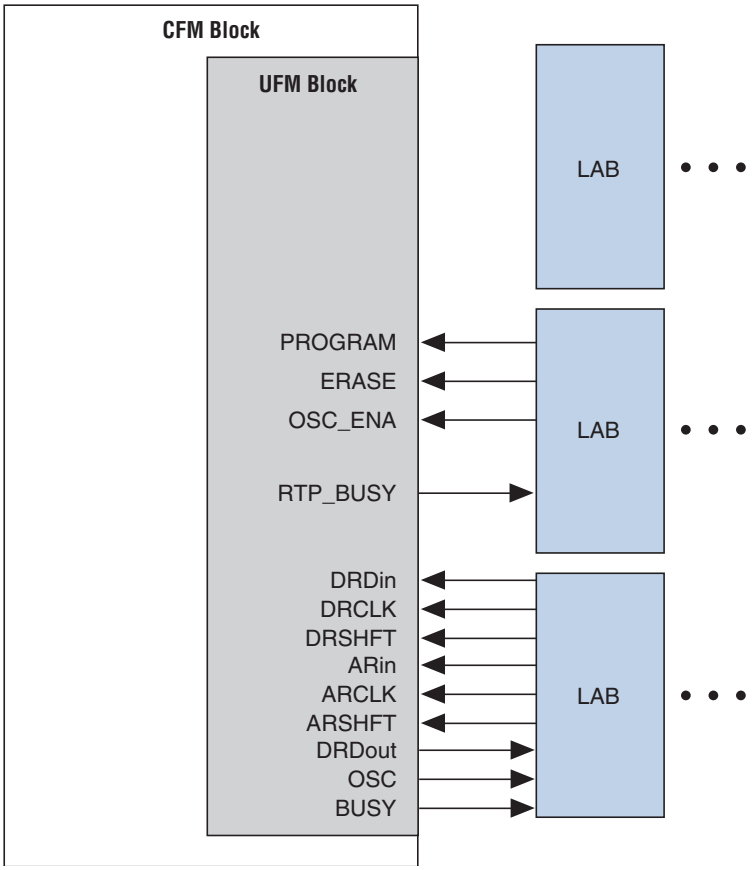
The UFM block supports a serial interface with serial address and data signals. The internal shift registers within the UFM block for address and data are 9 bits and 16 bits wide, respectively. The Quartus II software automatically generates interface logic in LEs for a parallel address and data interface to the UFM block. Other standard protocol interfaces such as SPI are also automatically generated in LE logic by the Quartus II software.

For more information on the UFM interface signals and the Quartus II LE-based alternate interfaces, see *Using User Flash Memory in MAX II Devices*.

UFM Block to Logic Array Interface

The UFM block is a small partition of the flash memory which contains the CFM block as shown in Figures 2–1 and 2–2. The UFM block for the EPM240 device is located on the left side of the device adjacent to the left most LAB column. The UFM block for the EPM570, EPM1270, and EPM2210 devices is located on the bottom left portion of the device. The UFM input and output signals interface to all types of interconnects (R4 interconnect, C4 interconnect, and DirectLink interconnect to/from adjacent LAB rows). The UFM signals can also be driven from global clocks, GCLK[3..0]. The interface region for the EPM240 device is shown in Figure 2–16. The interface regions for EPM570, EPM1270, and EPM2210 devices are shown in Figure 2–17.

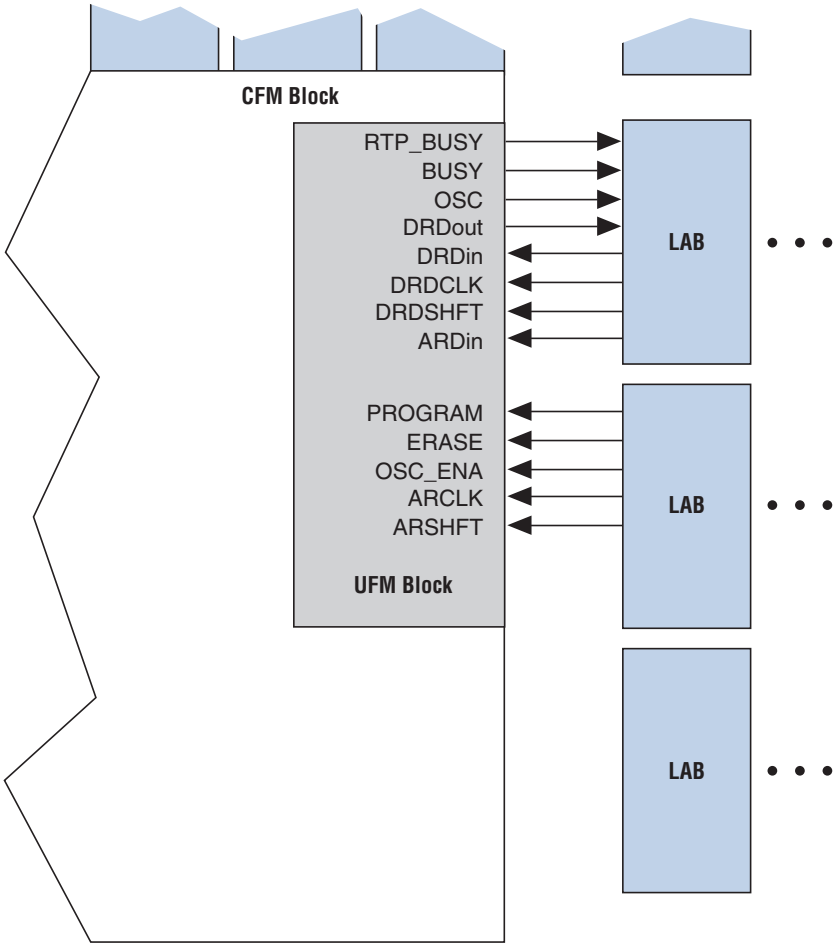
Figure 2–16. EPM240 UFM Block LAB Row Interface *Note (1)*



Note to Figure 2–16:

(1) The UFM block inputs and outputs can drive to/from all types of interconnects, not only DirectLink interconnects from adjacent row LABs.

Figure 2–17. EPM570, EPM1270 & EPM2210 UFM Block LAB Row Interface

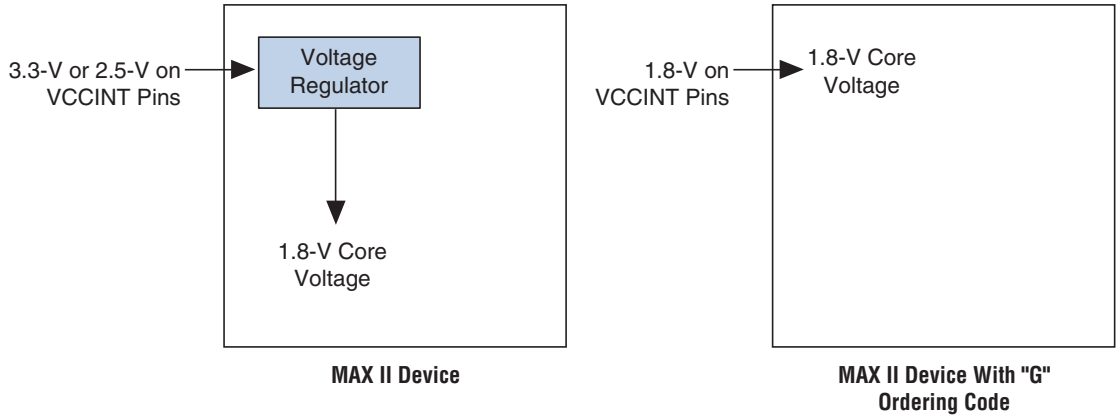


MultiVolt Core

The MAX II architecture supports the MultiVolt™ core feature, which allows MAX II devices to support multiple V_{CC} levels on the V_{CCINT} supply. An internal linear voltage regulator provides the necessary 1.8-V internal voltage supply to the device. The voltage regulator supports 3.3-V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage to the device, as shown in Figure 2–18. The voltage regulator is not guaranteed for voltages that are between the maximum recommended 2.5-V operating voltage and the minimum recommended 3.3-V operating voltage.

For external 1.8-V supplies, MAX IIG devices are required. The voltage regulator on these devices is bypassed to support the 1.8-V V_{CC} external supply path to the 1.8-V internal supply. Contact Altera for latest information regarding MAX IIG devices.

Figure 2–18. MultiVolt Core Feature in MAX II Devices



I/O Structure

IOEs support many features, including:

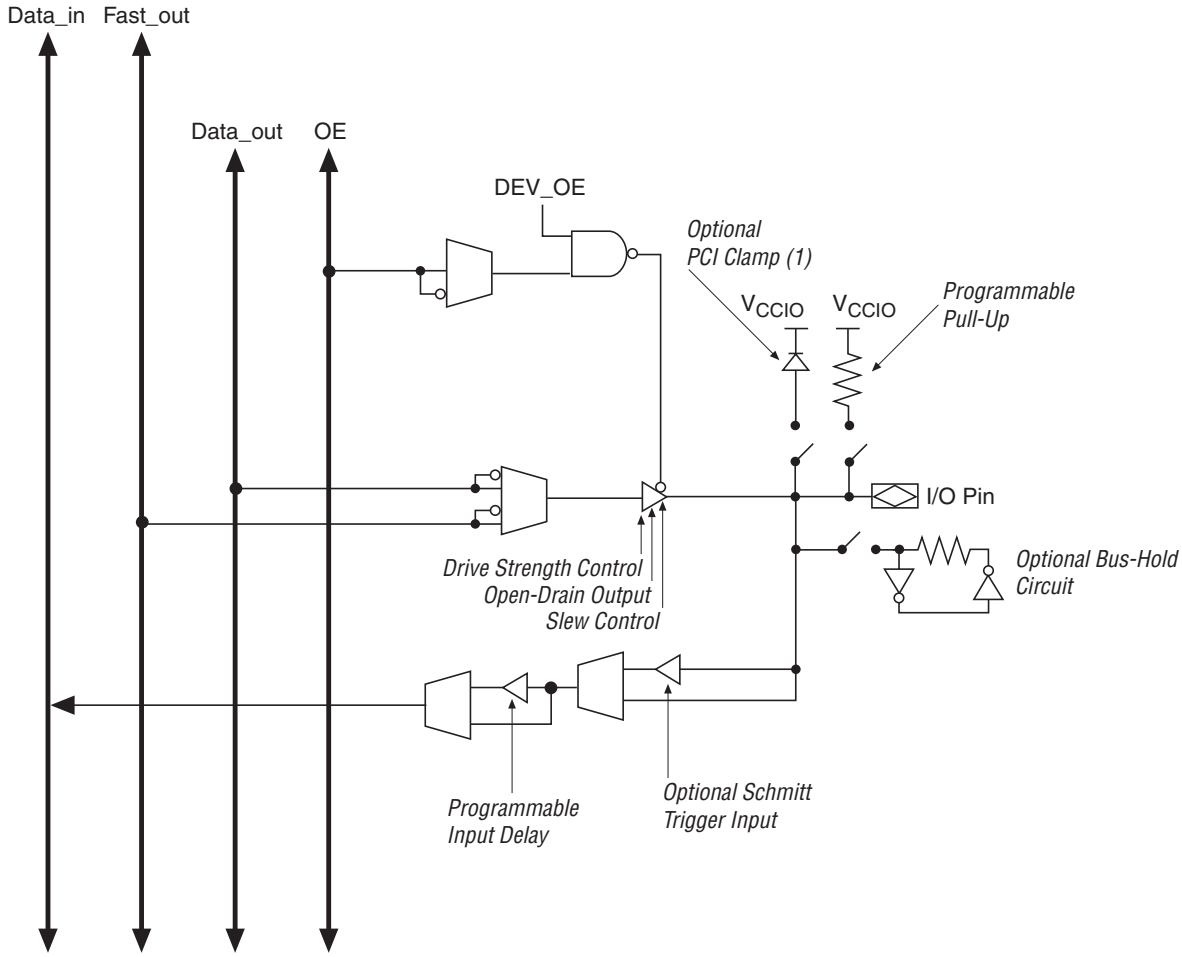
- LVTTL and LVCMOS I/O standards
- 3.3-V, 32-bit, 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Programmable drive strength control
- Weak pull-up resistors during power-up and in system programming
- Slew-rate control
- Tri-state buffers with individual output enable control
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Unique output enable per pin
- Open-drain outputs
- Schmitt trigger inputs
- Fast I/O connection
- Programmable input delay

MAX II device IOEs contain a bidirectional I/O buffer. Figure 2–19 shows the MAX II IOE structure. Registers from adjacent LABs can drive to or be driven from the IOE's bidirectional I/O buffers. The Quartus II software automatically attempts to place registers in the adjacent LAB with fast I/O connection to achieve the fastest possible clock-to-output and registered output enable timing. For input registers, the Quartus II software automatically routes the register to guarantee zero hold time. You can set timing assignments in the Quartus II software to achieve desired I/O timing.

Fast I/O Connection

A dedicated fast I/O connection from the adjacent LAB to the IOEs within an I/O block provides faster output delays for clock-to-output and t_{PD} propagation delays. This connection exists for data output signals, not output enable signals or input signals. Figures 2–20, 2–21, and 2–22 illustrate the fast I/O connection.

Figure 2–19. MAX II IOE Structure



Note to Figure 2–19:
(1) Available in EPM1270 and EPM2210 devices only.

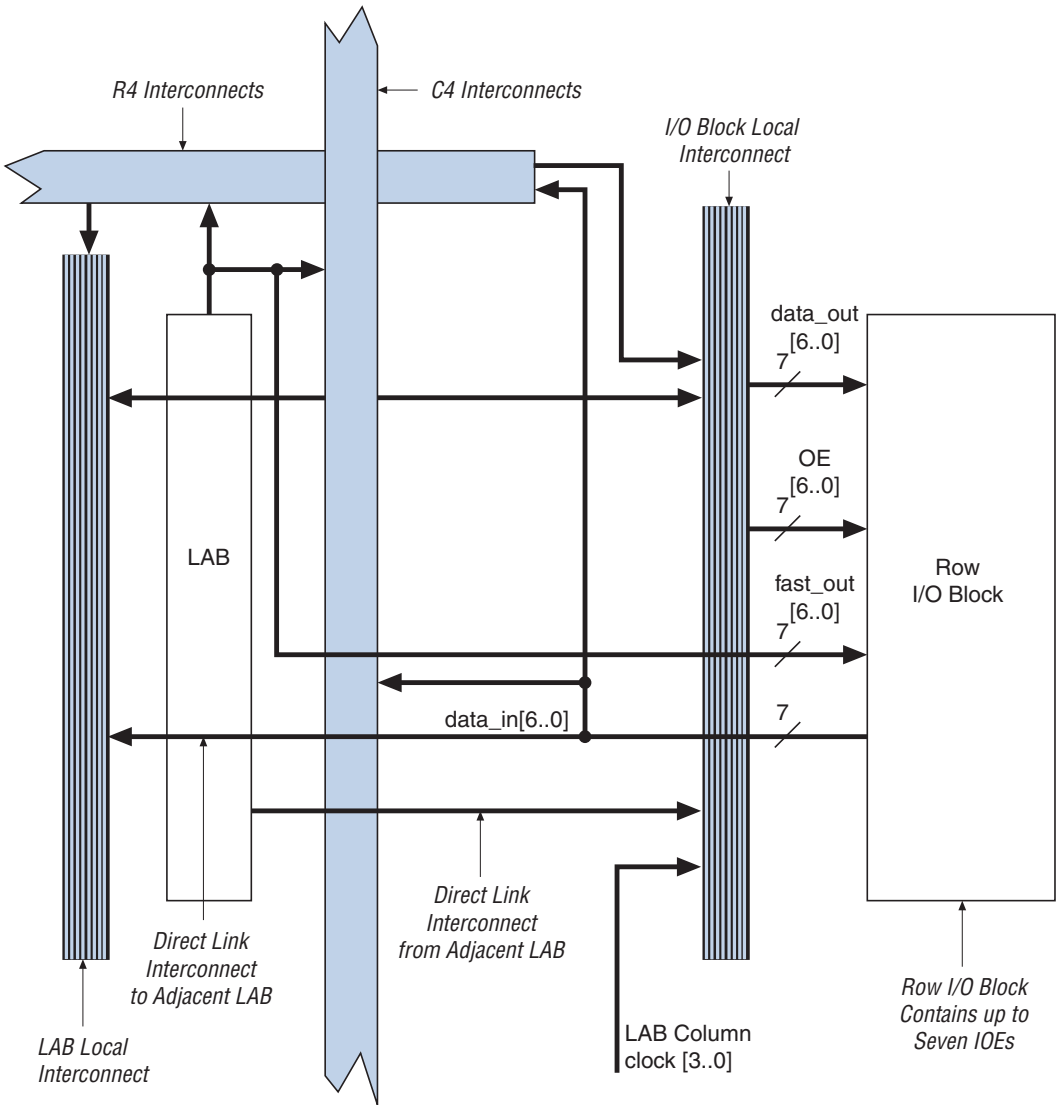
I/O Blocks

The IOEs are located in I/O blocks around the periphery of the MAX II device. There are up to seven IOEs per row I/O block (5 maximum in the EPM240 device) and up to four IOEs per column I/O block. Each column or row I/O block interfaces with its adjacent LAB and MultiTrack

interconnect to distribute signals throughout the device. The row I/O blocks drive row, column, or DirectLink interconnects. The column I/O blocks drive column interconnects.

Figure 2–20 shows how a row I/O block connects to the logic array.

Figure 2–20. Row I/O Block Connection to the Interconnect *Note (1)*

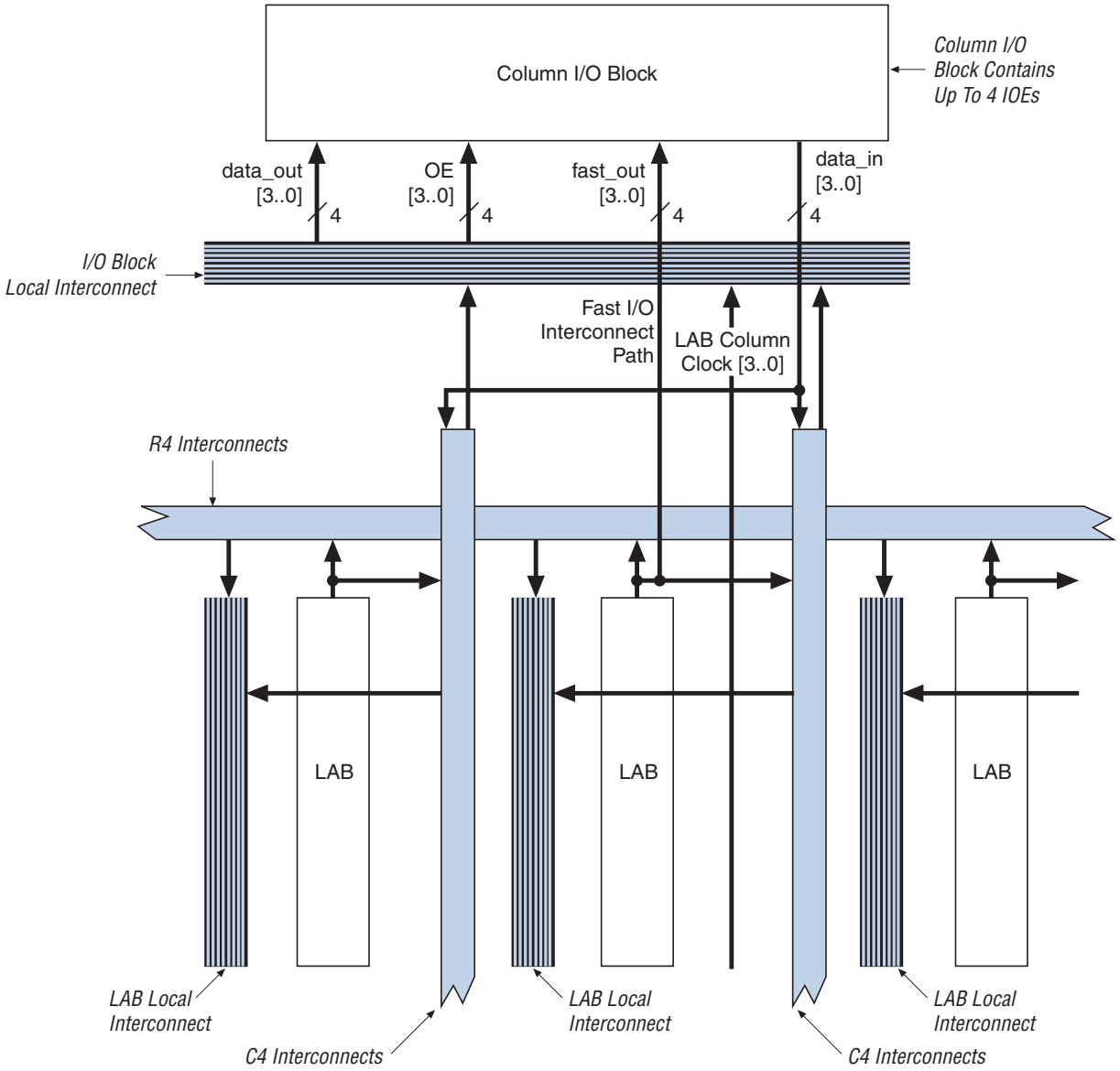


Note to Figure 2–20:

(1) Each of the seven IOEs in the row I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

Figure 2–21 shows how a column I/O block connects to the logic array.

Figure 2–21. Column I/O Block Connection to the Interconnect *Note (1)*



Note to Figure 2–21:

(1) Each of the four IOEs in the column I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

I/O Standards & Banks

MAX II device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI

Table 2–4 describes the I/O standards supported by MAX II devices.

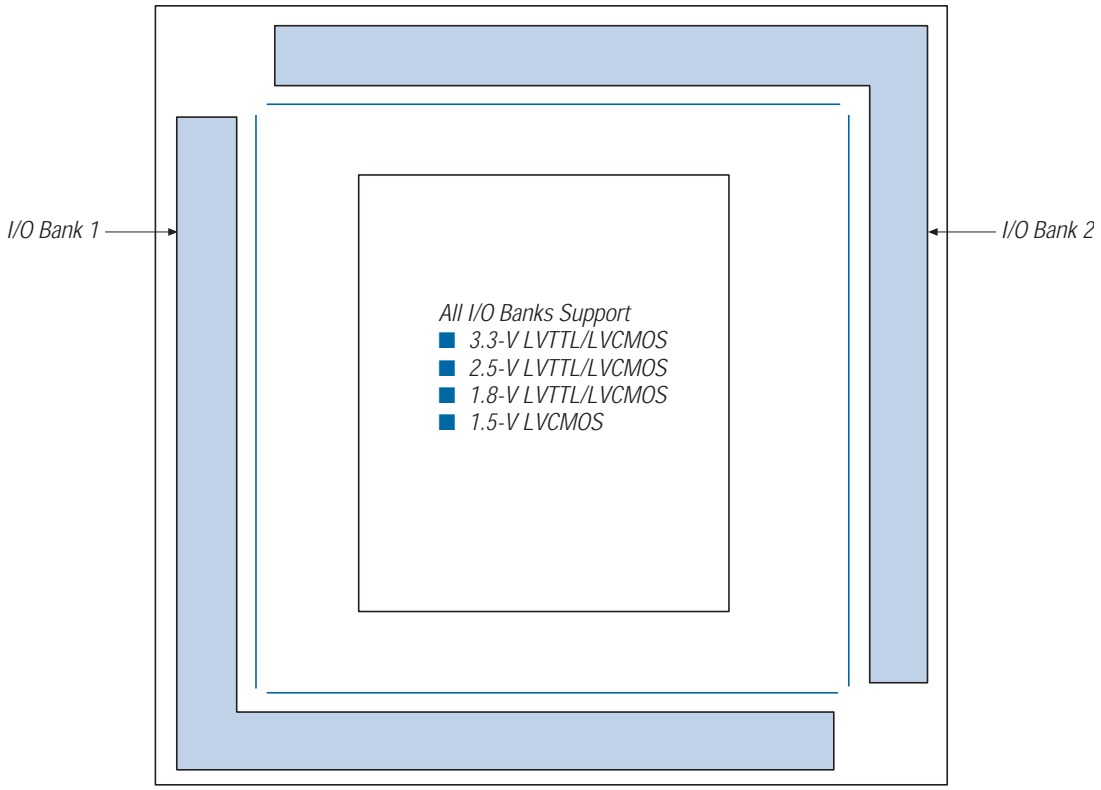
Table 2–4. MAX II I/O Standards

I/O Standard	Type	Output Supply Voltage (V_{CCIO}) (V)
3.3-V LVTTL/LVCMOS	Single-ended	3.3
2.5-V LVTTL/LVCMOS	Single-ended	2.5
1.8-V LVTTL/LVCMOS	Single-ended	1.8
1.5-V LVCMOS	Single-ended	1.5
3.3-V PCI *(1)*	Single-ended	3.3

Note to Table 2–4:
(1) 3.3-V PCI is supported in Bank 3 of the EPM1270 and EPM2210 devices.

The EPM240 and EPM570 devices support two I/O banks, as shown in Figure 2–22. Each of these banks support all the LVTTL and LVCMOS standards shown in Table 2–4. PCI I/O is not supported in these devices and banks.

Figure 2–22. MAX II I/O Banks for EPM240 & EPM570 *Notes (1), (2)*



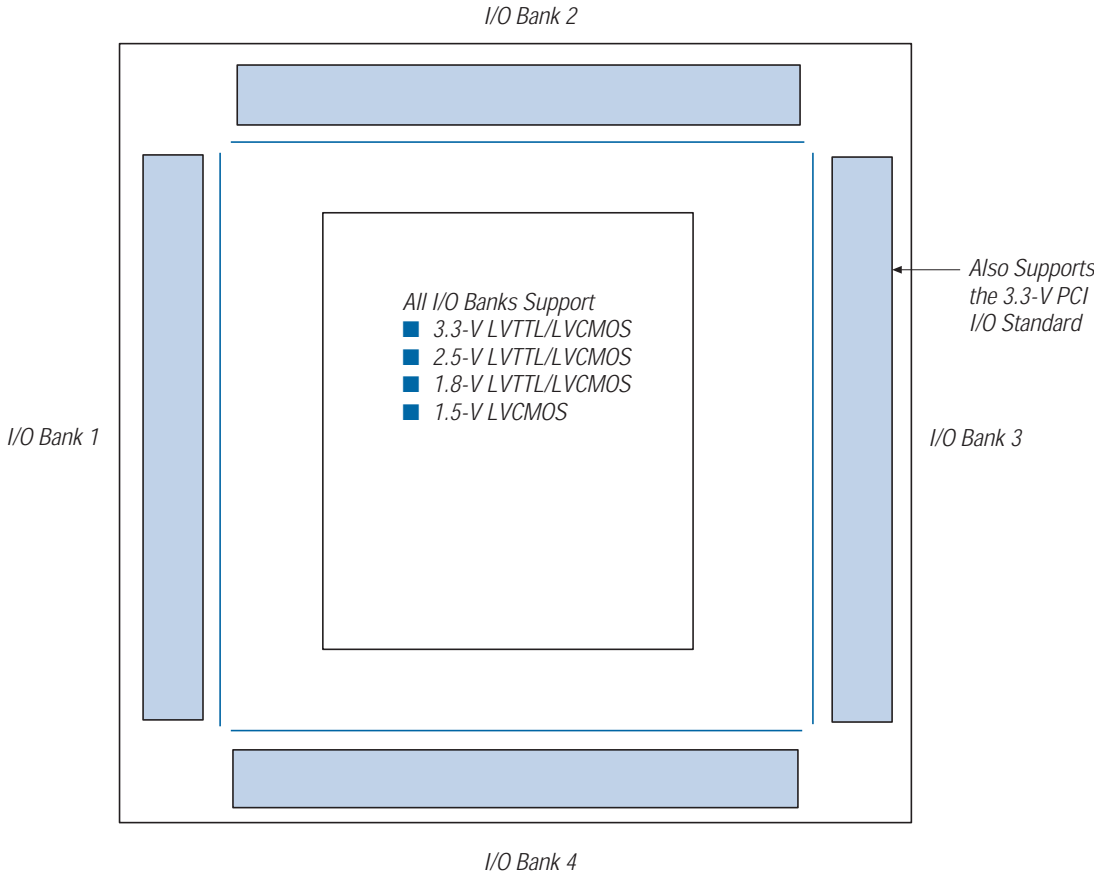
Notes to Figure 2–22:

(1) Figure 2–22 is a top view of the silicon die.

(2) Figure 2–22 is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

The EPM1270 and EPM2210 devices support four I/O banks, as shown in Figure 2–23. Each of these banks support all of the LVTTL and LVCMOS standards shown in Table 2–4. PCI I/O is supported in Bank 3. Bank 3 supports the PCI clamping diode on inputs and PCI drive compliance on outputs. You must use Bank 3 for designs requiring PCI compliant I/O pins. The Quartus II software automatically places I/O pins in this bank if assigned with the PCI I/O standard.

Figure 2–23. MAX II I/O Banks for EPM1270 & EPM2210 *Notes (1), (2)*



Notes to Figure 2–23:
(1) Figure 2–23 is a top view of the silicon die.
(2) Figure 2–23 is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has dedicated VCCIO pins which determine the voltage standard support in that bank. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX II devices.

The JTAG pins for MAX II devices are dedicated pins that cannot be used as regular I/O pins. The pins TMS, TDI, TDO, and TCK support all the I/O standards shown in Table 2–4 on page 2–32 except for PCI. These pins reside in Bank 1 for all MAX II devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

MAX II EPM1270 and EPM2210 devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2–5 shows the MAX II device speed grades that meet the PCI timing specifications.

Table 2–5. MAX II Devices & Speed Grades that Support 3.3-V PCI Electrical Specifications & Meet PCI Timing *Note (1)*

Device	33-MHz PCI
EPM1270	All Speed Grades
EPM2210	All Speed Grades

Note to Table 2–5:
(1) This table contains preliminary information.

Schmitt Trigger

The input buffer for each MAX II device I/O pin has an optional Schmitt trigger setting for the 3.3-V and 2.5-V standards. The Schmitt trigger allows input buffers to respond to slow input edge rates with a fast output edge rate. Most importantly, Schmitt triggers provide hysteresis on the input buffer, preventing slow rising noisy input signals from ringing or oscillating on the input signal driven into the logic array. This provides system noise tolerance on MAX II inputs, but adds a small, nominal input delay.

The JTAG input pins (`TMS`, `TCK`, and `TDI`) have Schmitt trigger buffers which are always enabled.

Output Enable Signals

Each MAX II IOE output buffer supports output enable signals for tri-state control. The output enable signal can originate from the `GCLK[3..0]` global signals or from the MultiTrack interconnect. The MultiTrack interconnect routes output enable signals and allows for a unique output enable for each output or bidirectional pin.

MAX II devices also provide a chip-wide output enable pin (DEV_OE) to control the output enable for every output pin in the design. An option set before compilation in the Quartus II software controls this pin. This chip-wide output enable uses its own routing resources and does not use any of the four global resources. If this option is turned on, all outputs on the chip operate normally when DEV_OE is asserted. When the pin is de-asserted, all outputs are tri-stated. If this option is turned off, the DEV_OE pin is disabled when the device operates in user mode and is available as a user I/O pin.

Programmable Drive Strength

The output buffer for each MAX II device I/O pin has two levels of programmable drive strength control for each of the LVTTL and LVCMOS I/O standards. Programmable drive strength provides system noise reduction control for high performance I/O designs. Although a separate slew-rate control feature exists, using the lower drive strength setting provides signal slew rate control to reduce system noise and signal overshoot without the large delay adder associated with the slew-rate control feature. Table 2–6 shows the possible settings for the I/O standards with drive strength control. The PCI I/O standard is always set at 20 mA with no alternate setting.

Table 2–6. Programmable Drive Strength *Note (1)*

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	16
	8
3.3-V LVCMOS	8
	4
2.5-V LVTTL/LVCMOS	14
	7
1.8-V LVTTL/LVCMOS	6
	3
1.5-V LVCMOS	4
	2

Note to Table 2–6:

(1) The I_{OH} current strength numbers shown are for a condition of a $V_{OUT} = V_{OH}$ minimum, where the V_{OH} minimum is specified by the I/O standard. The I_{OL} current strength numbers shown are for a condition of a $V_{OUT} = V_{OL}$ maximum, where the V_{OL} maximum is specified by the I/O standard. For 2.5-V LVTTL/LVCMOS, the I_{OH} condition is V_{OUT} = 1.7 V and the I_{OL} condition is V_{OUT} = 0.7 V.

Slew-Rate Control

The output buffer for each MAX II device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal output delay to rising and falling edges. The lower the voltage standard (e.g., 1.8-V LVTTL) the larger the output delay when slow slew is enabled. Each I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Open-Drain Output

MAX II devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX II devices can be used as an additional ground pin. This programmable ground feature does not require the use of the associated LEs in the device. In the Quartus II software, unused pins can be set as programmable GND on a global default basis or they can be individually assigned. Unused pins also have the option of being set as tri-stated input pins.

Bus Hold

Each MAX II device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option.

The bus-hold circuitry uses a resistor to pull the signal level to the last driven state. The chapter on *DC & Switching Characteristics* gives the specific sustaining current for each V_{CCIO} voltage level driven through this resistor and overdrive current used to identify the next-driven input level.

The bus-hold circuitry is only active after the device has fully initialized. The bus-hold circuit captures the value on the pin present at the moment user mode is entered.

Programmable Pull-Up Resistor

Each MAX II device I/O pin provides an optional programmable pull-up resistor during user mode. If the designer enables this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

The programmable pull-up resistor feature should not be used at the same time as the bus-hold feature on a given I/O pin.

Programmable Input Delay

The MAX II IOE includes a programmable input delay that is activated to ensure zero hold times. A path where a pin directly drives a register, with minimal routing between the two, may require the delay to ensure zero hold time. However, a path where a pin drives a register through long routing or through combinational logic may not require the delay to achieve a zero hold time. The Quartus II software uses this delay to ensure zero hold times when needed.

MultiVolt I/O Interface

The MAX II architecture supports the MultiVolt I/O interface feature, which allows MAX II devices in all packages to interface with systems of different supply voltages. The devices have one set of `VCC` pins for internal operation (`VCCINT`), and four sets for input buffers and I/O output driver buffers (`VCCIO`).

Connect VCCIO pins to either a 1.5-V, 1.8 V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 2–7 summarizes MAX II MultiVolt I/O support.

Table 2–7. MAX II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓ (2)	✓ (2)		✓				
1.8		✓	✓	✓		✓ (3)	✓			
2.5			✓	✓		✓ (4)	✓ (4)	✓		
3.3			✓ (5)	✓	✓ (6)	✓ (7)	✓ (7)	✓ (7)	✓	✓ (8)

Notes to Table 2–7:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V including the overshoot, disable the PCI clamping diode. However, to drive 5.0-V inputs to the device, enable the PCI clamping diode to prevent V_I from rising above 4.0 V.

(2) When V_{CCIO} = 1.5-V and a 2.5-V or 3.3-V input signal feeds an input pin, higher pin leakage current is expected.

(3) When V_{CCIO} = 1.8-V, a MAX II device can drive a 1.5-V device with 1.8-V tolerant inputs.

(4) When V_{CCIO} = 2.5-V, a MAX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(5) When V_{CCIO} = 3.3-V and a 2.5-V input signal feeds an input pin, the VCCIO supply current will be slightly larger than expected.

(6) MAX II devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode on the EPM1270 and EPM2210 devices.

(7) When V_{CCIO} = 3.3-V, a MAX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

(8) When V_{CCIO} = 3.3-V, a MAX II device can drive a device with 5.0-V TTL inputs but not 5.0-V CMOS inputs. In the case of 5.0-V CMOS, open-drain setting with internal PCI clamp diode (available only on EPM1270 and EPM2210 devices) and external resistor is required.

Chapter 3. JTAG & In-System Programmability

MII51003-1.2

IEEE Std. 1149.1 (JTAG) Boundary Scan Support

All MAX® II devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1-2001 specification. JTAG boundary-scan testing can only be performed at any time after V_{CCINT} and all V_{CCIO} banks have been fully powered and a t_{CONFIG} amount of time has passed. MAX II devices can also use the JTAG port for in-system programming together with either the Quartus® II software or hardware using Programming Object Files (**.pof**), Jam™ Standard Test and Programming Language (STAPL) Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

The JTAG pins support 1.5-V, 1.8-V, 2.5-V, or 3.3-V I/O standards. The supported voltage level and standard is determined by the V_{CCIO} of the bank where it resides. The dedicated JTAG pins reside in Bank 1 of all MAX II devices.

MAX II devices support the JTAG instructions shown in Table 3–1.

Table 3–1. MAX II JTAG Instructions (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. This register defaults to all 1's if not specified in the Quartus II software.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.

Table 3–1. MAX II JTAG Instructions (Part 2 of 2)

JTAG Instruction	Instruction Code	Description
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while holding I/O pins to a state defined by the data in the boundary-scan register.
USER0	00 0000 1100	This instruction allows the user to define their own scan chain between TDI and TDO in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
USER1	00 0000 1110	This instruction allows the user to define their own scan chain between TDI and TDO in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
IEEE 1532 instructions	*(2)*	IEEE 1532 ISC instructions used when programming a MAX II device via the JTAG port.

Notes to Table 3–1:

(1) HIGHZ, CLAMP, and EXTEST instructions do not disable weak pull-up resistors or bus hold features.

(2) These instructions are shown in the 1532 BSDL files, which will be posted on the Altera® web site at **www.altera.com** when they are available.

The MAX II device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for MAX II devices.

Table 3–2. MAX II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM240	240
EPM570	480
EPM1270	636
EPM2210	816

Table 3–3. 32-Bit MAX II Device IDCODE

Device	Binary IDCODE (32 Bits) *(1)*				HEX IDCODE
	Version (4 Bits)	Part Number	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*	
EPM240	0000	0010 0000 1010 0001	000 0110 1110	1	0x020A10DD
EPM570	0000	0010 0000 1010 0010	000 0110 1110	1	0x020A20DD
EPM1270	0000	0010 0000 1010 0011	000 0110 1110	1	0x020A30DD
EPM2210	0000	0010 0000 1010 0100	000 0110 1110	1	0x020A40DD

Notes to Table 3–2:

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

For JTAG AC characteristics, refer to the chapter on *DC & Switching Characteristics*. For more information on JTAG BST, see the chapter on *IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices*.

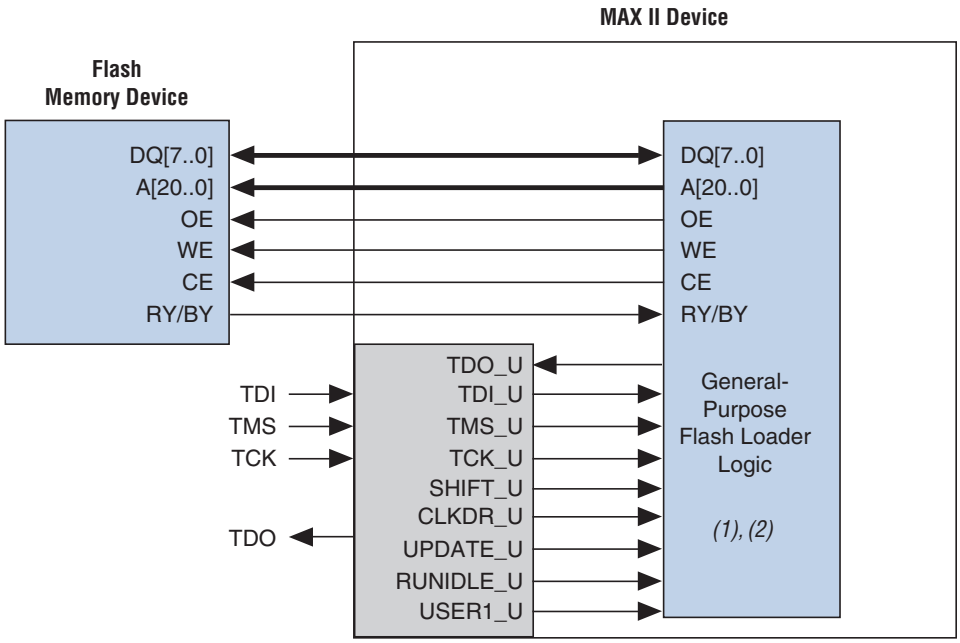
JTAG Translator

The JTAG translator feature allows you to access the JTAG TAP and state signals when either the USER0 or USER1 instruction is issued to the JTAG TAP. The USER0 and USER1 instructions bring the JTAG boundary scan chain (TDI) through the user logic instead of the MAX II device's boundary scan cells. Each USER instruction allows for one unique user-defined JTAG chain into the logic array.

Parallel Flash Loader

The JTAG translator ability to interface JTAG to non-JTAG devices is ideal for general-purpose flash memory devices (such as Intel or Fujitsu based devices) that require programming during in-circuit test. The flash memory devices can be used for FPGA configuration or be part of system memory. In many cases, the MAX II device is already connected to these devices as the configuration control logic between the FPGA and the flash device. Unlike ISP-capable CPLD devices, bulk flash devices do not have JTAG TAP pins or connections. For small flash devices, it is common to use the serial JTAG scan chain of a connected device to program the non-JTAG flash device. This is slow and inefficient in most cases and impractical for large parallel flash devices. Using the MAX II device's JTAG translator as a parallel flash loader to program and verify flash contents provides a fast and cost-effective means of in-circuit programming during test. Figure 3–1 shows MAX II being used as a parallel flash loader.

Figure 3–1. MAX II JTAG Translator as General-Purpose Flash Loader



Notes to Figure 3–1:
(1) This block is implemented in LEs.
(2) This function will be supported in a future version of the Quartus II software.

In System Programmability

MAX II devices can be programmed in-system via the industry standard 4-pin IEEE Std. 1149.1 (JTAG) interface. In system programmability (ISP) offers quick, efficient iterations during design development and

debugging cycles. The logic, circuitry, and interconnects in the MAX II architecture are configured with flash-based SRAM configuration elements. These SRAM elements require configuration data to be loaded each time the device is powered. The process of loading the SRAM data is called configuration. The on-chip configuration flash memory (CFM) block stores the SRAM element's configuration data. The CFM block stores the design's configuration pattern in a reprogrammable flash array. During ISP, the MAX II JTAG and ISP circuitry programs the design pattern into the CFM block's non-volatile flash array.

The MAX II JTAG and ISP controller internally generate the high programming voltages required to program the CFM cells, allowing in-system programming with any of the recommended operating external voltage supplies (i.e., 3.3 V/2.5 V or 1.8 V for the MAX IIG devices). ISP can be performed anytime after V_{CCINT} and all V_{CCIO} banks have been fully powered and the device has completed the configuration power-up time. By default, during in-system programming, the I/O pins are tri-stated and weakly pulled-up to V_{CCIO} to eliminate board conflicts. The in-system programming clamp and real-time ISP feature allows user control of I/O state or behavior during ISP.

For more information, refer to "In-System Programming Clamp" on page 3–7 and "Real-Time ISP" on page 3–7.

These devices also offer an `ISP_DONE` bit that provides safe operation when in-system programming is interrupted. This `ISP_DONE` bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

IEEE 1532 Support

The JTAG circuitry and ISP instruction set in MAX II devices is compliant to the IEEE 1532-2002 programming specification. This provides industry-standard hardware and software for in-system programming among multiple vendor programmable logic devices (PLDs) in a JTAG chain.

The MAX II 1532 BSDL files will be released on the Altera web site when available.

Jam Standard Test & Programming Language (STAPL)

The Jam STAPL JEDEC standard, JESD71, can be used to program MAX II devices with in-circuit testers, PCs, or embedded processors. The Jam byte code is also supported for MAX II devices. These software programming protocols provide a compact embedded solution for programming MAX II devices.

For more information, see the chapter on *Using Jam STAPL for ISP via an Embedded Processor*.

Programming Sequence

During in-system programming, 1532 instructions, addresses, and data are shifted into the MAX II device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data. Programming a pattern into the device requires the following six ISP steps. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6. These steps are automatically executed by third-party programmers, the Quartus® II software, or the Jam STAPL and Jam Byte-Code Players.

1. *Enter ISP* – The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode.

2. *Check ID* – Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Sector Erase* – Erasing the device in-system involves shifting in the instruction to erase the device and applying an erase pulse(s). The erase pulse is automatically generated internally by waiting in the run/test/idle state for the specified erase pulse time of 500 ms for the CFM block and 500 ms for each sector of the UFM block.

4. *Program* – Programming the device in-system involves shifting in the address, data, and program instruction and generating the program pulse to program the flash cells. The program pulse is automatically generated internally by waiting in the run/test/idle state for the specified program pulse time of 75 µs. This process is repeated for each address in the CFM and UFM block.

5. *Verify* – Verifying a MAX II device in-system involves shifting in addresses, applying the verify instruction to generate the read pulse, and shifting out the data for comparison. This process is repeated for each CFM and UFM address.

6. *Exit ISP* – An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode.

For TCK frequencies of 10 MHz, the erase and programming takes less than two seconds for EPM240 and EPM570 devices. Erase and programming times are less than three seconds for EPM1270 and less than four seconds for the EPM2210 devices. The TCK frequency can operate at up to 18 MHz in MAX II devices providing slight improvements in these ISP times.

UFM Programming

The Quartus II software, with the use of POF, Jam, or JBC files, supports programming of each user flash memory (UFM) block sector independent from the logic array design pattern stored in the CFM block. This allows updating or reading UFM contents through ISP without altering the current logic array design, or vice versa. By default, these programming files and methods will program both the entire flash memory contents, which includes the CFM block and UFM contents. The stand-alone embedded Jam STAPL player and Jam Byte-Code Player provides action commands for programming or reading the entire flash memory (UFM and CFM together) or each independently.

For more information, see the chapter on *Using Jam STAPL for ISP via an Embedded Processor*.

In-System Programming Clamp

By default, the IEEE 1532 instruction used for entering ISP automatically tri-states all I/O pins with weak pull-up resistors for the duration of the ISP sequence. However, some systems may require certain pins on MAX II devices to maintain a specific DC logic level during an in-field update. For these systems, an optional in-system programming clamp instruction exists in MAX II circuitry to control I/O behavior during the ISP sequence. The in-system programming clamp instruction enables the device to sample and sustain the value on an output pin (an input pin would remain tri-stated if sampled) or to explicitly set a logic high, logic low, or tri-state value on any pin. Setting these options is controlled on an individual pin basis using the Quartus II software.

For more information, see the chapter on *Real-Time ISP & ISP Clamp for MAX II Devices*.

Real-Time ISP

For systems that require more than DC logic level control of I/O pins, the real-time ISP feature allows you to update the CFM block with a new design image while the current design continues to operate in the SRAM logic array and I/O pins. A new programming file is updated into the MAX II device without halting the original design's operation, saving

down-time costs for remote or field upgrades. The updated CFM block configures the new design into the SRAM upon the next power cycle. It is also possible to execute an immediate configuration of the SRAM without a power cycle by using a specific sequence of ISP commands. The configuration of SRAM without a power cycle takes a specific amount of time (t_{CONFIG}). During this time, the I/O pins are tri-stated and weakly pulled-up to V_{CCIO}.

Design Security

All MAX II devices contain a programmable security bit that controls access to the data programmed into the CFM block. When this bit is programmed, design programming information, stored in the CFM block, cannot be copied or retrieved. This feature provides a high level of design security because programmed data within flash memory cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased. The SRAM is also invisible and cannot be accessed regardless of the security bit setting. The UFM block data is not protected by the security bit and is accessible through JTAG or logic array connections.

Programming with External Hardware

MAX II devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera® ByteblasterMV™, MasterBlaster™, ByteBlaster™ II, and USB-Blaster cables, and through the universal serial bus (USB)-based Altera Programming Unit (APU) with the appropriate adapter.

BP Microsystems, System General, and other programming hardware manufacturers provide programming support for Altera devices. Check their web sites for device support information.

Chapter 4. Hot Socketing & Power-On Reset in MAX II Devices

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Hot Socketing

MAX® II devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support. Designers can insert or remove a MAX II board in a system during operation without undesirable effects to the system bus. The hot socketing feature removes some of the difficulty designers face when using components on printed circuit boards (PCBs) that contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices.

The MAX II device hot socketing feature provides:

- Board or device insertion and removal
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

MAX II Hot-Socketing Specifications

MAX II devices offer all three of the features required for hot socketing capability listed above without any external components or special design requirements. The following are hot-socketing specifications:

- The device can be driven before and during power-up or power-down without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies. External input signals to I/O pins of the device do not internally power the V_{CCIO} or V_{CCINT} power supplies of the device via internal paths.

Devices Can Be Driven before Power-Up

Signals can be driven into the MAX II device I/O pins and `GCLK[3..0]` pins before or during power-up or power-down without damaging the device. MAX II devices support any power-up or power-down sequence (V_{CCIO1}, V_{CCIO2}, V_{CCIO3}, V_{CCIO4}, V_{CCINT}), simplifying system-level design.

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot socketing situation, the MAX II device's output buffers are turned off during system power-up. MAX II devices do not drive out until the device attains proper operating conditions and is fully configured. See "Power-On Reset Circuitry" on page 4–6 for information about turn-on voltages.

Signal Pins Do Not Drive the V_{CCIO} or V_{CCINT} Power Supplies

MAX II devices do not have a current path from I/O pins or `GCLK[3..0]` pins to the V_{CCIO} or V_{CCINT} pins before or during power-up. A MAX II device may be inserted into (or removed from) a system board that was powered up without damaging or interfering with system-board operation. When hot socketing, MAX II devices may have a minimal effect on the signal integrity of the backplane.

AC & DC Specifications

You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. There are no V_{CC} ramp rate requirements for MAX II devices. During hot socketing, the I/O pin capacitance is less than 8 pF. MAX II devices meet the following hot socketing specification:

- The hot socketing DC specification is $| I_{IOPIN} | < 300$ µA.
- The hot socketing AC specification is dependent on the signal voltages and board capacitance:

$$| I_{IOPIN} | < (\Delta v / \Delta t) \times \text{capacitance}$$

where capacitance is the sum of I/O pin, trace, and connector capacitance.

MAX II devices are immune to latch-up when hot socketing.

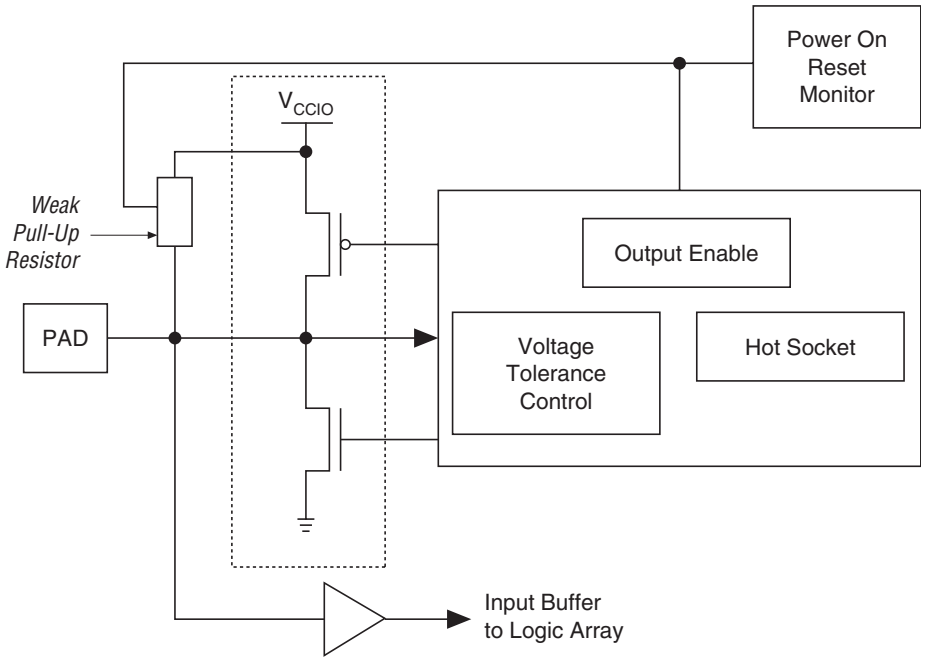
If the `TCK` JTAG input pin is driven high during hot-socketing, the current on that pin might exceed the specifications above.

Hot Socketing Feature Implementation in MAX II Devices

The hot socketing feature turns off (tri-states) the output buffer during the power-up event (either V_{CCINT} or V_{CCIO} supplies) or power down. The hot-socket circuit generates an internal HOTSCKT signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage. The HOTSCKT signal cuts off the output buffer to make sure that no DC current (except for weak pull-up leaking) leaks through the pin. When V_{CC} ramps up very slowly, V_{CC} may still be relatively low even after the power-on reset (POR) signal is released and device configuration is complete.

Each I/O and clock pin has the following circuitry, as shown in Figure 4–1.

Figure 4–1. Hot Socketing Circuit Block Diagram for MAX II Devices



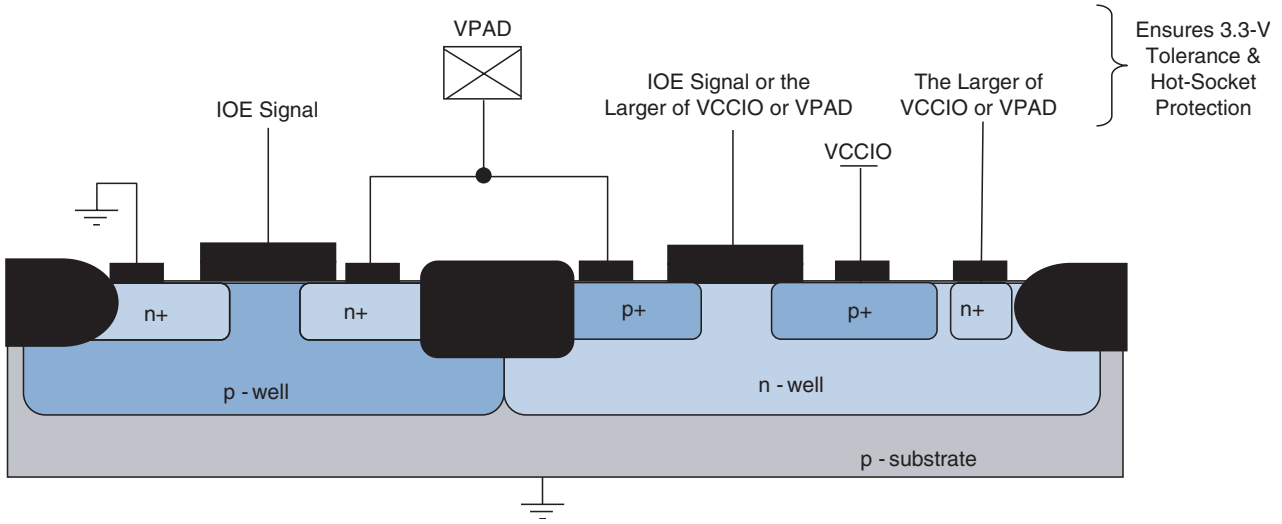
The POR circuit monitors V_{CCINT} and V_{CCIO} voltage levels and keeps I/O pins tri-stated until the device has completed its flash memory configuration of the SRAM logic. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is enabled during download to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not fully powered or

operational. The hot- socket circuit prevents I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.

For information on 5.0-V tolerance, See the chapter on *Using MAX II Devices in Multi-Voltage Systems*.

Figure 4–2 shows a transistor level cross section of the MAX II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

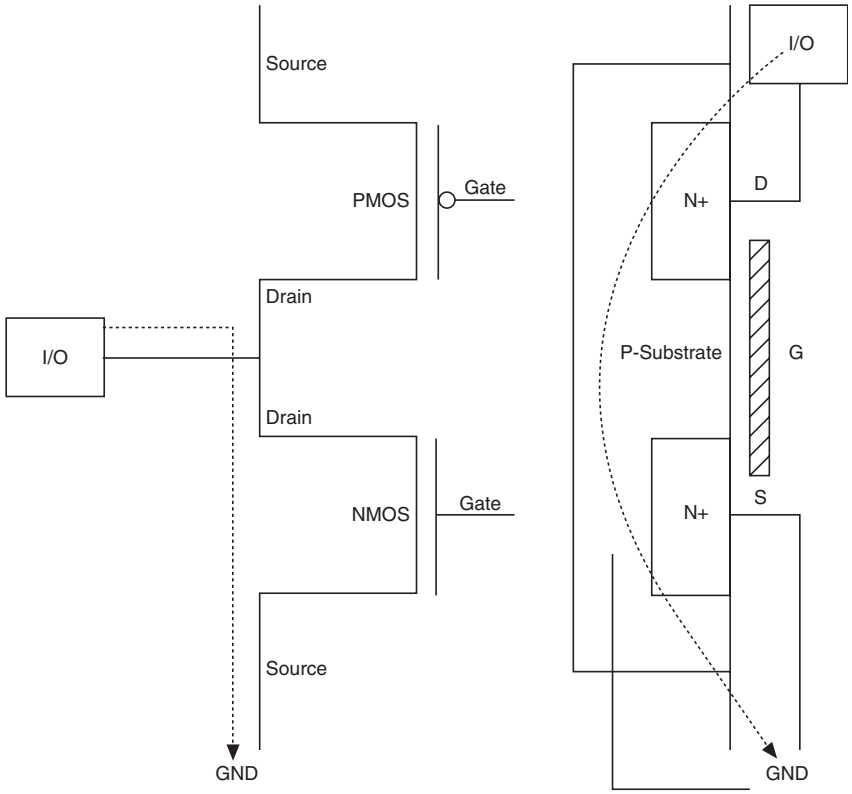
Figure 4–2. Transistor-Level Diagram of MAX II Device I/O Buffers



The CMOS output drivers in the I/O pins intrinsically provide electrostatic discharge (ESD) protection. There are two cases to consider for ESD voltage strikes: positive voltage zap and negative voltage zap.

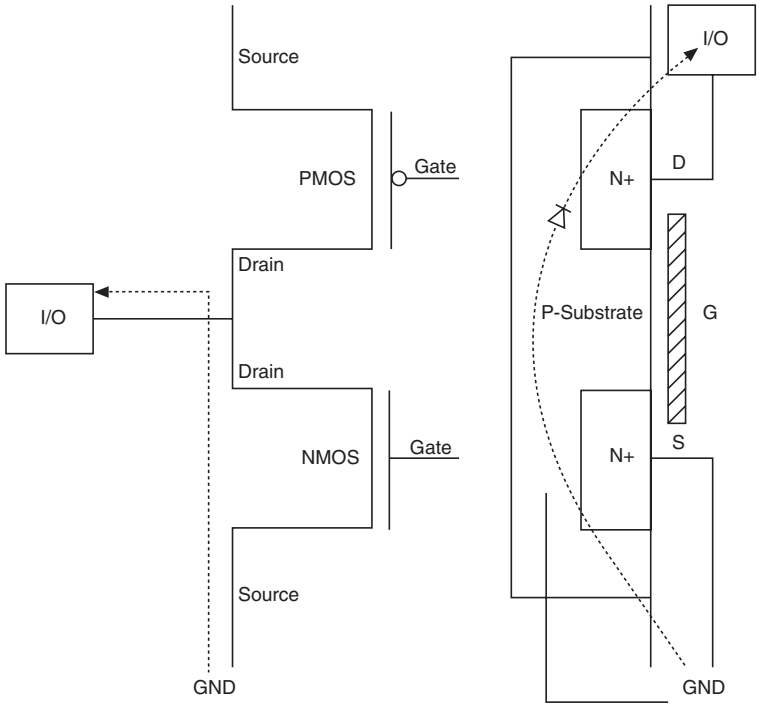
A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain)/P-Substrate junction of the N-channel drain to break down and the N+ (Drain)/P-Substrate/N+ (Source) intrinsic bipolar transistor turns on to discharge ESD current from I/O pin to GND. The dashed line (see Figure 4–3) shows the ESD current discharge path during a positive ESD zap.

Figure 4–3. ESD Protection During Positive Voltage Zap



When the I/O pin receives a negative ESD zap at the pin that is less than -0.7 V (0.7 V is the voltage drop across a diode), the intrinsic P-Substrate/N+ drain diode is forward biased. Hence, the discharge ESD current path is from GND to the I/O pin, as shown in Figure 4–4.

Figure 4–4. ESD Protection During Negative Voltage Zap



Power-On Reset Circuitry

MAX II devices have POR circuits to V_{CCINT} and V_{CCIO} voltage levels during power-up. The POR circuit monitors these voltages, triggering download from the non-volatile configuration flash memory (CFM) block to the SRAM logic, maintaining tri-state of the I/O pins (with weak pull-up resistors enabled) before and during this process. When the MAX II device enters user mode, the POR circuit releases the I/O pins to user functionality and continues to monitor the V_{CCINT} voltage level to detect a brown-out condition. If there is a V_{CCINT} voltage sag below the MAX II operational level during user mode, the POR circuit resets the device and re-triggers an SRAM download. The I/O bank V_{CCIO} levels are not monitored after initial power-up and transition into user mode functionality.

Power-Up Characteristics

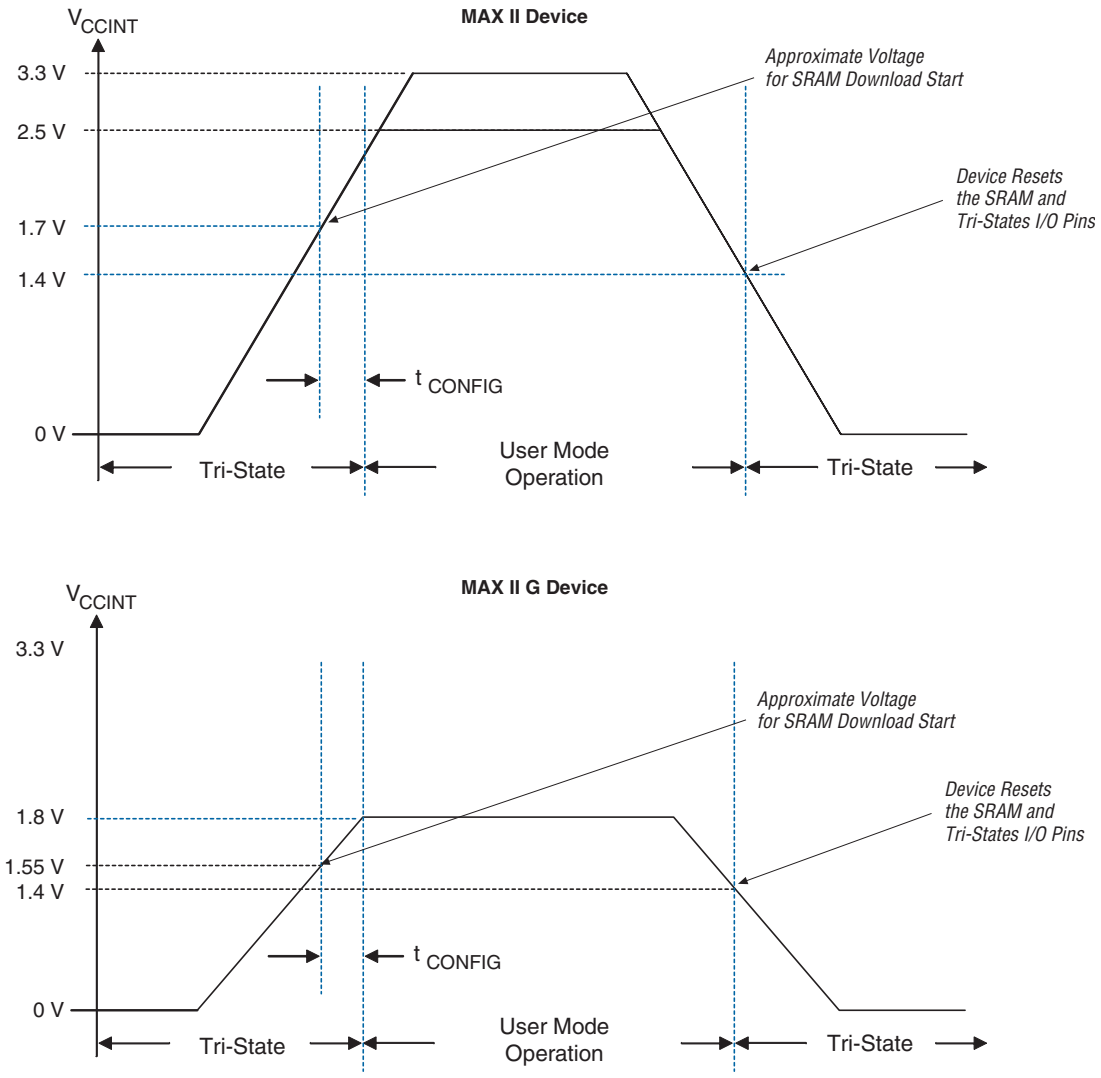
When power is applied to a MAX II device, the POR circuit monitors V_{CCINT} and begins SRAM download at a maximum voltage of 1.7 V, or 1.55 V for MAX II G devices. From this voltage reference, SRAM download and entry into user mode takes 200 to 450 µs maximum depending on device density. This period of time is specified as t_{CONFIG} in the power-up timing section of *Chapter 5. DC & Switching Characteristics*.

Entry into user mode is gated by whether all V_{CCIO} banks are powered with sufficient operating voltage. If V_{CCINT} and V_{CCIO} are powered simultaneously, the device enters user mode within the t_{CONFIG} specifications. If V_{CCIO} is powered more than t_{CONFIG} after V_{CCINT}, the device does not enter user mode until 2 µs after all V_{CCIO} banks are powered.

In user mode, the POR circuitry continues to monitor the V_{CCINT} (but not V_{CCIO}) voltage level to detect a brown-out condition. If there is a V_{CCINT} voltage sag at or below 1.4 V during user mode, the POR circuit resets the SRAM and tri-states the I/O pins. Once V_{CCINT} rises back to 1.7 V (or 1.55 V for MAX II G devices), the SRAM download restarts and the device begins to operate after t_{CONFIG} time has passed.

Figure 4–5 shows the voltages for MAX II and MAX II G device POR during power-up into user mode and from user mode to power-down or brown-out.

Figure 4–5. Power-Up Characteristics for MAX II & MAX II G Devices *Notes (1), (2)*



Notes to Figure 4–5:

(1) Time scale is relative.

(2) Figure 4–5 assumes all V_{CCIO} banks power simultaneously with the V_{CCINT} profile shown. If not, t_{CONFIG} stretches out until all V_{CCIO} banks are powered.

After SRAM configuration, all registers in the device are cleared and released into user function before I/O tri-states are released. To release clears after tri-states are released, use the DEV_CLRn pin option. To hold the tri-states beyond the power-up configuration time, use the DEV_OE pin option.

Chapter 5. DC & Switching Characteristics

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Operating Conditions

Tables 5–1 through 5–12 provide information on absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for MAX® II devices.

Absolute Maximum Ratings

Table 5–1 shows the absolute maximum ratings for the MAX II device family.

Table 5–1. MAX II Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Internal Supply voltage *(3)*	With respect to ground	–0.5	4.6	V
V_{CCIO}	I/O Supply Voltage		–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	TQFP and BGA packages under bias		135	° C

Notes to Table 5–1:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 5–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Maximum V_{CCINT} for MAX II devices is 4.6 V. For MAX IIG devices, it is 2.4 V.

Recommended Operating Conditions

Table 5–2 shows the MAX II device family recommended operating conditions.

Table 5–2. MAX II Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT} *(1)*	3.3-V supply voltage for internal logic and ISP		3.00	3.60	V
	2.5-V supply voltage for internal logic and ISP		2.375	2.625	V
	1.8-V supply voltage for internal logic and ISP (MAX IIG devices)		1.71	1.89	V
V_{CCIO} *(1)*	Supply voltage for I/O buffers, 3.3-V operation		3.00	3.60	V
	Supply voltage for I/O buffers, 2.5-V operation		2.375	2.625	V
	Supply voltage for I/O buffers, 1.8-V operation		1.71	1.89	V
	Supply voltage for I/O buffers, 1.5-V operation		1.425	1.575	V
V_I	Input voltage	*(2)*, *(3)*, *(4)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V

Table 5–2. MAX II Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C

Notes to Table 5–2:

(1) MAX II device in-system programming and/or UFM programming via JTAG or logic array is not guaranteed outside the recommended operating conditions (i.e., if brown-out occurs in the system during a potential write/program sequence to the UFM, users are recommended to read back UFM contents and verify against the intended write data).

(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) During transitions, the inputs may overshoot to the voltages shown in the following table based upon input duty cycle. The DC case is equivalent to 100% duty cycle. For more information on 5.0-V tolerance refer to the chapter on *Using MAX II Devices in Multi-Voltage Systems*.

V_{IN}	Max. Duty Cycle
4.0 V	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

(4) All pins, including clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

Programming/Erasure Specifications

Table 5–3 shows the MAX II device family programming/erasure specifications.

Table 5–3. MAX II Device Programming/Erasure Specifications

Parameter	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	100 *(1)*			Cycles

Note to Table 5–3:

(1) This specification applies to the user flash memory (UFM) and CFM blocks.

DC Electrical Characteristics

Table 5–4 shows the MAX II device family DC electrical characteristics.

Table 5–4. MAX II Device DC Electrical Characteristics *Note (1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*	–10		10	µA
$I_{CCSTANDBY}$	V_{CCINT} supply current (standby) *(3)*	MAX II devices		12		mA
		MAX IIG devices		2		mA
$V_{SCHMITT}$	Hysteresis for Schmitt trigger input	V_{CCIO} = 3.3 V		460		mV
		V_{CCIO} = 2.5 V		170		mV
$I_{CCPower-up}$	V_{CCINT} supply current during power-up *(4)*	MAX II devices		40		mA
		MAX IIG devices		30		mA
R_{PULLUP}	Value of I/O pin pull-up resistor during power-up and in-system programming	V_{CCIO} = 3.3 V *(5)*	5		25	kΩ
		V_{CCIO} = 2.5 V *(5)*	10		40	kΩ
		V_{CCIO} = 1.8 V *(5)*	25		60	kΩ
		V_{CCIO} = 1.5 V *(5)*	45		95	kΩ
C_{IO}	Input capacitance for user I/O pin				8	pF
C_{GCLK}	Input capacitance for dual-purpose GCLK/user I/O pin				8	pF

Note to Table 5–4:

(1) Typical values are for T_A = 25 ° C, V_{CCINT} = 3.3 or 2.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, or 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) V_I = ground, no load, no toggling inputs.

(4) This is average current during power-up. The typical peak current is no more than 65 mA for MAX II devices. For MAX IIG devices, the typical peak current is no more than 55 mA.

(5) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Tables 5–5 through 5–10 show the MAX II device family I/O standard specifications.

Table 5–5. 3.3-V LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.5	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(1)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(1)*		0.45	V

Table 5–6. 3.3-V LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.5	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = -0.1 mA	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA		0.2	V

Table 5–7. 2.5-V I/O Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.5	0.7	V

Table 5–7. 2.5-V I/O Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 mA *(1)*	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OL} = 1 mA		0.4	V
		I_{OL} = 2 mA *(1)*		0.7	V

Table 5–8. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.71	1.89	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(1)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(1)*		0.45	V

Table 5–9. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.425	1.575	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(1)*	0.75 × V_{CCIO}		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(1)*		0.25 × V_{CCIO}	V

Notes to Tables 5–5 through 5–9:

(1) Drive strength is programmable according to values in *Chapter 2. MAX II Architecture*.

Table 5–10. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OL} = 1.5 mA			0.1 × V_{CCIO}	V

Bus Hold Specifications

Table 5–11 shows the MAX II device family bus hold specifications.

Table 5–11. Bus Hold Specifications

Parameter	Conditions	V_{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V_{IN} > V_{IL} (maximum)	20		30		50		70		µA
High sustaining current	V_{IN} < V_{IH} (minimum)	–20		–30		-50		–70		µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}		160		200		300		500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}		–160		–200		–300		–500	µA

Power-Up Timing

Table 5–12 shows the power-up timing characteristics for MAX II devices.

Table 5–12. MAX II Power-Up Timing *Note (1)*

Symbol	Parameter	Device	Min	Typ	Max	Unit
t_{CONFIG}	The amount of time from when V_{CCINT} reaches 2.375 V until the device enters user mode *(2)*	EPM240			200	µs
		EPM570			300	µs
		EPM1270			300	µs
		EPM2210			450	µs

Notes to Table 5–12:

(1) These numbers are preliminary.

(2) For more information on POR trigger voltage, refer to the chapter on *Hot Socketing & Power-On Reset in MAX II Devices*.

Power Consumption

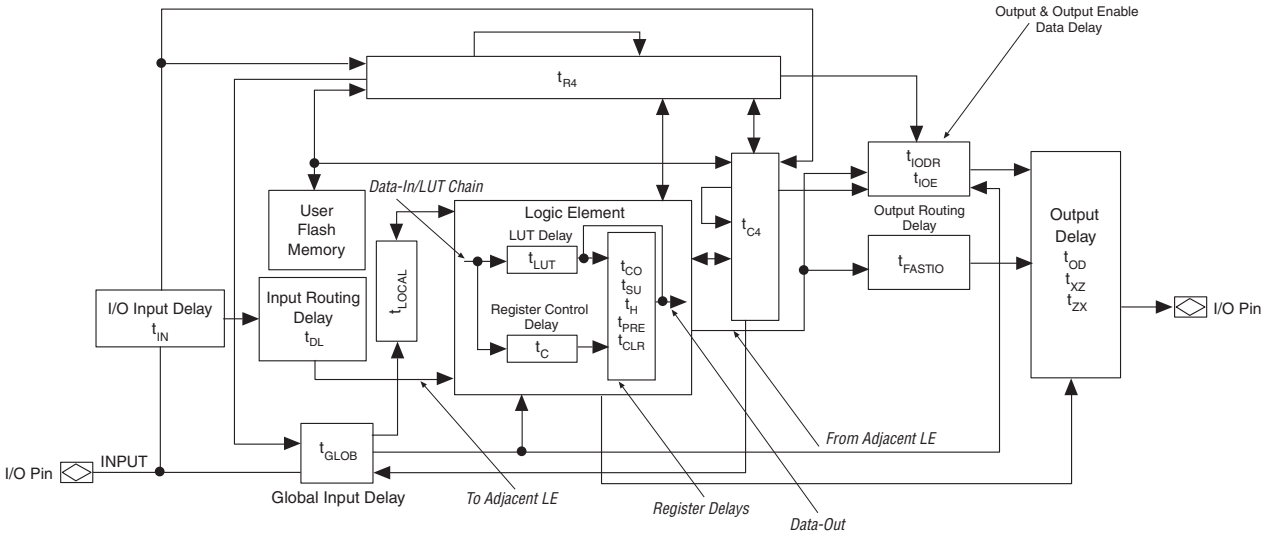
Designers can use the Altera® web power calculator to estimate the device power. See the chapter on *Understanding & Evaluating Power in MAX II Devices* for more information.

Timing Model & Specifications

MAX II devices timing can be analyzed with the Altera Quartus II software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 5–1.

MAX II devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 5–1. MAX II Device Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Refer to the chapter on *Understanding Timing in MAX II Devices* for more information.

This section describes and specifies the performance, internal, external, and UFM timing specifications. All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary & Final Timing

Timing models can have either preliminary or final status. The Quartus® II software issues an informational message during the design compilation if the timing models are preliminary. Table 5–13 shows the status of the MAX II device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 5–13. MAX II Device Timing Model Status

Device	Preliminary	Final
EPM240	✓	
EPM570	✓	
EPM1270	✓	
EPM2210	✓	

Performance

Table 5–14 shows the MAX II device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions. These performance values are based on an EPM1270 device target.

Table 5–14. MAX II Device Performance (Part 1 of 2)

Resource Used	Design Size & Function	Mode	Resources Used		Performance			Unit
			LEs	UFM Blocks	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	
LE	16-bit counter *(1)*	-	16	0	304.0	249.9	202.9	MHz
	64-bit counter *(1)*	-	64	0	200.7	154.6	125.0	MHz
	16-to-1 multiplexer	-	11	0	6.3	8.1	10.3	ns
	32-to-1 multiplexer	-	24	0	7.2	9.2	11.3	ns
	16-bit XOR function	-	5	0	5.3	6.8	8.7	ns
	16-bit decoder with single address line	-	5	0	5.5	6.8	8.7	ns

Table 5–14. MAX II Device Performance (Part 2 of 2)

Resource Used	Design Size & Function	Mode	Resources Used		Performance			Unit
			LEs	UFM Blocks	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	
UFM	512 x 16	None	3	1	10.0	10.0	10.0	MHz
	512 x 16	SPI *(2)*	37	1	9.8	9.8	9.7	MHz
	512 x 8	Parallel *(3)*	73	1	*(4)*	*(4)*	*(4)*	MHz

Notes to Table 5–14:

(1) This design is a binary loadable up counter.
(2) This design is configured for read only operation in Extended mode. Read and write ability increases the number of LEs used.
(3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.
(4) This design is asynchronous.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 5–15 through 5–22 describe the MAX II device internal timing microparameters for logic elements (LEs), input/output elements (IOEs), UFM structures, and MultiTrack™ interconnects.

For more explanations and descriptions on each internal timing microparameters symbol, refer to the chapter on *Understanding Timing in MAX II Devices*.

Table 5–15. LE Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{LUT}	LE combinational LUT delay		583		757		932	ps
t_{CLR}	LE register clear delay	243		315		388		ps
t_{PRE}	LE register preset delay	243		315		388		ps
t_{SU}	LE register setup time before clock	113		146		180		ps
t_{H}	LE register hold time after clock	0		0		0		ps

Table 5–15. LE Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{CO}	LE register clock-to-output delay		243		315		388	ps
t_{CLKHL}	Minimum clock high or low time	170		221		272		ps
t_{C}	Register control delay		875		1,137		1,400	ps

Table 5–16. IOE Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{FASTIO}	Data output delay from adjacent LE to I/O block		164		214		261	ps
t_{IN}	I/O input pad and buffer delay		708		920		1,132	ps
t_{GLOB} *(1)*	I/O input pad and buffer delay use as global signal pin		1,588		2,064		2,540	ps
t_{IOE}	Internally generated output enable delay		424		552		679	ps
t_{DL}	Input routing delay		171		222		274	ps
t_{OD} *(2)*	Output delay buffer and pad delay		1,064		1,383		1,702	ps
t_{XZ} *(3)*	Output buffer disable delay		756		982		1,209	ps
t_{ZX} *(4)*	Output buffer enable delay		1,003		1,303		1,604	ps

Notes to Table 5–16:

(1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers shown in Table 5–16 are based on an EPM240 device target.

(2) Refer to Table 5–29 and Table 5–31 for delay adders associated with different I/O Standards, drive strengths, and slew rates.

(3) Refer to Table 5–19 and Table 5–20 for t_{XZ} delay adders associated with different I/O Standards, drive strengths, and slew rates.

(4) Refer to Table 5–17 and Table 5–18 for t_{ZX} delay adders associated with different I/O Standards, drive strengths, and slew rates.

Tables 5–17 and 5–18 show the adder delays for t_{OD} and t_{ZX} microparameters when using an I/O standard other than 3.3-V LVTTL with 16 mA drive strength.

Table 5–17. t_{ZX} IOE Microparameter Adders for Fast Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	8 mA		0		0		0	ps
	4 mA		28		37		45	ps
3.3-V LVTTL	16 mA		0		0		0	ps
	8 mA		28		37		45	ps
2.5-V LVTTL	14 mA		14		19		23	ps
	7 mA		95		124		152	ps
1.8-V LVTTL	6 mA		450		585		720	ps
	3 mA		526		684		842	ps
1.5-V LVTTL	4 mA		926		1,204		1,482	ps
	2 mA		1,005		1,307		1,608	ps
3.3-V PCI	20 mA		19		25		31	ps

Table 5–18. t_{ZX} IOE MIcroparameter Adders for Slow Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	8 mA		5,682		5,382		5,081	ps
	4 mA		6,416		6,116		5,815	ps
3.3-V LVTTL	16 mA		5,682		5,382		5,081	ps
	8 mA		6,416		6,116		5,815	ps
2.5-V LVTTL	14 mA		8,510		8,210		7,909	ps
	7 mA		9,437		9,137		8,836	ps
3.3-V PCI	20 mA		–75		–375		–676	ps

Table 5–19. t_{XZ} IOE Microparameter Adders for Fast Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	8 mA		0		0		0	ps
	4 mA		–56		–72		–89	ps
3.3-V LVTTL	16 mA		0		0		0	ps
	8 mA		–56		–72		–89	ps
2.5-V LVTTL	14 mA		–3		–4		–5	ps
	7 mA		–47		–61		–75	ps
1.8-V LVTTL	6 mA		40		52		64	ps
	3 mA		–47		61		75	ps
1.5-V LVTTL	4 mA		152		198		243	ps
	2 mA		197		256		315	ps
3.3-V PCI	20 mA		71		93		114	ps

Table 5–20. t_{XZ} IOE MIcroparameter Adders for Slow Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	8 mA		206		–20		–247	ps
	4 mA		159		–67		–294	ps
3.3-V LVTTL	16 mA		206		–20		–247	ps
	8 mA		159		–67		–294	ps
2.5-V LVTTL	14 mA		222		–4		–231	ps
	7 mA		188		–38		–265	ps
3.3-V PCI	20 mA		161		–65		–292	ps

Table 5–21. UFM Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{ASU}	Address register shift signal setup to address register clock	20		20		20		ns
t_{AH}	Address register shift signal hold to address register clock	20		20		20		ns
t_{ADS}	Address register data in setup to address register clock	20		20		20		ns
t_{ADH}	Address register data in hold from address register clock	20		20		20		ns
t_{DSS}	Data register shift signal setup to data register clock	60		60		60		ns
t_{DSH}	Data register shift signal hold from data register clock	20		20		20		ns
t_{DDS}	Data register data in setup to data register clock	20		20		20		ns
t_{DDH}	Data register data in hold from data register clock	20		20		20		ns
t_{DP}	Program signal to data clock hold time	0		0		0		ns
t_{PB}	Maximum delay between program rising edge to UFM busy signal rising edge		960		960		960	ns
t_{BP}	Minimum delay allowed from UFM busy signal going low to program signal going low	20		20		20		ns

Table 5–21. UFM Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{PPMX}	Maximum length of busy pulse during a program		100		100		100	µs
t_{AE}	Minimum erase signal to address clock hold time	0		0		0		ns
t_{EB}	Maximum delay between the erase rising edge to the UFM busy signal rising edge		960		960		960	ns
t_{BE}	Minimum delay allowed from the UFM busy signal going low to erase signal going low	20		20		20		ns
t_{EPMX}	Maximum length of busy pulse during an erase		500		500		500	ms
t_{DCO}	Delay from data register clock to data register output		5		5		5	ns
t_{OE}	Delay from data register clock to data register output	136		136		136		ns
t_{RA}	Maximum read access time		65		65		65	ns
t_{OSCS}	Maximum delay between the OSC_ENA rising edge to the erase/program signal rising edge	350		350		350		ns
t_{OSCH}	Minimum delay allowed from the erase/program signal going low to OSC_ENA signal going low	350		350		350		ns

Figures 5–2 through 5–4 show the read, program, and erase waveforms for UFM block timing parameters shown in Table 5–21.

Figure 5–2. UFM Read Waveforms

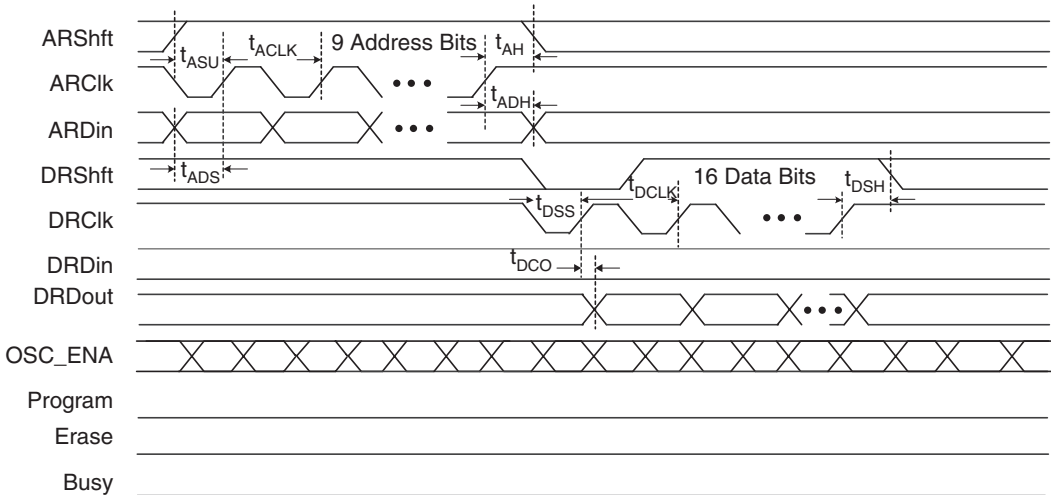


Figure 5–3. UFM Program Waveforms

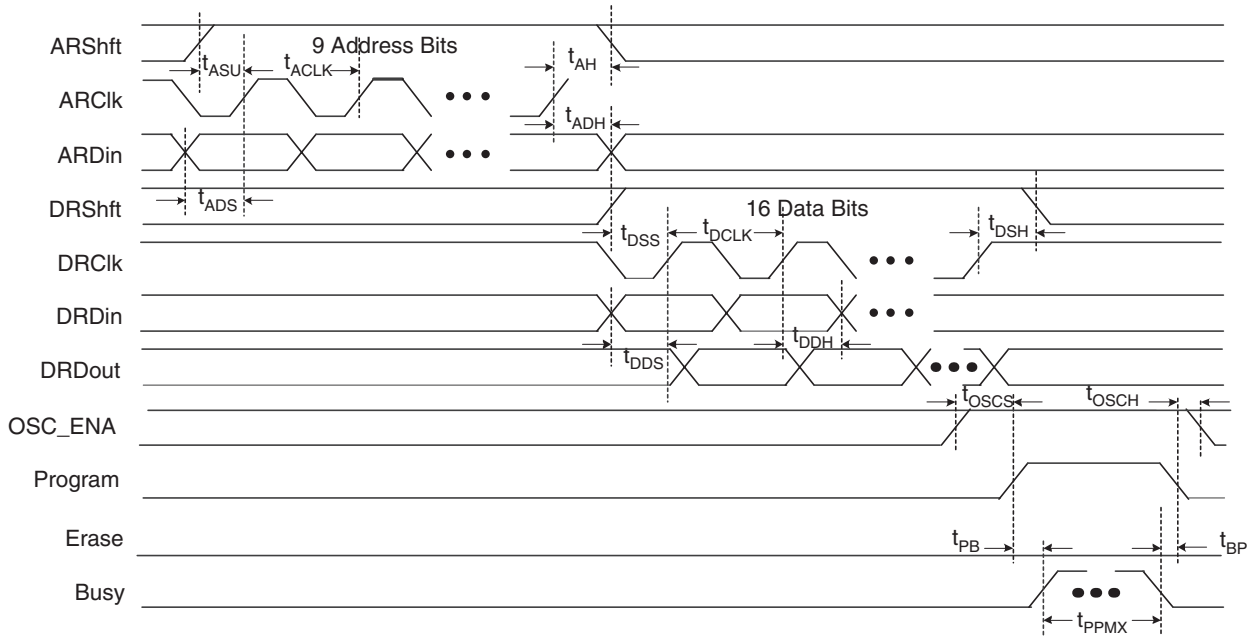


Figure 5–4. UFM Erase Waveforms

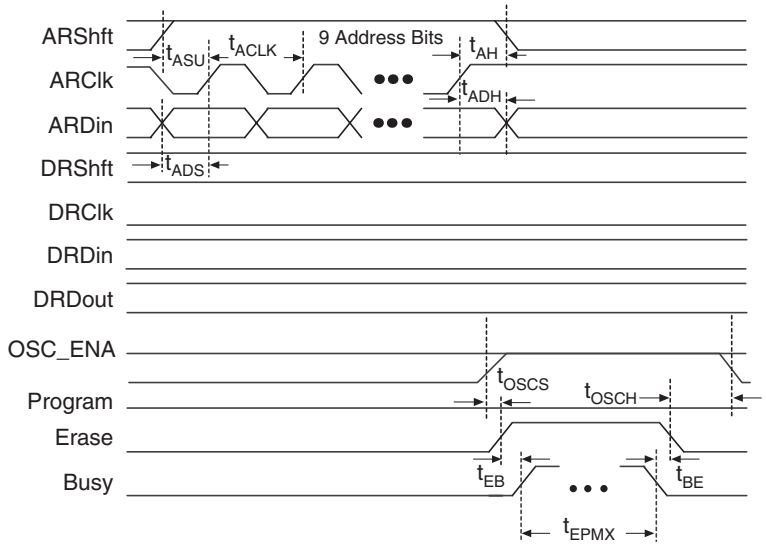


Table 5–22. Routing Delay Internal Timing Microparameters

Routing	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{C4}		369		480		591	ps
t_{R4}		456		593		730	ps
t_{LOCAL}		342		445		548	ps

External Timing Parameters

External timing parameters are specified by device density and speed grade. All external I/O timing parameters shown are for the 3.3-V LVTTL I/O standard with the maximum drive strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in Tables 5–27 through 5–31.

Table 5–23 shows the external I/O timing parameters for EPM240 devices.

Table 5–23. EPM240 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin to pin delay through 1 look-up table (LUT)	10 pF		4.7		6.2		7.6	ns
t_{PD2}	Best case pin to pin delay through 1 LUT	10 pF		3.8		4.9		6.0	ns
t_{SU}	Global clock setup time		1.6		2.1		2.6		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.3	2.0	5.6	2.0	6.9	ns
t_{CH}	Global clock high time		170		221		272		ps
t_{CL}	Global clock low time		170		221		272		ps
t_{CNT}	Minimum global clock period for 16-bit counter		3.3		4.0		4.9		ns
f_{CNT}	Maximum global clock frequency for 16-bit counter			304.0 *(1)*		249.9		202.9	MHz

Note to Table 5–23:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–24 shows the external I/O timing parameters for EPM570 devices.

Table 5–24. EPM570 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin to pin delay through 1 look-up table (LUT)	10 pF		5.5		7.1		8.8	ns
t_{PD2}	Best case pin to pin delay through 1 LUT	10 pF		3.7		4.8		6.0	ns
t_{SU}	Global clock setup time		1.4		1.9		2.3		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.5	2.0	5.9	2.0	7.2	ns
t_{CH}	Global clock high time		170		221		272		ps
t_{CL}	Global clock low time		170		221		272		ps
t_{CNT}	Minimum global clock period for 16-bit counter		3.3		4.0		4.9		ns
f_{CNT}	Maximum global clock frequency for 16-bit counter			304.0 *(1)*		249.9		202.9	MHz

Note to Table 5–24:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–25 shows the external I/O timing parameters for EPM1270 devices

Table 5–25. EPM1270 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin to pin delay through 1 look-up table (LUT)	10 pF		6.3		8.2		10.1	ns
t_{PD2}	Best case pin to pin delay through 1 LUT	10 pF		3.7		4.8		6.0	ns
t_{SU}	Global clock setup time		1.4		1.8		2.2		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.6	2.0	6.0	2.0	7.3	ns
t_{CH}	Global clock high time		170		221		272		ps
t_{CL}	Global clock low time		170		221		272		ps
t_{CNT}	Minimum global clock period for 16-bit counter		3.3		4.0		4.9		ns
f_{CNT}	Maximum global clock frequency for 16-bit counter			304.0 *(1)*		249.9		202.9	MHz

Note to Table 5–25:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–26 shows the external I/O timing parameters for EPM2210 devices.

Table 5–26. EPM2210 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin to pin delay through 1 look-up table (LUT)	10 pF		7.1		9.2		11.3	ns
t_{PD2}	Best case pin to pin delay through 1 LUT	10 pF		3.7		4.8		6.0	ns
t_{SU}	Global clock setup time		1.4		1.8		2.2		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.7	2.0	6.1	2.0	7.5	ns
t_{CH}	Global clock high time		170		221		272		ps
t_{CL}	Global clock low time		170		221		272		ps
t_{CNT}	Minimum global clock period for 16-bit counter		3.3		4.0		4.9		ns
f_{CNT}	Maximum global clock frequency for 16-bit counter			304.0 *(1)*		249.9		202.9	MHz

Note to Table 5–26:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

External Timing I/O Delay Adders

I/O delay timing parameters for I/O standard input and output adders and input delays are specified by speed grade independent of device density.

Tables 5–27 through 5–31 show the adder delays associated with I/O pins for all packages. If an I/O standard is selected other than LVTTL with a unit value of 16 mA and a fast slew rate, add the selected input delay adder to the external t_{SU} timing parameters shown in Tables 5–23 through 5–26. Add the output delay adder to the external t_{CO} and t_{PD} shown in Tables 5–23 through 5–26.

Table 5–27. External Timing Input Delay Adders

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger		0		0		0	ps
	With Schmitt Trigger		334		434		535	ps
3.3-V LVCMOS	Without Schmitt Trigger		0		0		0	ps
	With Schmitt Trigger		334		434		535	ps
2.5-V LVTTL	Without Schmitt Trigger		23		30		37	ps
	With Schmitt Trigger		339		441		543	ps
1.8-V LVTTL	Without Schmitt Trigger		291		378		466	ps
1.5-V LVTTL	Without Schmitt Trigger		681		885		1,090	ps
3.3-V PCI	Without Schmitt Trigger		0		0		0	ps

Table 5–28. External Timing Input Delay t_{GLOB} Adders for GCLK Pins

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger		0		0		0	ps
	With Schmitt Trigger		308		400		493	ps
3.3-V LVCMOS	Without Schmitt Trigger		0		0		0	ps
	With Schmitt Trigger		308		400		493	ps
2.5-V LVTTL	Without Schmitt Trigger		21		27		33	ps
	With Schmitt Trigger		423		550		677	ps
1.8-V LVTTL	Without Schmitt Trigger		353		459		565	ps
1.5-V LVTTL	Without Schmitt Trigger		855		1,111		1,368	ps
3.3-V PCI	Without Schmitt Trigger		6		7		9	ps

Table 5–29. External Timing Input Delay & t_{OD} Adders for Fast Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA		0		0		0	ps
	8 mA		65		84		104	ps
3.3-V LVCMOS	8 mA		0		0		0	ps
	4 mA		65		84		104	ps
2.5-V LVTTL	14 mA		122		158		195	ps
	7 mA		193		251		309	ps
1.8-V LVTTL	6 mA		568		738		909	ps
	3 mA		654		850		1,046	ps
1.5-V LVTTL	4 mA		1,059		1,376		1,694	ps
	2 mA		1,167		1,517		1,867	ps
3.3-V PCI	20 mA		3		4		5	ps

Table 5–30. External Timing Output Delay & t_{OD} Adders for Slow Slew Rate

Standard		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA		5,710		5,391		5,072	ps
	8 mA		6,445		6,126		5,807	ps
3.3-V LVCMOS	8 mA		5,710		5,391		5,072	ps
	4 mA		6,445		6,126		5,807	ps
2.5-V LVTTL	14 mA		8,518		8,199		7,880	ps
	7 mA		9,446		9,127		8,808	ps
3.3-V PCI	20 mA		261		339		418	ps

Table 5–31. MAX II IOE Programmable Delays

Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Increase_input_delay_to_internal_cells=ON		1,837		2,388		2,939	ps
Increase_input_delay_to_internal_cells=OFF		214		278		342	ps

Maximum Input & Output Clock Rates

Tables 5–32 and 5–33 show the maximum input and output clock rates for standard I/O pins in MAX II devices.

Table 5–32. MAX II Maximum Input Clock Rate for I/O (Part 1 of 2)

Standard		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
3.3-V LVTTL	Without Schmitt Trigger	304	304	304	MHz
	With Schmitt Trigger	250	250	250	MHz
3.3-V LVCMOS	Without Schmitt Trigger	304	304	304	MHz
	With Schmitt Trigger	250	250	250	MHz
2.5-V LVTTL	Without Schmitt Trigger	220	220	220	MHz
	With Schmitt Trigger	188	188	188	MHz
2.5-V LVCMOS	Without Schmitt Trigger	220	220	220	MHz
	With Schmitt Trigger	188	188	188	MHz

Table 5–32. MAX II Maximum Input Clock Rate for I/O (Part 2 of 2)

Standard		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.8-V LVTTL	Without Schmitt Trigger	200	200	200	MHz
1.8-V LVCMOS	Without Schmitt Trigger	200	200	200	MHz
1.5-V LVCMOS	Without Schmitt Trigger	150	150	150	MHz
3.3-V PCI	Without Schmitt Trigger	304	304	304	MHz

Table 5–33. MAX II Maximum Output Clock Rate for I/O

Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
3.3-V LVTTL	304	304	304	MHz
3.3-V LVCMOS	304	304	304	MHz
2.5-V LVTTL	220	220	220	MHz
2.5-V LVCMOS	220	220	220	MHz
1.8-V LVTTL	200	200	200	MHz
1.8-V LVCMOS	200	200	200	MHz
1.5-V LVCMOS	150	150	150	MHz
3.3-V PCI	304	304	304	MHz

JTAG Timing Specifications

Figure 5–5 shows the timing waveforms for the JTAG signals.

Figure 5–5. MAX II JTAG Timing Waveforms

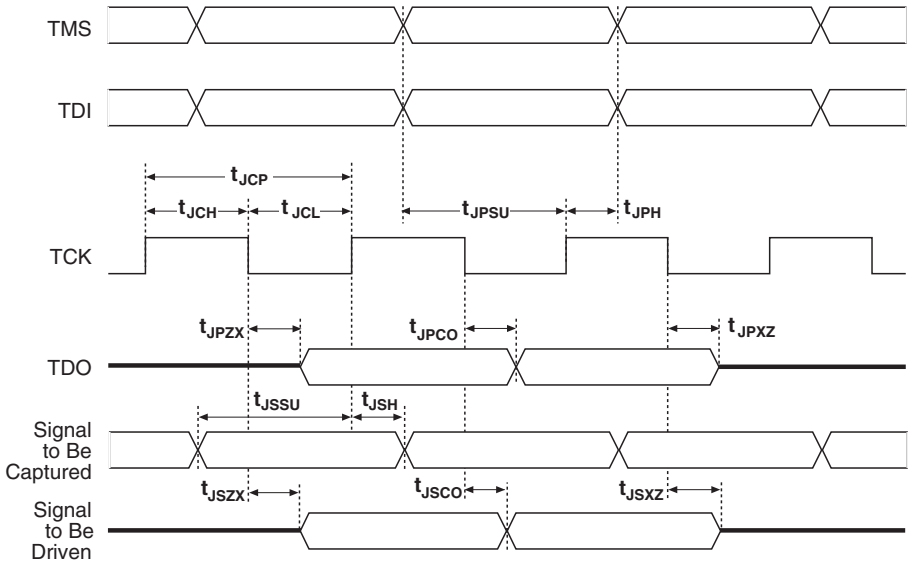


Table 5–34 shows the JTAG Timing parameters and values for MAX II devices.

Table 5–34. MAX II JTAG Timing Parameters (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JCP} *(1)*	TCK clock period for V_{CCIO1} = 3.3 V	55.5		ns
	TCK clock period for V_{CCIO1} = 2.5 V	62.5		ns
	TCK clock period for V_{CCIO1} = 1.8 V	100		ns
	TCK clock period for V_{CCIO1} = 1.5 V	143		ns
t_{JCH}	TCK clock high time	20		ns
t_{JCL}	TCK clock low time	20		ns
t_{JPSU}	JTAG port setup time *(2)*	8		ns
t_{JPH}	JTAG port hold time	10		ns

Table 5–34. MAX II JTAG Timing Parameters (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JPCO}	JTAG port clock to output *(2)*		15	ns
t_{JPZX}	JTAG port high impedance to valid output *(2)*		15	ns
t_{JPXZ}	JTAG port valid output to high impedance *(2)*		15	ns
t_{JSSU}	Capture register setup time	8		ns
t_{JSH}	Capture register hold time	10		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

Notes to Table 5–34:

(1) Minimum clock period specified for 10 pF load on the TDO pin. Larger loads on TDO will degrade the maximum TCK frequency.

(2) This specification is shown for 3.3-V LVTTL/LVCMOS and 2.5-V LVTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the t_{JPSU} minimum is 6 ns and t_{JPCO}, t_{JPZX}, and t_{JPXZ} are maximum values at 35 ns.

Chapter 6. Reference & Ordering Information

MII51006-1.0

Software

MAX® II devices are supported by the Altera® Quartus® II design software with new, optional MAX+PLUS® II look and feel, which provides HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, and device programming. See the *Design Software Selector Guide* for more details on the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT, Sun Solaris, Linux Red Hat v8.0, and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

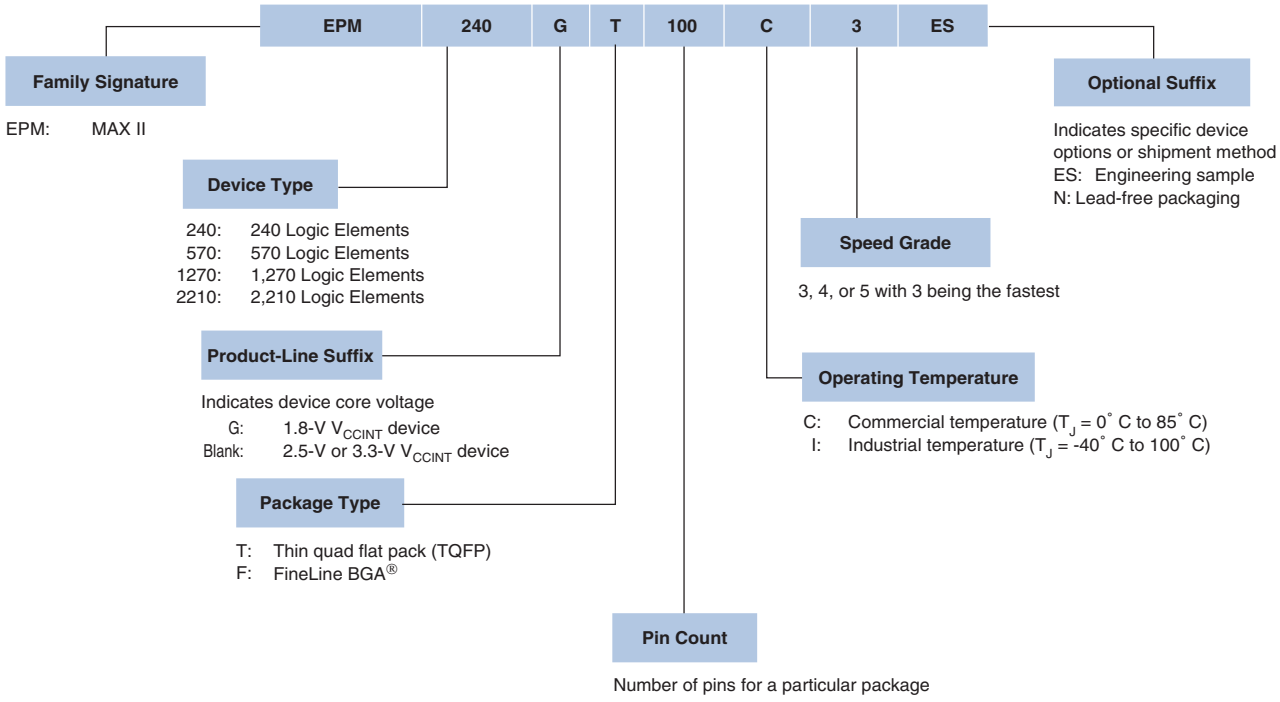
Device Pin-Outs

Printed device pin-outs for MAX II devices will be released on the Altera web site (**www.altera.com**) and in the MAX II Device Handbook when they are available.

Ordering Information

Figure 6–1 describes the ordering codes for MAX II devices. For more information on a specific package, refer to the chapter on *Package Information*.

Figure 6–1. MAX II Device Packaging Ordering Information



Dual Marking

On MAX II devices, packages display a dual marking for the -4 commercial and -5 industrial ordering codes. For example, both EPM570GT100C4 and EPM570GT100I5 ordering codes are marked on the same package.