FAIRCHILD
A Schlumberger Company

# DAC1408/1508 Series 8-Bit Multiplying D/A Converters

Linear Division Data Acquisition

## Description

The DAC1408/1508 Series are monolithic 8-bit multiplying digital-to-analog converters constructed using the Fairchild Planar Epitaxial process. It is designed for use where the output current is a linear product of an 8-bit digital word and an analog input voltage. The DAC1408/1508 Series are lead-for-lead replacements for the MC 1408 and SSS 1408 devices.

- **Relative Accuracy ±0.19% Error Maximum DAC1408A**
- **7 And 6-Bit Accuracy Available DAC1408B, DAC1408C**
- **Fast Settling Time To 1/2 LSB — 85 ns**
- **Non-inverting Digital Inputs are TTL And CMOS Compatible**
- **Output Voltage Swing +0.5 V to −5.0 V**
- **High-speed Multiplying Input Slew Rate 4.0 mA/μs**
- **Standard Supply Voltages +5.0 V And −5.0 V To −15 V**
- **Low Full Scale Current Drift +10 ppm/°C Typically**
- **Low Power Consumption 33 mW at ±5 V**
- **Low Cost**

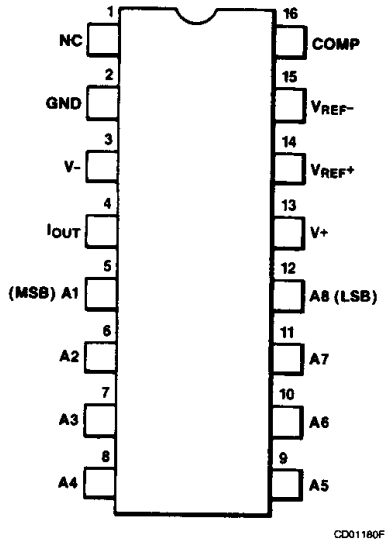
## Absolute Maximum Ratings

| | |
|---|---|
| Storage Temperature Range | |
| Ceramic DIP | −65°C to +175°C |
| Molded DIP | −65°C to +150°C |
| Operating Temperature Range | |
| Extended (DAC1508M) | −55°C to +125°C |
| Commercial (DAC1408C) | 0°C to +70°C |
| Lead Temperature | |
| Ceramic DIP (soldering, 60 s) | 300°C |
| Molded DIP (soldering, 10 s) | 265°C |
| Internal Power Dissipation[1, 2] | |
| 16L-Ceramic DIP | 1.50 W |
| 16L-Molded DIP | 1.04 W |
| V+ | 5.5 V |
| V− | −16.5 V |
| Digital Input Voltage (5 V to 12 V) | 5.5 V |
| Applied Output Voltage | 0.5 V to −5.2 V |
| Reference Current (I14) | 5.0 mA |
| Reference Amplifier Inputs ($V_{14}$, $V_{15}$) | 5.5 V, −16.5 V |

**Notes**

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Molded DIP at 8.3 mW/°C, the 16L-Ceramic DIP at 10 mw/°C.

## Connection Diagram
## 16-Lead DIP
## (Top View)

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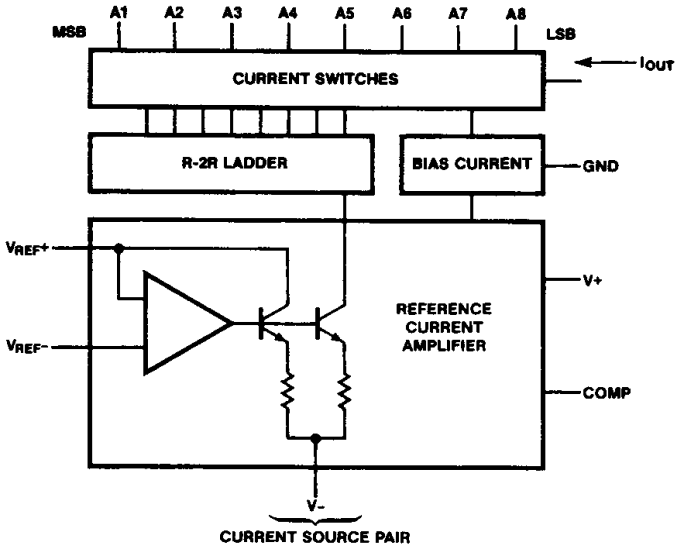
## Order Information

| Device Code | Package Code | Package Description |
|---|---|---|
| DAC1408ADC | 7B | Ceramic DIP |
| DAC1408APC | 9B | Molded DIP |
| DAC1408BDC | 7B | Ceramic DIP |
| DAC1408BPC | 9B | Molded DIP |
| DAC1408CDC | 7B | Ceramic DIP |
| DAC1408CPC | 9B | Molded DIP |
| DAC1508DM | 7B | Ceramic DIP |

## Equivalent Circuit

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**DAC1408/1508 Series**
**Electrical Characteristics** $T_A = 0°C$ to $70°C$ for the DAC1408, $-55°C$ to $+125°C$ for the DAC1508; $V+ = +5.0$ V, $V- = -15$ V, $V_{REF}/R14 = 2.0$ mA. All digital inputs at HIGH logic level.

| Symbol | Characteristic | Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $E_r$ | Relative Accuracy (Error Relative to Full Scale $I_O$) | DAC1408A/DAC1508 | | | | ±0.19 | % |
| | | DAC1408B[1] | | | | ±0.39 | |
| | | DAC1408C[1] | | | | ±0.78 | |
| $t_S$ | Settling Time to Within ½ LSB (Includes $t_{PLH}$) | $T_A = 25°C$[2] | | | 85 | 135 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay | $T_A = 25°C$ | | | 30 | 100 | ns |
| $TCI_O$ | Output Full Scale Current Drift | | | | ±20 | | ppm/°C |
| $V_{IH}$ | Logic Input Voltage HIGH | | | 2.0 | | | V |
| $V_{IL}$ | Logic Input Voltage LOW | | | | | 0.8 | |
| $I_{IH}$ | Logic Input Current HIGH | $V_{IH} = 5.0$ V | | | 0 | 0.04 | mA |
| $I_{IL}$ | Logic Input Current LOW | $V_{IL} = 0.8$ V | | | −0.4 | −0.8 | |
| $I_{I5}$ | Reference Input Bias Current | | | | −1.0 | −5.0 | μA |
| $I_{OR}$ | Output Current Range | $V- = -5.0$ V | | 0 | 2.0 | 2.1 | mA |
| | | $V- = -6.0$ to $-15$ V | | 0 | 2.0 | 4.2 | |
| $I_O$ | Output Current | $V_{REF} = 2.000$ V, R14 = 1.0 kΩ | | 1.9 | 1.99 | 2.1 | mA |
| $I_{O\ Min}$ | Output Current | All bits LOW | | | 0 | 4.0 | μA |
| $V_{OC}$ | Output Voltage Compliance | $E_r \leq 0.19\%$ at $T_A = 25°C$ | $V- = -5.0$ V | | | −0.55, +0.4 | V |
| | | | V− below −10 V | | | −5.0, +0.5 | |
| dI/dt | Reference Current Slew Rate | | | | 4.0 | | mA/μs |
| PSRR (−) | Output Current Supply Sensitivity | | | | 0.5 | 2.7 | μA/V |
| I+ | Supply Current | All bits LOW | | | +13.5 | +22 | mA |
| I− | | | | | −7.5 | −13 | |
| $V_R+$ | Power Supply Voltage Range | $T_A = 25°C$ | | +4.5 | +5.0 | +5.5 | V |
| $V_R-$ | | | | −4.5 | −15 | −16.5 | |
| $P_c$ | Power Consumption | All bits LOW, $V- = -5.0$ V | | | 105 | 170 | mW |
| | | All bits LOW, $V- = -15$ V | | | 190 | 305 | |
| | | All bits HIGH, $V- = -5.0$ V | | | 90 | | |
| | | All bits HIGH, $V- = -15$ V | | | 160 | | |

**Notes**
1. All current switches are tested to guarantee at least 50% of rated output current.
2. All bits switched.

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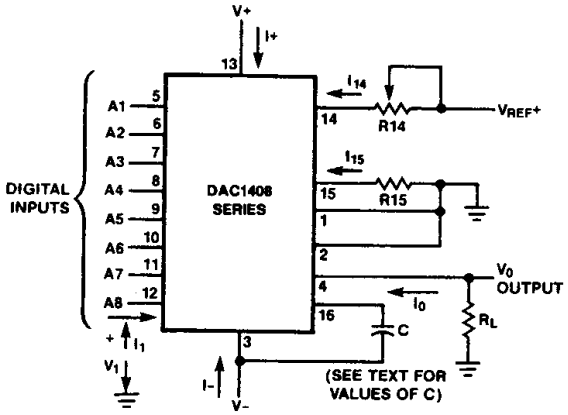
## Test Circuits

### Figure 1 Notation Definitions




Typical values: R14 = R15 = 1 k
$V_{REF}$ = +20 V
C = 15 pF

$V_1$ and $I_1$ apply to inputs A1 thru A8

The resistor tied to lead 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

where $K \approx \frac{V_{REF}}{R14}$

and $A_n$ = "1" if $A_n$ is at HIGH level
$A_n$ = "0" if $A_n$ is at LOW level

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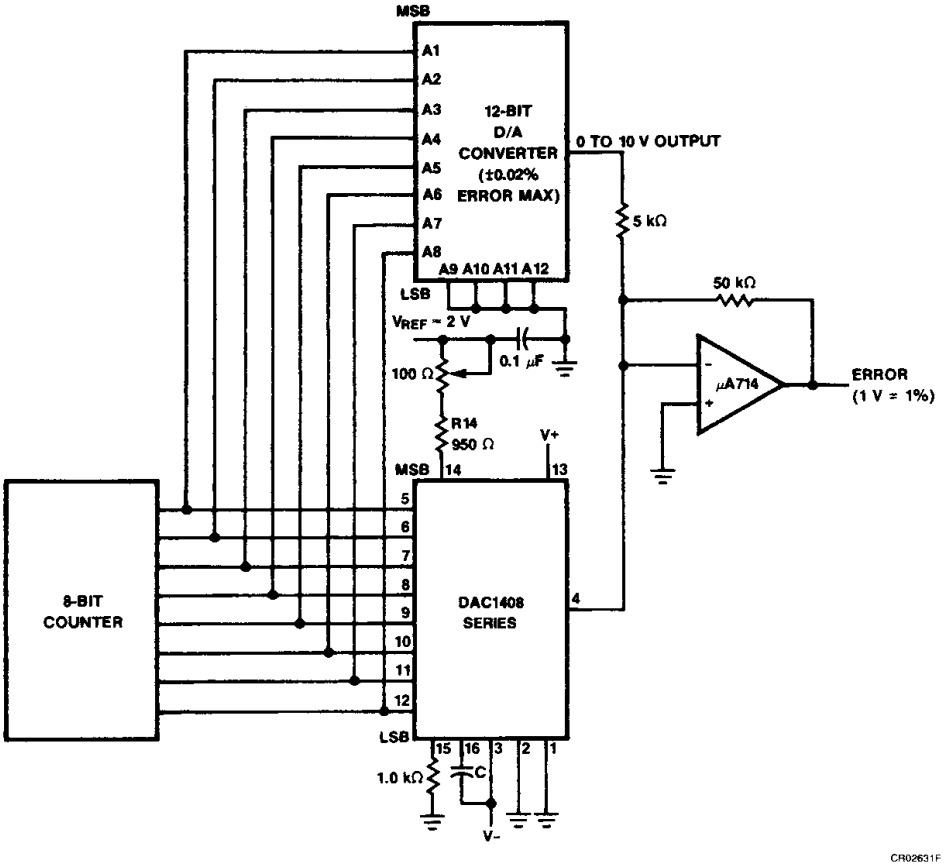
### Figure 2 Relative Accuracy Test Circuit

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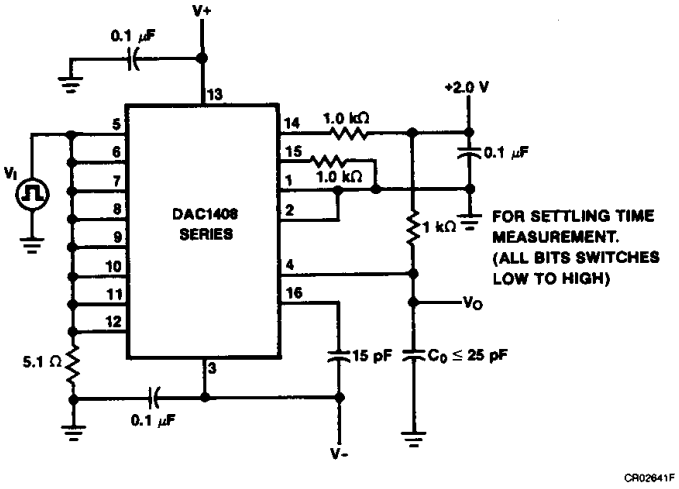
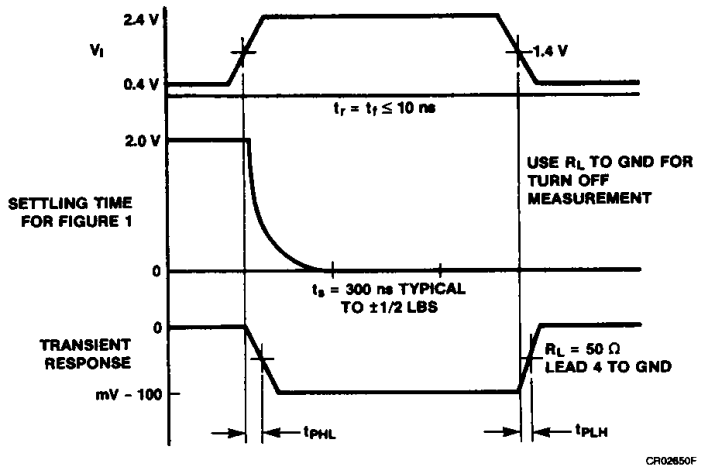
## Test Circuits (Cont.)

**Figure 3 Transient Response and Settling Time**

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## Applications

- Tracking a/d Converters
- Successive Approximation a/d Converters
- 2 1/2 Digit Panel Meters and DVMs
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

## Applications (Cont.)

**Figure 4 Positive $V_{REF}$**

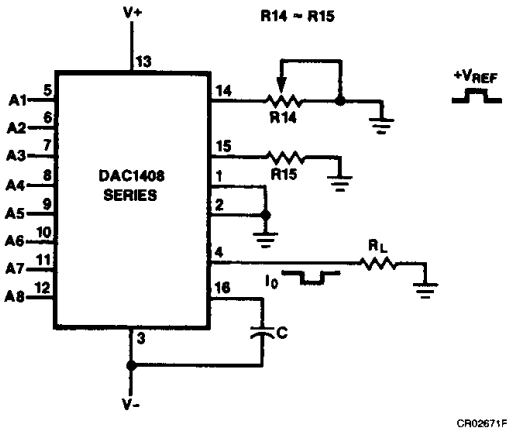



**Figure 5 Negative $V_{REF}$**

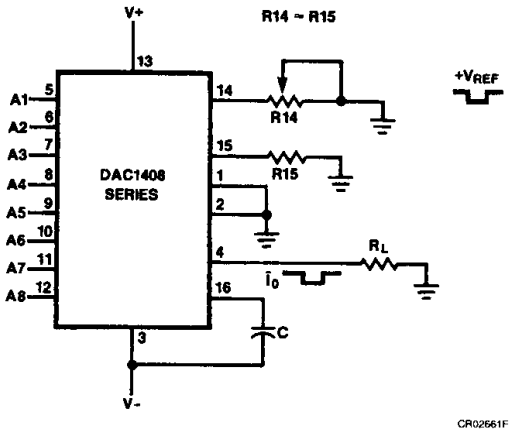
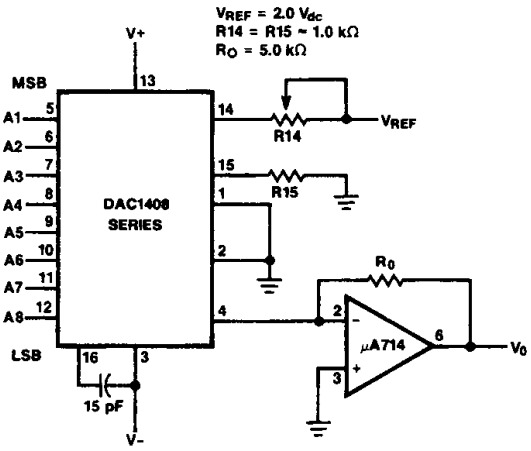



**Figure 6 Use with Current-to-Voltage Converting OP AMP**




**Theoretical $V_O$**

$$V_O = \frac{V_{REF}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust $V_{REF}$ R14 or $R_O$ so that $V_O$ with all digital inputs at HIGH level is equal to 9.961 Volts.

$$V_O = \frac{2\,V}{1\,k}(5\,k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\,V\,\frac{255}{256} = 9.961\,V$$

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