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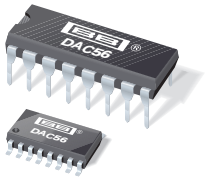


DAC56

Monolithic 16-Bit Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
  Internal Voltage Reference
  ±3V Output Operational Amplifier
  Pinout Allows I_{OUT} (±1.0mA) Option
  No external components required
- 0.012% LINEARITY ERROR MAX
- 12-BIT MONOTONICITY GUARANTEED OVER 0°C TO +70°C
- ±5V TO ±12V POWER SUPPLY
- SETTLING TIME: V_{OUT} = 1.5µs;
  I_{OUT} = 350ns
- SERIAL DATA INPUT: Binary Two's Complement
- 16-PIN PLASTIC DIP AND SOIC

APPLICATIONS

- PROCESS CONTROL
- ATE PIN ELECTRONICS LEVEL SETTING
- CLOSED-LOOP SERVO-CONTROL
- AUTO-CALIBRATION CIRCUIT FOR A/D BOARDS
- UP-GRADE REPLACEMENT FOR MULTIPLYING D/A
- X-Y PLOTTER
- DSP PROCESSOR BOARDS

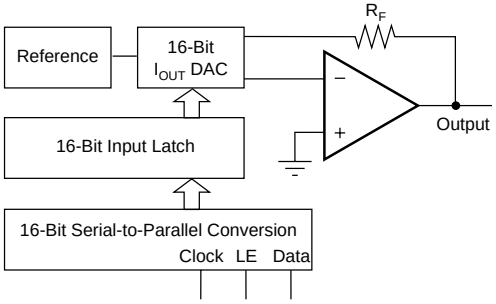
DESCRIPTION

The DAC56 is a complete 16-bit monolithic D/A converter. Completely self-contained with a stable, low noise, internal zener voltage reference; high-speed current switches; a resistor ladder network; and a low noise output operational amplifier all on a single monolithic chip. The DAC56 operates over a wide power supply range from ±5V to ±12V.

Differential linearity error (DLE) is guaranteed to meet specifications without external adjustment. However, provisions for an externally adjustable circuit controlling the MSB error, the differential linearity error at bipolar zero, makes the DLE at BPZ essentially zero and provides for high system performance. The I/V amplifier stage includes an output current limiting circuit to protect both amplifier and load from excessive current. This assures the user of high system reliability.

A high-speed interface is capable of clocking in data at a rate of 10MHz max, and its interface logic contains a serial data clock (input), serial data (input) and latch-enable (input). Serial data is clocked MSB first into a 16-bit register and then latched into a 16-bit parallel register.

The DAC56 is packaged in a 16-pin plastic DIP and 16-pin SOIC.



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SPECIFICATIONS

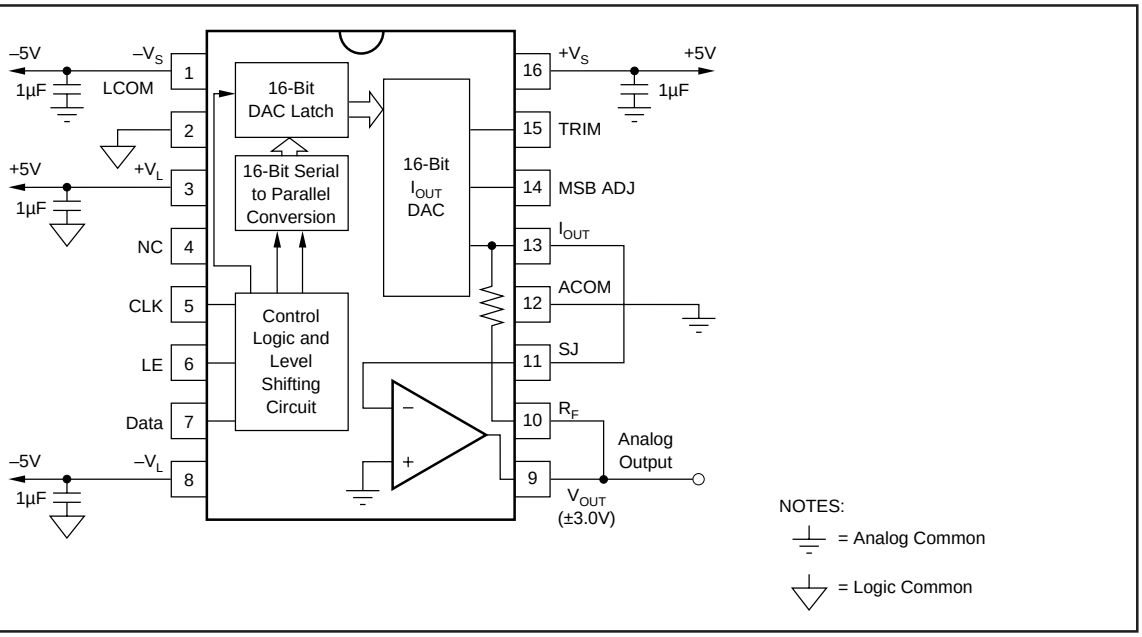
ELECTRICAL

All specifications at +25°C, and power supply voltage of ±5V, unless otherwise noted.

PARAMETER	CONDITIONS	DAC56 MIN	DAC56 TYP	DAC56 MAX	UNITS
DIGITAL INPUT					
Resolution			16		Bits
Digital Input Level: [1] V_{IH}		+2.4		$+V_L$	V
V_{IL}		0		+0.8	V
$I_{IH} \bullet V_I = +2.7V$				+1	µA
$I_{IL} \bullet V_I = +0.4V$				–50	µA
Input Clock Frequency		10			MHz
ACCURACY					
Integral Linearity Error				±0.012	% of FSR[3]
Differential Linearity Error				±0.024	% of FSR
Gain Error				±1.5	% of FSR
Bipolar Zero Error				±0.5	% of FSR
Monotonicity	0°C to +70°C			12	Bits
TEMPERATURE DRIFT	0°C to +70°C				
Gain Drift			±60		ppm of FSR/°C
Bipolar Zero Drift			±20		ppm of FSR/°C
Linearity Drift				±0.012	% of FSR
Differential Linearity Drift				±0.024	% of FSR
POWER SUPPLY SENSITIVITY	$\pm V_S = \pm V_L = \pm 5VDC$				
Gain			±0.0045		% of FSR/%V
Bipolar Zero			±0.0015		% of FSR/%V
SETTLING TIME	to ±0.006% of FSR				
Voltage Output					
6V Step			1.5		µs
1LSB			1		µs
Current Output					
1mA Step	10 to 100Ω Load		350		ns
	1kΩ Load[3]		350		ns
Slew Rate			12		V/µs
ANALOG OUTPUT					
Voltage Output Configuration					
Bipolar Range		±2.66	±3.0	±3.34	V
Output Current		±8			mA
Output Impedance			0.1		Ω
Short Circuit Duration			Indefinite to Common		
Current Output Configuration					
Bipolar Range			±1		mA
Output Impedance			1.2		kΩ
WARMUP TIME		1			min
POWER SUPPLY REQUIREMENTS[4]					
Supply Voltage					
$+V_S$ and $+V_L$		+4.75	+5.00	+13.2	V
$–V_S$ and $–V_L$		–4.75	–5.00	–13.2	V
Supply Drain (No Load)					
+V ($+V_S$ and $+V_L$ = +5V)			+10	+17	mA
–V ($–V_S$ and $–V_L$ = –5V)			–25	–35	mA
+V ($+V_S$ and $+V_L$ = +12V)			+12		mA
–V ($–V_S$ and $–V_L$ = –12V)			–27		mA
Power Dissipation					
V_S and V_L = ±5V			175	260	mW
V_S and V_L = ±12V			468		mW
TEMPERATURE RANGE					
Specification		0		70	°C
Storage		–60		100	°C

NOTES: (1) Logic input levels are TTL-/CMOS-compatible. (2) FSR means full-scale range and is equivalent to 6V (±3V) for DAC56 in the V_{OUT} mode. (3) Measured with an active clamp to provide a low impedance for approximately 200ns. (4) All specifications assume $+V_S$ connected to $+V_L$ and $–V_S$ connected to $–V_L$. If supplies are connected separately, $–V_L$ must not be more negative than $–V_S$ to assure proper operation. No similar restriction applies to the value of $+V_L$ with respect to $+V_S$.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	$-V_S$	Analog Negative Supply
2	LCOM	Logic Common
3	$+V_L$	Logic Positive Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	ACOM	Analog Common
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trim-pot Terminal
16	$+V_S$	Analog Positive Supply

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC56P	16-Pin Plastic DIP	180
DAC56U	16-Pin SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	±15VDC
Input Logic Voltage	–1V to $+V_S/+V_L$
Power Dissipation	850mW
Operating Temperature	–25°C to +70°C
Storage Temperature	–80°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

OPERATING INSTRUCTIONS

The accuracy of a D/A converter is described by the transfer function as shown in Figure 1. Digital input to analog output converter relationships are shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including gain, offset, linearity, differential linearity, and power supply sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and offset drift shifts the line left or right over the operating temperature range. Most of the offset and gain drift is due to the drift of the internal reference zener diode with temperature or time.

The converter is designed so that these drifts are in opposite directions. This way the bipolar zero voltage is virtually unaffected by variations in the reference voltage.

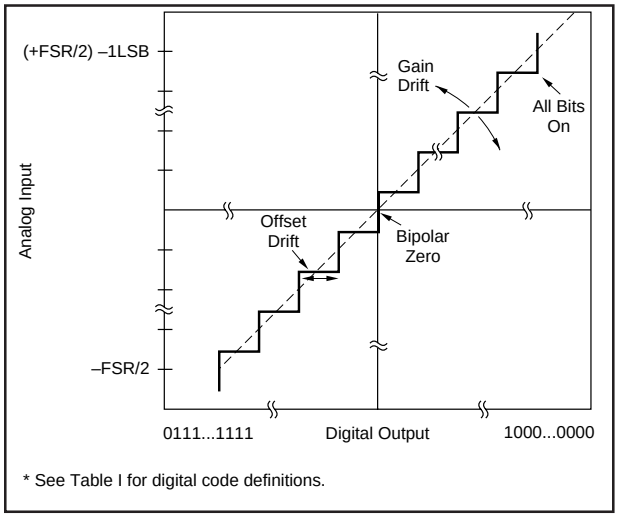


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V), V_{OUT} Mode	Current (mA), I_{OUT} Mode
$7FFF_H$	+ Full Scale	+2.999908	–0.999970
8000_H	– Full Scale	–3.000000	+1.000000
0000_H	Bipolar Zero	0.000000	0.000000
$FFFF_H$	Zero –1LSB	–0.000092	+0.030500µA

TABLE I. Digital Input to Analog Output Relationship.

DIGITAL INPUT CODES

The DAC56 accepts serial input data (MSB first) in Binary Two's Complement form—Refer to Table I for input/output relationships.

POWER SUPPLY CONNECTIONS

Power supply decoupling capacitors should be added as shown in the Connection Diagram (Figure 2), for optimum performance and noise rejection.

These capacitors (1µF tantalum recommended) should be connected as close as possible to the converter.

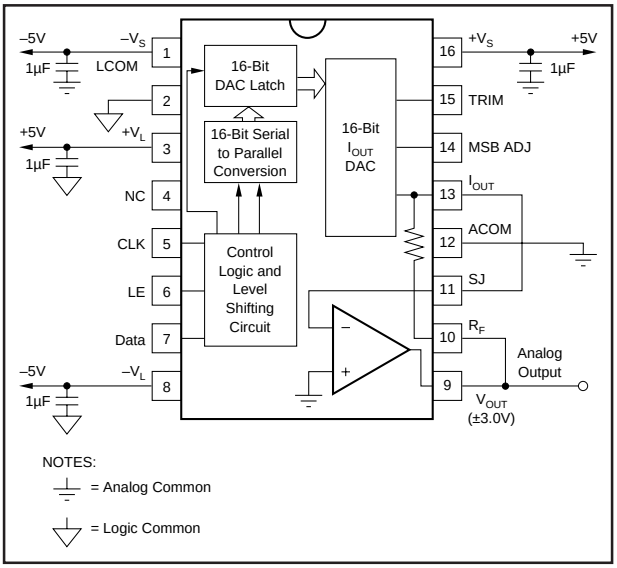


FIGURE 2. Connection Diagram.

MSB ERROR ADJUSTMENT (OPTIONAL)

Differential linearity error at all codes of the DAC56 is guaranteed to meet specifications without an external adjustment. However, if adjustment of the differential linearity error at bipolar zero is desired, it can be trimmed essentially to zero using the circuit as shown in Figure 3.

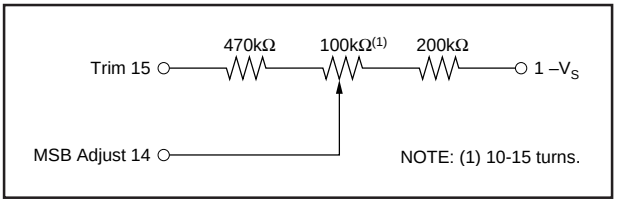
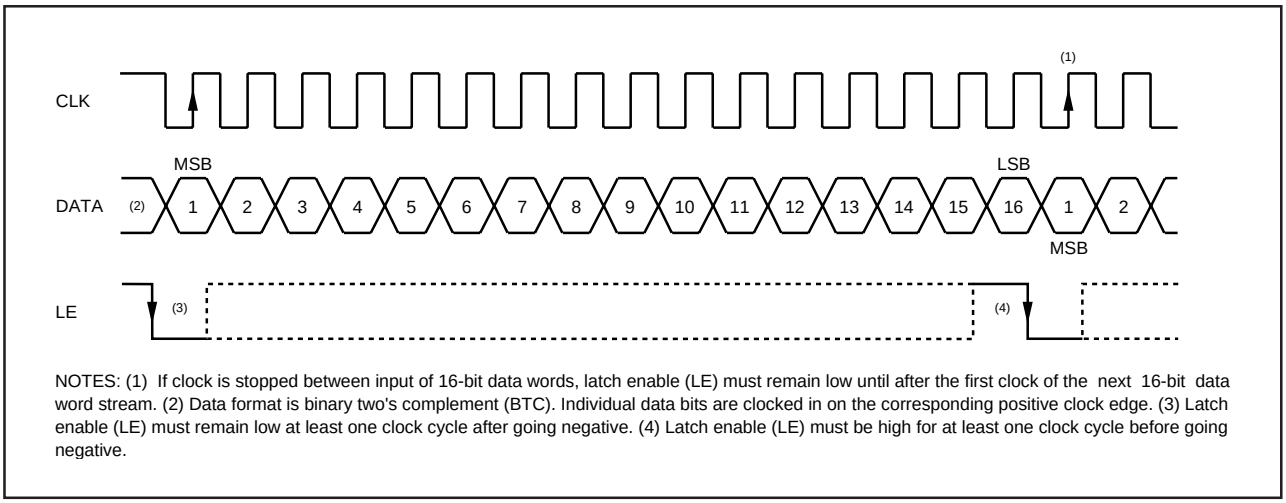


FIGURE 3. MSB Adjustment Circuit.

After allowing ample warm-up time (5 to 10 minutes) to assure stable operation, select the input code $FFFF_H$. Measure the output voltage using a 6-1/2 digit voltmeter and record the measurement. Change the digital input code to 0000_H. Adjust the 100kΩ potentiometer (TCR of 100ppm per °C or less is recommended) to make the output voltage read 1LSB more than the voltage reading of the previous code (ex. 1LSB = 92µV at FSR = 6V).

If the MSB adjustment circuit is not used, pins 14 and 15 should be left open.



NOTES: (1) If clock is stopped between input of 16-bit data words, latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 4. Input Timing Diagram.

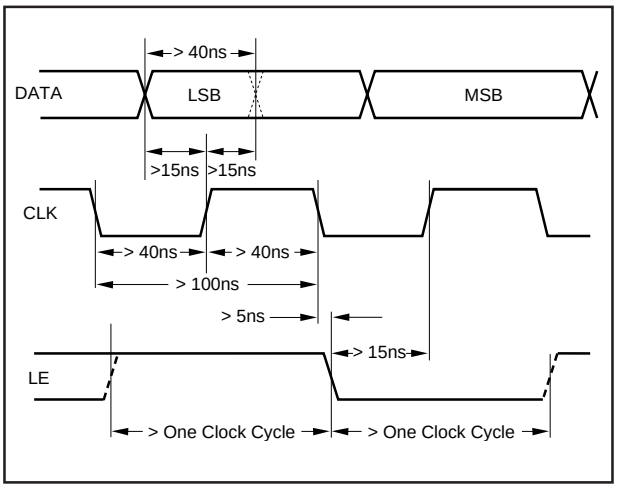


FIGURE 5. Input Timing Relationships.

INPUT TIMING CONSIDERATIONS

Figures 4 and 5 refer to the input timing required to interface the inputs of DAC56 to a serial input data stream. Serial data is accepted in Binary Two's Complement with the MSB being loaded first. Data is clocked in on positive going clock (CLK, pin 5) edges and is latched into the DAC input register on negative going latch enable (LE, pin 6) edges.

The latch enable input must be high for at least one clock cycle before going low, and then must be held low for at least one clock cycle. The last 16 data bits clocked into the serial input register are those that are transferred to the DAC input register when latch enable goes low. In other words, when more than 16 clock cycles occur between a latch enable, only the data present during the last 16 clocks will be transferred to the DAC input register.

Figure 4 gives the general input format required for the DAC56. Figure 5 shows the specific relationships between the various signals and their timing constraints.