Single Supply / Low Power / 256-tap / 2-Wire Bus

# X9279

## Single Digitally-Controlled (XDCP™) Potentiometer

### FEATURES

- 256 Resistor Taps
- 2-Wire Serial Interface for write, read, and transfer operations of the potentiometer
- Wiper Resistance, 100Ω typical @ 5V
- 16 Nonvolatile Data Registers for Each Potentiometer
- Nonvolatile Storage of Multiple Wiper Positions
- Power On Recall. Loads Saved Wiper Position on Power Up.
- Standby Current < 5µA Max
- $V_{CC}$: 2.7V to 5.5V Operation
- 50KΩ, 100KΩ versions of End to End Resistance
- Endurance: 100,000 Data Changes per Bit per Register
- 100 yr. Data Retention
- 14-Lead TSSOP, 16-Lead CSP (Chip Scale Package)
- Low Power CMOS

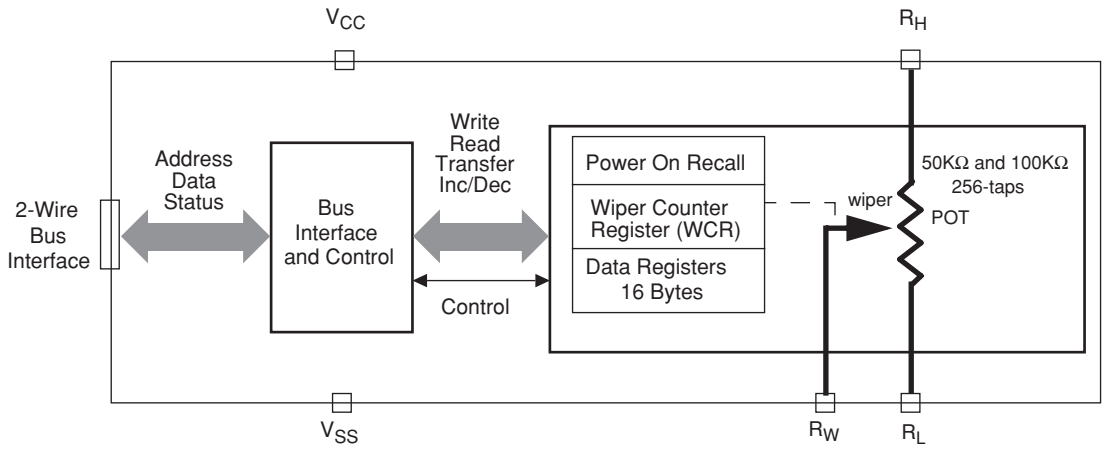
### DESCRIPTION

The X9279 integrates a single digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

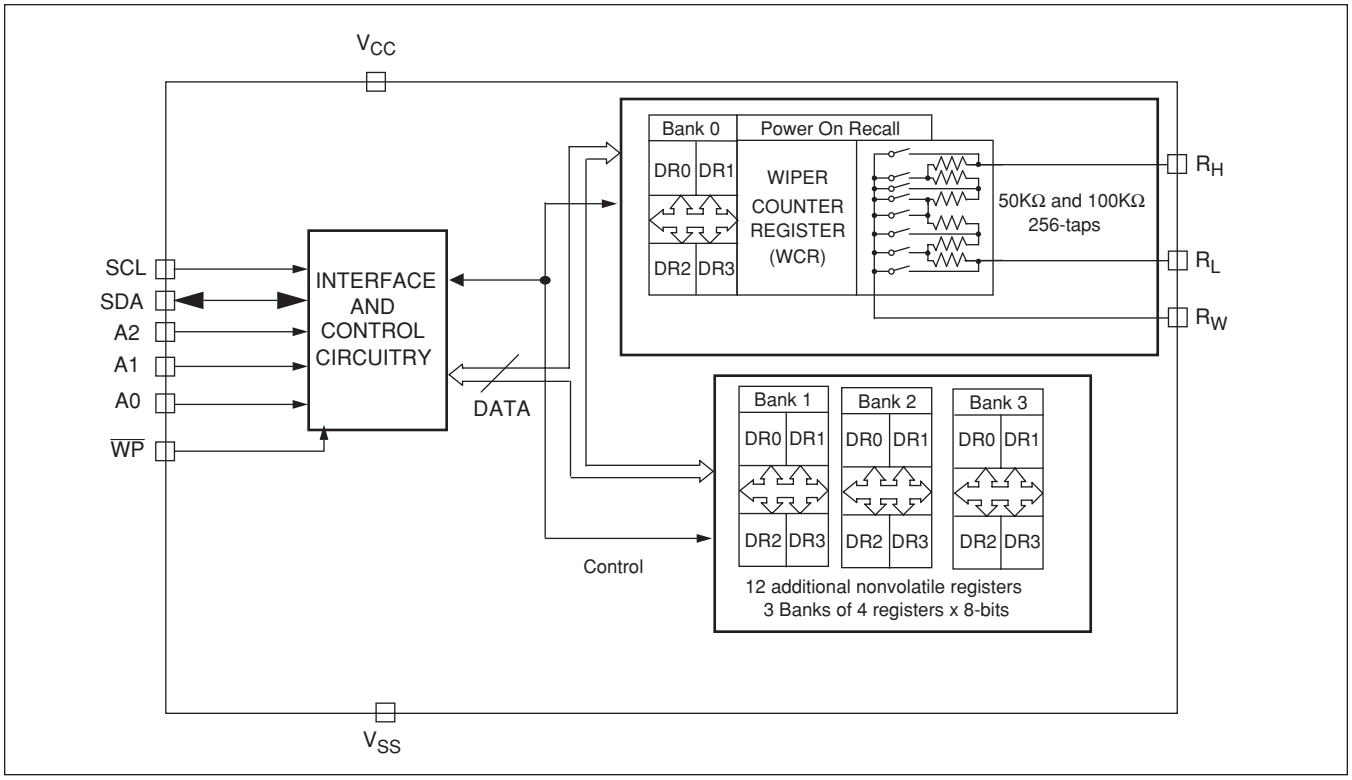
The digital controlled potentiometer is implemented using 255 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-Wire bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and a four nonvolatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array though the switches. Powerup recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

### FUNCTIONAL DIAGRAM



## DETAILED FUNCTIONAL DIAGRAM



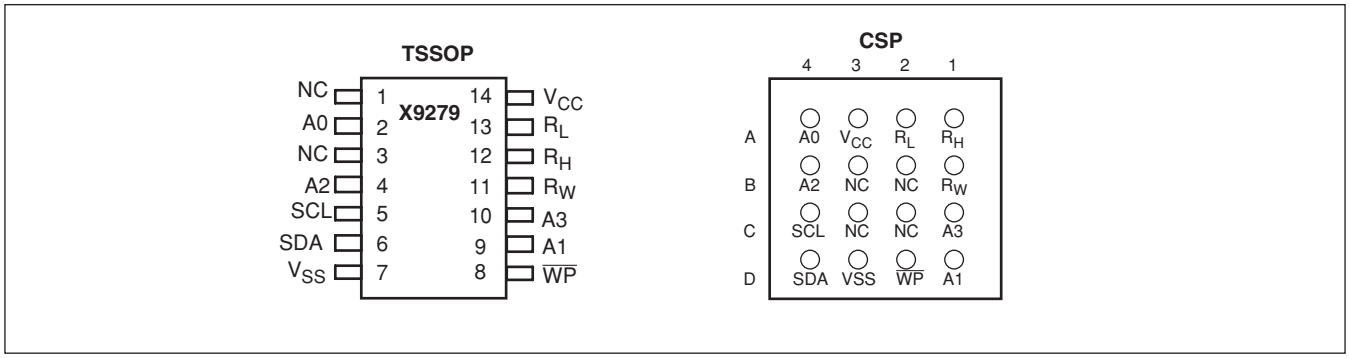

## CIRCUIT LEVEL APPLICATIONS

- Vary the gain of a voltage amplifier
- Provide programmable dc reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the dc biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

## SYSTEM LEVEL APPLICATIONS

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

## PIN CONFIGURATION




## PIN ASSIGNMENTS

| Pin TSSOP | Pin CSP | Symbol | Function |
|---|---|---|---|
| 1 | B2, B3 | NC | No Connect |
| 2 | A4 | A0 | Device Address for 2-Wire bus. |
| 3 | C2, C3 | NC | No Connect |
| 4 | B4 | A2 | Device Address for 2-Wire bus. |
| 5 | C4 | SCL | Serial Clock for 2-Wire bus. |
| 6 | D4 | SDA | Serial Data Input/Output for 2-Wire bus. |
| 7 | D3 | $V_{SS}$ | System Ground. |
| 8 | D2 | $\overline{WP}$ | Hardware Write Protect |
| 9 | D1 | A1 | Device Address for 2-Wire bus. |
| 10 | C1 | A3 | Device Address for 2 wire-bus. |
| 11 | B1 | $R_W$ | Wiper Terminal of the Potentiometer. |
| 12 | A1 | $R_H$ | High Terminal of the Potentiometer. |
| 13 | A2 | $R_L$ | Low Terminal of the Potentiometer. |
| 14 | A3 | $V_{CC}$ | System Supply Voltage. |

## PIN DESCRIPTIONS

### Bus Interface Pins

#### Serial Data Input/Output (SDA)

The SDA is a bidirectional serial data input/output pin for a 2-Wire slave device and is used to transfer data into and out of the device. It receives device address, opcode, wiper register address and data sent from an 2-Wire master at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

#### Serial Clock (SCL)

This input is used by 2-Wire master to supply 2-Wire serial clock to the X9279.

#### Device Address (A2 - A0)

The Address inputs are used to set the least significant 3 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9279. A maximum of 8 devices may occupy the 2-Wire serial bus.

### Potentiometer Pins

#### $R_H$, $R_L$

The $R_H$ and $R_L$ pins are equivalent to the terminal connections on a mechanical potentiometer.

#### $R_W$

The wiper pin is equivalent to the wiper terminal of a mechanical potentiometer.

### Bias Supply Pins

#### System Supply Voltage ($V_{CC}$) and Supply Ground ($V_{SS}$)

The $V_{CC}$ pin is the system supply voltage. The $V_{SS}$ pin is the system ground.

### Other Pins

#### No Connect

No connect pins should be left open. This pins are used for Xicor manufacturing and testing purposes.

#### Hardware Write Protect Input ($\overline{WP}$)

The $\overline{WP}$ pin when LOW prevents nonvolatile writes to the Data Registers.

## PRINCIPLES OF OPERATION

The X9279 is a integrated microcircuit incorporating a resistor array and associated registers and counter and the serial interface logic providing direct communication between the host and the digitally controlled potentiometers. This section provides detail description of the following:

**– Resistor Array Description.**

**– Serial Interface Description.**

**– Instruction and Register Description.**

### Array Description

The X9279 is comprised of a resistor array (see Figure 1). The array contains, in effect, 255 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer ($R_H$ and $R_L$ inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper ($R_W$) output. Within each individual array only one switch may be turned on at a time.

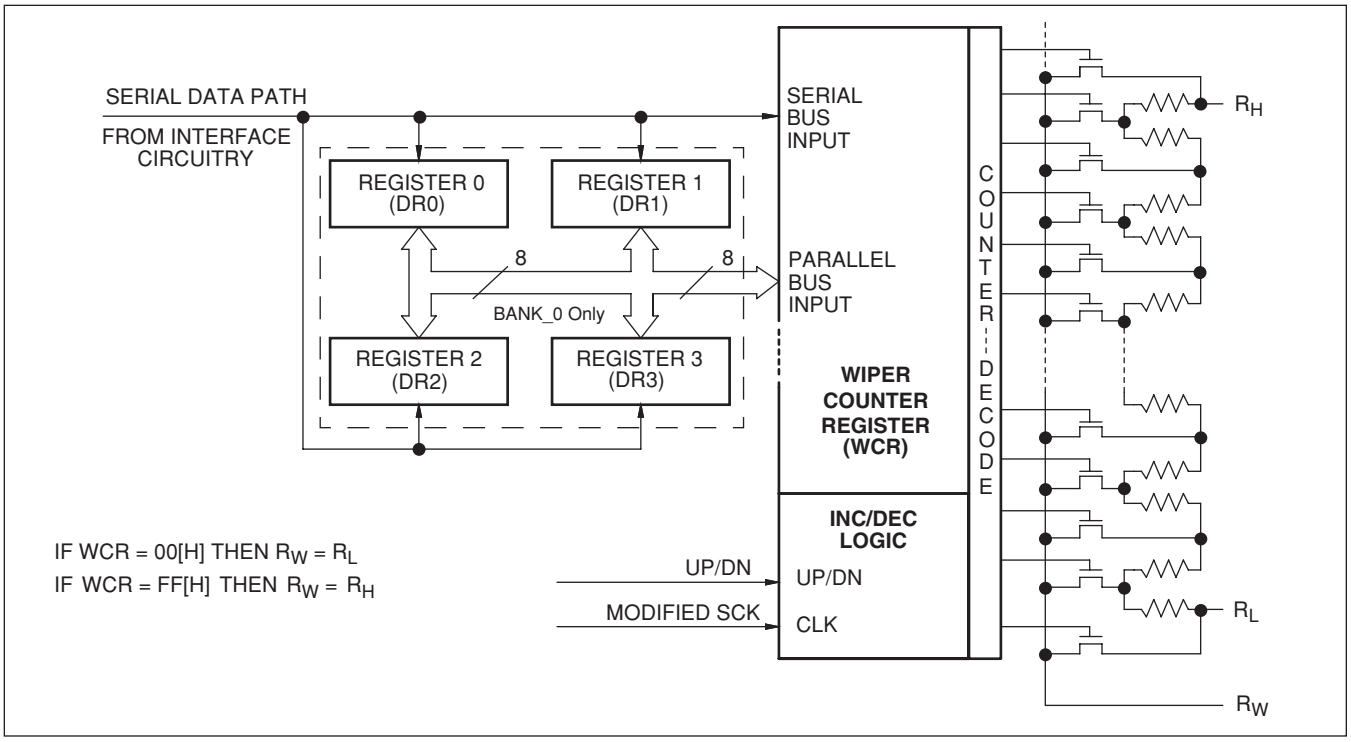
These switches are controlled by a Wiper Counter Register (WCR). The 8-bits of the WCR (WCR[7:0]) are decoded to select, and enable, one of 256 switches (see Table 1).

The WCR may be written directly. These Data Registers can the WCR can be read and written by the host system.

### Power Up and Down Recommendations.

There are no restrictions on the power-up or power-down conditions of $V_{CC}$ and the voltages applied to the potentiometer pins provided that $V_{CC}$ is always more positive than or equal to $V_H$, $V_L$, and $V_W$, i.e., $V_{CC} \geq V_H$, $V_L$, $V_W$. The $V_{CC}$ ramp rate specification is always in effect.

**Figure 1. Detailed Potentiometer Block Diagram**



## SERIAL INTERFACE DESCRIPTION

### Serial Interface

The X9279 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9279 will be considered a slave device in all applications.

### Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 2.

### Start Condition

All commands to the X9279 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The X9279 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met. See Figure 2.

### Stop Condition

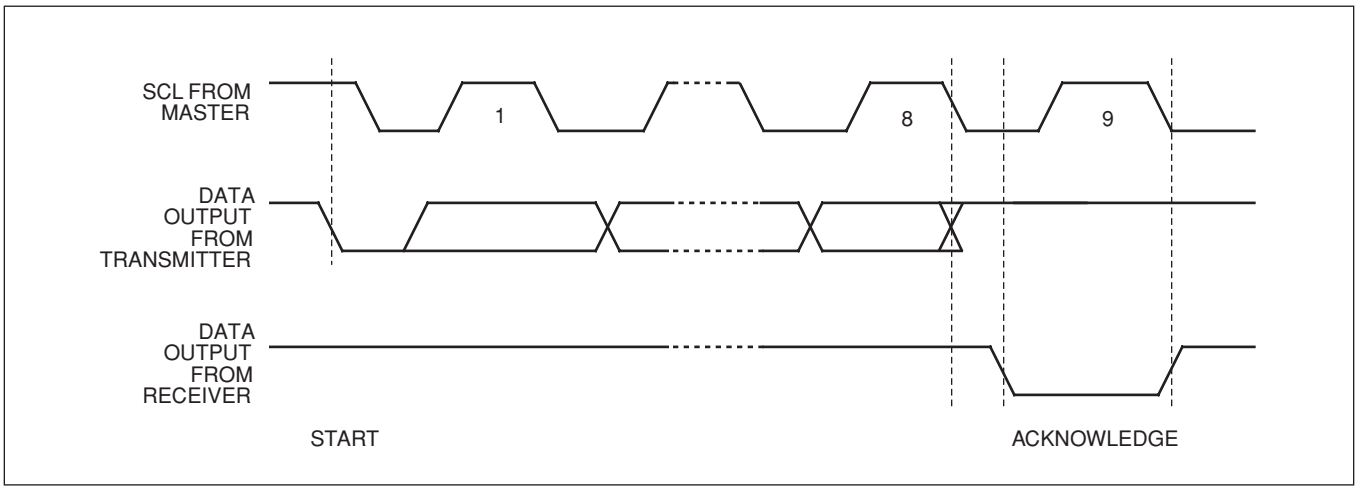
All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. See Figure 2.

### Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9279 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9279 will respond with a final acknowledge. See Figure 2.

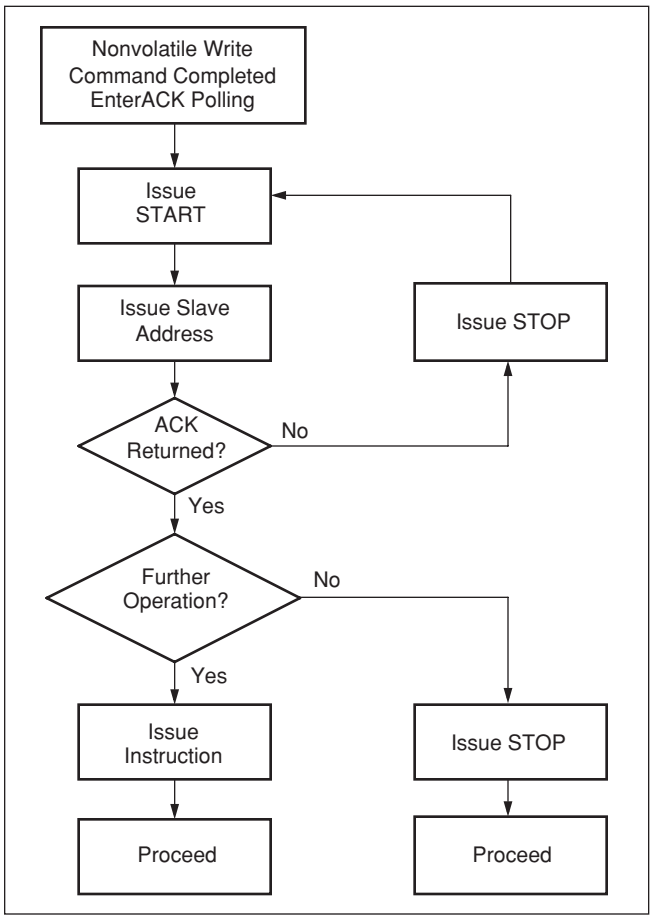
**Figure 2. Acknowledge Response from Receiver**



### Acknowledge Polling

The disabling of the inputs, during the internal nonvolatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9279 initiates the internal write cycle. ACK polling, Flow 1, can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9279 is still busy with the write operation no ACK will be returned. If the X9279 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

### FLOW 1: ACK Polling Sequence




## INSTRUCTION AND REGISTER DESCRIPTION

### Device Addressing: Identification Byte ( ID and A)

The first byte sent to the X9279 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the Identification byte. The most significant four bits of the slave address are a device type identifier. The ID[3:0] bits is the device ID for the X9279; this is fixed as 0101[B] (refer to Table 1).

The A[2:0] bits in the ID byte is the internal slave address. The physical device address is defined by the state of the A2-A0 input pins. The slave address is externally specified by the user. The X9279 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9279 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A2-A0 inputs can be actively driven by CMOS input signals or tied to $V_{CC}$ or $V_{SS}$.

### Instruction Byte (I)

The next byte sent to the X9279 contains the instruction and register pointer information. The three most significant bits are used provide the instruction opcode I [2:0]. The RB and RA bits point to one of the four Data Registers. P0 is the POT selection; since the X9279 is single POT, the P0=0. The format is shown in Table 2.

### Register Bank Selection (RB, RA, P1, P0)

There are 16 registers organized into four banks. Bank 0 is the default bank of registers. Only Bank 0 registers can be used for Data Register to Wiper Counter Register operations.

Banks 1, 2, and 3 are additional banks of registers (12 total) that can be used for 2-Wire write and read operations. The Data Registers in Banks 1, 2, and 3 cannot be used for direct read/write operations between the Wiper Counter Register.

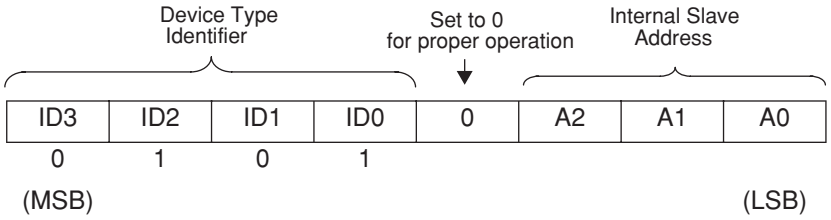
### Register Selection (R0 to R3) Table

| RB | RA | Register Selection | Operations |
|---|---|---|---|
| 0 | 0 | 0 | Data Register Read and Write; Wiper Counter Register Operations |
| 0 | 1 | 1 | Data Register Read and Write; Wiper Counter Register Operations |
| 1 | 0 | 2 | Data Register Read and Write; Wiper Counter Register Operations |
| 1 | 1 | 3 | Data Register Read and Write; Wiper Counter Register Operations |

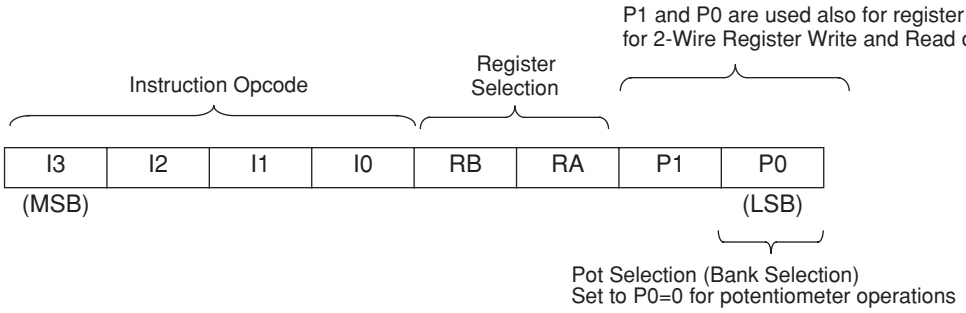
### Register Bank Selection (Bank 0 to Bank 3) Table

| P1 | P0 | Bank Selection | Operations |
|---|---|---|---|
| 0 | 0 | 0 | Data Register Read and Write; Wiper Counter Register Operations |
| 0 | 1 | 1 | Data Register Read and Write Only |
| 1 | 0 | 2 | Data Register Read and Write Only |
| 1 | 1 | 3 | Data Register Read and Write Only |

### Table 1. Identification Byte Format




### Table 2. Instruction Byte Format




**Register Selection**

| Register Selected | RB | RA |
|---|---|---|
| DR0 | 0 | 0 |
| DR1 | 0 | 1 |
| DR2 | 1 | 0 |
| DR3 | 1 | 1 |

**Table 3. Instruction Set**

| Instruction | Instruction Set | | | | | | | | Operation |
|---|---|---|---|---|---|---|---|---|---|
| | I3 | I2 | I1 | I0 | RB | RA | $P_1$ | $P_0$ | |
| Read Wiper Counter Register | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Read the contents of the Wiper Counter Register |
| Write Wiper Counter Register | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Write new value to the Wiper Counter Register |
| Read Data Register | 1 | 0 | 1 | 1 | 1/0 | 1/0 | 1/0 | 1/0 | Read the contents of the Data Register pointed to by P1-P0 and RB-RA |
| Write Data Register | 1 | 1 | 0 | 0 | 1/0 | 1/0 | 1/0 | 1/0 | Write new value to the Data Register pointed to by P1-P0 and RB-RA |
| XFR Data Register to Wiper Counter Register | 1 | 1 | 0 | 1 | 1/0 | 1/0 | 0 | 0 | Transfer the contents of the Data Register pointed to by RB-RA (Bank 0 only) to the Wiper Counter Register |
| XFR Wiper Counter Register to Data Register | 1 | 1 | 1 | 0 | 1/0 | 1/0 | 0 | 0 | Transfer the contents of the Wiper Counter Register to the Register pointed to by RB-RA (Bank 0 only) |
| Increment/Decrement Wiper Counter Register | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Enable Increment/decrement of the Wiper Counter Register |

**Note:** 1/0 = data is one or zero

## DEVICE DESCRIPTION

### Wiper Counter Register (WCR)

The X9279 contains contains a Wiper Counter Register, for the DCP potentiometer. The Wiper Counter Register can be envisioned as a 8-bit parallel and serial load counter with its outputs decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction (see Instruction section for more details). Finally, it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9279 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR0 value into the WCR. The DR0 value of Bank 0 is the default value.

### Data Registers (DR)

The potentiometer has four 8-bit nonvolatile Data Registers (DR3-DR0). These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Counter Register. All operations changing data in one of the Data Registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bit [7:0] are used to store one of the 256 wiper positions (0~255).

**Table 4. Wiper counter Register, WCR (8-bit), WCR[7:0]:** Used to store the current wiper position (Volatile, V).

| WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 |
|---|---|---|---|---|---|---|---|
| V | V | V | V | V | V | V | V |
| (MSB) | | | | | | | (LSB) |

**Table 5. Data Register, DR (8-bit), Bit [7:0]:** Used to store wiper positions or data (Nonvolatile, NV).

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| NV | NV | NV | NV | NV | NV | NV | NV |
| MSB | | | | | | | LSB |

## Instructions

Four of the seven instructions are three bytes in length. These instructions are:

– **Read Wiper Counter Register** – read the current wiper position of the potentiometer,

– **Write Wiper Counter Register** – change current wiper position of the potentiometer,

– **Read Data Register** – read the contents of the selected Data Register;

– **Write Data Register** – write a new value to the selected Data Register.

The basic sequence of the three byte instructions is illustrated in Figure 4. These three-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by $t_{WRL}$. A transfer from the WCR (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of $t_{WR}$ to complete. The transfer can occur between the potentiometer and one of its four associated registers (Bank 0).

Two instructions require a two-byte sequence to complete. These instructions transfer data between the host and the X9279; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

– **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the Wiper Counter Register.

– **XFR Wiper Counter Register to Data Register** – This transfers the contents of the Wiper Counter Register to the specified Data Register.

The final command is Increment/Decrement (Figure 5 and 6). The Increment/Decrement command is different from the other commands. Once the command is issued and the X9279 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse ($t_{HIGH}$) while SDA is HIGH, the selected wiper will move one resistor segment towards the $R_H$ terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the $R_L$ terminal.

See Instruction format for more details.

**Figure 3. Two-Byte Instruction Sequence**

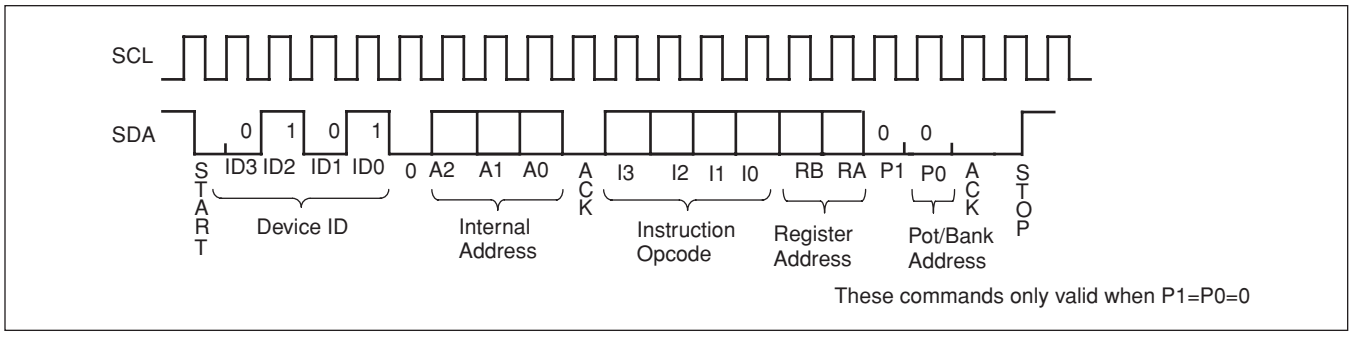


**Figure 4. Three-Byte Instruction Sequence**

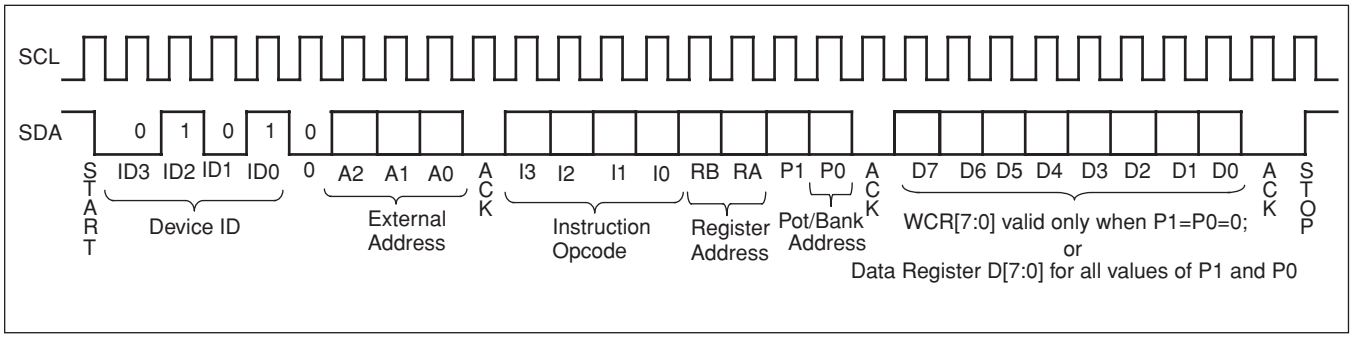



**Figure 5. Increment/Decrement Instruction Squence**

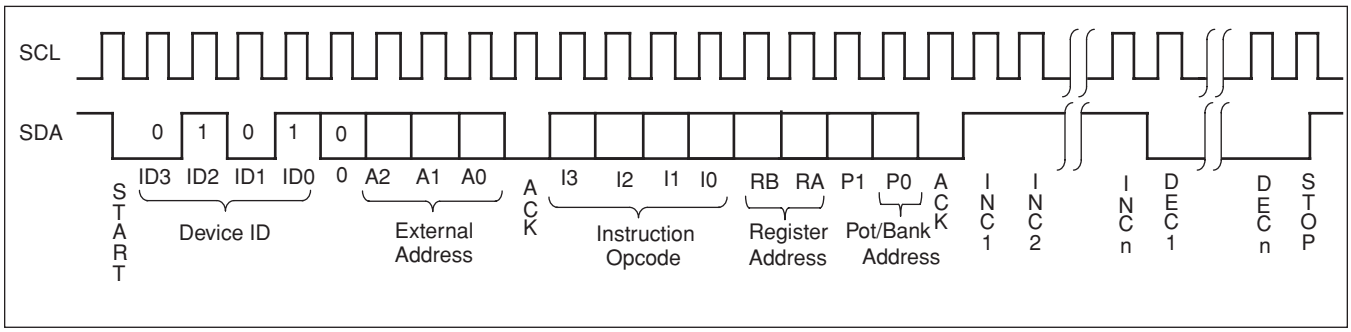
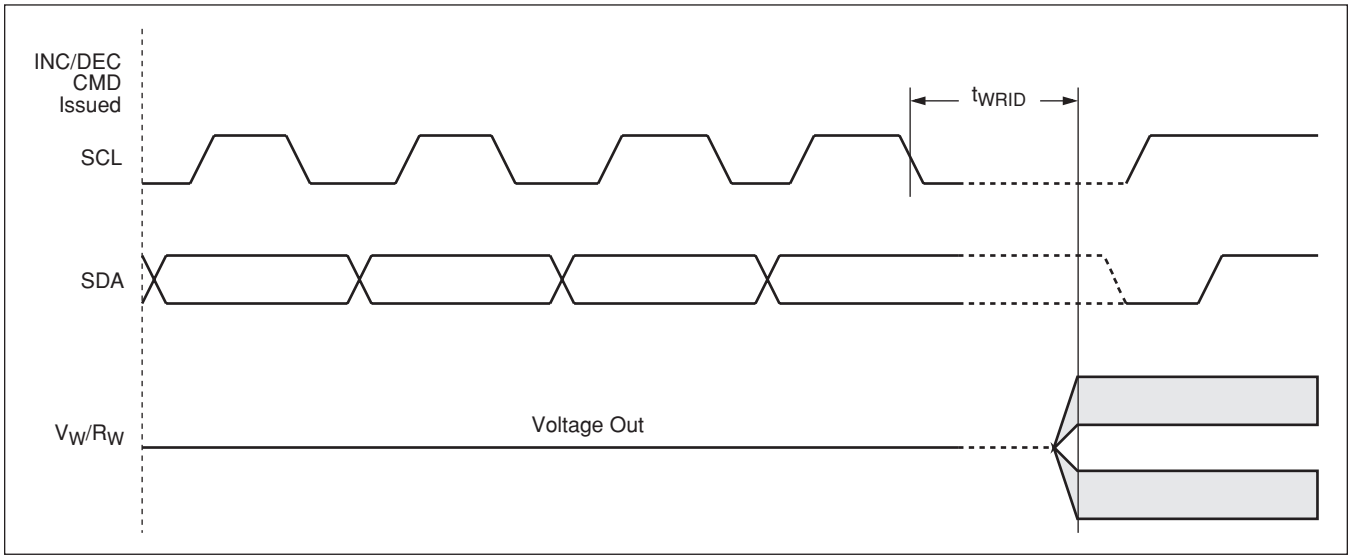



**Figure 6. Increment/Decrement Timing Limits**



## INSTRUCTION FORMAT

### Read Wiper Counter Register (WCR)

| START | Device Type Identifier | | | | Device Addresses | | | | SACK | Instruction Opcode | | | | DR/Bank Addresses | | | | SACK | Wiper Position (Sent by X9279 on SDA) | | | | | | | | MACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | A2 | A1 | A0 | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 | | |

### Write Wiper Counter Register (WCR)

| START | Device Type Identifier | | | | Device Addresses | | | | SACK | Instruction Opcode | | | | DR/Bank Addresses | | | | SACK | Wiper Position (Sent by Master on SDA) | | | | | | | | SACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | A2 | A1 | A0 | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 | | |

### Read Data Register (DR)

| START | Device Type Identifier | | | | Device Addresses | | | | SACK | Instruction Opcode | | | | DR/Bank Addresses | | | | SACK | Wiper Position (Sent by X9279 on SDA) | | | | | | | | MACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | A2 | A1 | A0 | | 1 | 0 | 1 | 1 | RB | RA | P1 | P0 | | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 | | |

### Write Data Register (DR)

| START | Device Type Identifier | | | | Device Addresses | | | | SACK | Instruction Opcode | | | | DR/Bank Addresses | | | | SACK | Wiper Position (Sent by Master on SDA) | | | | | | | | SACK | STOP | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | A2 | A1 | A0 | | 1 | 1 | 0 | 0 | RB | RA | P1 | P0 | | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 | | | HIGH-VOLTAGE WRITE CYCLE |

### Transfer Wiper Counter Register (WCR) to Data Register (DR)

| START | Device Type Identifier | | | | Device Addresses | | | | SACK | Instruction Opcode | | | | DR/Bank Addresses | | | | SACK | STOP | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | A2 | A1 | A0 | | 1 | 1 | 1 | 0 | RB | RA | 0 | 0 | | | HIGH-VOLTAGE WRITE CYCLE |

### Transfer Data Register (DR) to Wiper Counter Register (WCR)

| START | Device Type Identifier | | | | Device Addresses | | | | SACK | Instruction Opcode | | | | DR/Bank Addresses | | | | SACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | A 2 | A 1 | A 0 | | 1 | 1 | 0 | 1 | RB | RA | 0 | 0 | | |

### Increment/Decrement Wiper Counter Register (WCR)

| START | Device Type Identifier | | | | Device Addresses | | | | SACK | Instruction Opcode | | | | DR/Bank Addresses | | | | SACK | Increment/Decrement (Sent by Master on SDA) | | | | | | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | A 2 | A 1 | A 0 | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | I/D | I/D | . | . | . | I/D | I/D | |

**Notes:** (1) “MACK”/”SACK”: stands for the acknowledge sent by the master/slave.
(2) “A3 ~ A0”: stands for the device addresses sent by the master.
(3) “X”: indicates that it is a “0” for testing purpose but physically it is a “don’t care” condition.
(4) “I”: stands for the increment operation, SDA held high during active SCL phase (high).
(5) “D”: stands for the decrement operation, SDA held low during active SCL phase (high).

## ABSOLUTE MAXIMUM RATINGS

Temperature under bias .....–65°C to +135°C
Storage temperature .....–65°C to +150°C
Voltage on SCL, SDA any address input
with respect to $V_{SS}$.....–1V to +7V
$\Delta V = | (V_H – V_L) |$..... 5.5V
Lead temperature (soldering, 10 seconds)..... 300°C
$I_W$ (10 seconds)..... ±6mA

## COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Temp | Min. | Max. |
|---|---|---|
| Commercial | 0°C | +70°C |
| Industrial | –40°C | +85°C |

| Device | Supply Voltage ($V_{CC}$)(4) Limits |
|---|---|
| X9279 | 5V ±10% |
| X9279-2.7 | 2.7V to 5.5V |

## ANALOG CHARACTERISTICS (Over recommended industrial (2.7V) operating conditions unless otherwise stated.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | |
| $R_{TOTAL}$ | End to End Resistance | | 100 | | kΩ | T version |
| $R_{TOTAL}$ | End to End Resistance | | 50 | | kΩ | U version |
| | End to End Resistance Tolerance | | | ±20 | % | |
| | Power Rating | | | 50 | mW | 25°C, each pot |
| $I_W$ | Wiper Current | | | ±3 | mA | |
| $R_W$ | Wiper Resistance | | | 300 | Ω | $I_W$ = ± 3mA @ $V_{CC}$ = 3V |
| $R_W$ | Wiper Resistance | | | 150 | Ω | $I_W$ = ± 3mA @ $V_{CC}$ = 5V |
| $V_{TERM}$ | Voltage on any $R_H$ or $R_L$ Pin | $V_{SS}$ | | $V_{CC}$ | V | $V_{SS}$ = 0V |
| | Noise | | -120 | | dBV/$\sqrt{Hz}$ | Ref: 1V |
| | Resolution | | 0.4 | | % | |
| | Absolute Linearity (1) | | | ±1 | MI(3) | $R_{w(n)(actual)} – R_{w(n)(expected)}$(5) |
| | Relative Linearity (2) | | | ±0.2 | MI(3) | $R_{w(n+1)} – [R_{w(n)} + MI]$(5) |
| | Temperature Coefficient of $R_{TOTAL}$ | | ±300 | | ppm/°C | |
| | Ratiometric Temp. Coefficient | | | 20 | ppm/°C | |
| $C_H/C_L/C_W$ | Potentiometer Capacitances | | 10/10/25 | | pF | See Macro model |

**Notes:** (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT / 255 or ($R_H – R_L$) / 255, single pot
(4) During power up $V_{CC} > V_H$, $V_L$, and $V_W$.
(5) n = 0, 1, 2, ....,255; m =0, 1, 2, ...., 254.

## D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | |
| $I_{CC1}$ | $V_{CC}$ supply current (active) | | | 3 | mA | $f_{SCL}$ = 400KHz; $V_{CC}$ = +6V; SDA = Open; (for 2-Wire, Active, Read and |
| $I_{CC2}$ | $V_{CC}$ supply current (nonvolatile write) | | | 5 | mA | $f_{SCL}$ = 400KHz; $V_{CC}$ = +6V; SDA = Open; (for 2-Wire, Active, Nonvolatile Write State only) |
| $I_{SB}$ | $V_{CC}$ current (standby) | | | 5 | µA | $V_{CC}$ = +6V; $V_{IN}$ = $V_{SS}$ or $V_{CC}$; SDA = $V_{CC}$; (for 2-Wire, Standby State only) |
| $I_{LI}$ | Input leakage current | | | 10 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ |
| $I_{LO}$ | Output leakage current | | | 10 | µA | $V_{OUT}$ = $V_{SS}$ to $V_{CC}$ |
| $V_{IH}$ | Input HIGH voltage | $V_{CC}$ x 0.7 | | $V_{CC}$ + 1 | V | |
| $V_{IL}$ | Input LOW voltage | –1 | | $V_{CC}$ x 0.3 | V | |
| $V_{OL}$ | Output LOW voltage | | | 0.4 | V | $I_{OL}$ = 3mA |
| $V_{OH}$ | Output HIGH voltage | | | | | |

## ENDURANCE AND DATA RETENTION

| Parameter | Min. | Units |
|---|---|---|
| Minimum endurance | 100,000 | Data changes per bit per register |
| Data retention | 100 | years |

## CAPACITANCE

| Symbol | Test | Max. | Units | Test Conditions |
|---|---|---|---|---|
| $C_{IN/OUT}$(6) | Input / Output capacitance (SDA) | 8 | pF | $V_{OUT}$ = 0V |
| $C_{IN}$(6) | Input capacitance (SCL, $\overline{WP}$, A2, A1 and A0) | 6 | pF | $V_{IN}$ = 0V |

## POWER-UP TIMING

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_r$ $V_{CC}$(6) | $V_{CC}$ Power-up rate | 0.2 | 50 | V/ms |
| $t_{PUR}$(7) | Power-up to initiation of read operation | | 1 | ms |
| $t_{PUW}$(7) | Power-up to initiation of write operation | | 50 | ms |

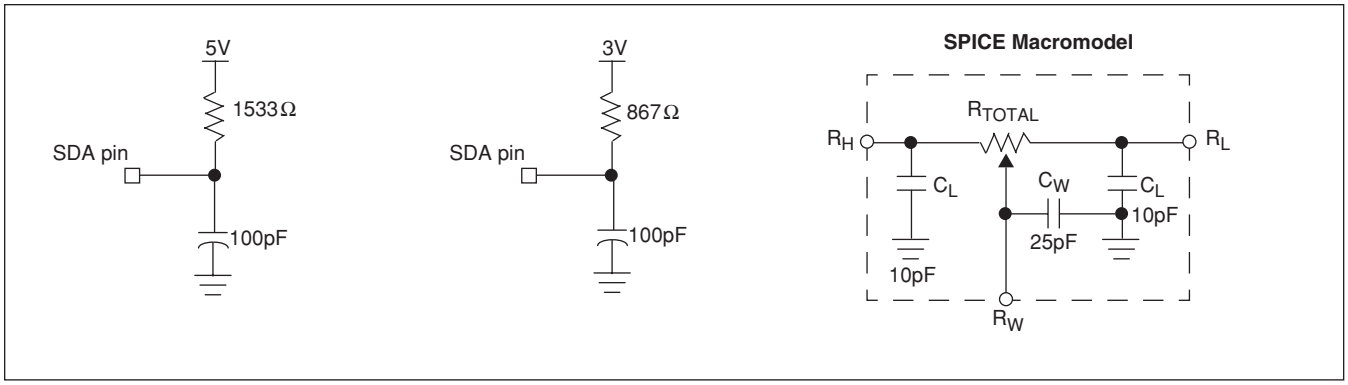
## A.C. TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | $V_{CC}$ x 0.1 to $V_{CC}$ x 0.9 |
| Input rise and fall times | 10ns |
| Input and output timing level | $V_{CC}$ x 0.5 |

**Notes:** (6) This parameter is not 100% tested

(7) $t_{PUR}$ and $t_{PUW}$ are the delays required from the time the (last) power supply ($V_{CC}$-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

## EQUIVALENT A.C. LOAD CIRCUIT




## AC TIMING

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency | | 400 | kHz |
| $t_{CYC}$ | Clock Cycle Time | 2500 | | ns |
| $t_{HIGH}$ | Clock High Time | 600 | | ns |
| $t_{LOW}$ | Clock Low Time | 1300 | | ns |
| $t_{SU:STA}$ | Start Setup Time | 600 | | ns |
| $t_{HD:STA}$ | Start Hold Time | 600 | | ns |
| $t_{SU:STO}$ | Stop Setup Time | 600 | | ns |
| $t_{SU:DAT}$ | SDA Data Input Setup Time | 100 | | ns |
| $t_{HD:DAT}$ | SDA Data Input Hold Time | 30 | | ns |
| $t_R$ | SCL and SDA Rise Time | | 300 | ns |
| $t_F$ | SCL and SDA Fall Time | | 300 | ns |
| $t_{AA}$ | SCL Low to SDA Data Output Valid Time | | 0.9 | µs |
| $t_{DH}$ | SDA Data Output Hold Time | 0 | | ns |
| $T_I$ | Noise Suppression Time Constant at SCL and SDA inputs | 50 | | ns |
| $t_{BUF}$ | Bus Free Time (Prior to Any Transmission) | 1200 | | ns |
| $t_{SU:WPA}$ | A0, A1 Setup Time | 0 | | ns |
| $t_{HD:WPA}$ | A0, A1 Hold Time | 0 | | ns |

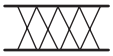
## HIGH-VOLTAGE WRITE CYCLE TIMING

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $t_{WR}$ | High-voltage write cycle time (store instructions) | 5 | 10 | ms |

## XDCP TIMING

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{WRPO}$ | Wiper response time after the third (last) power supply is stable | 5 | 10 | µs |
| $t_{WRL}$ | Wiper response time after instruction issued (all load instructions) | 5 | 10 | µs |

## SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
|  | Must be steady | Will be steady |
|  | May change from Low to High | Will change from Low to High |
|  | May change from High to Low | Will change from High to Low |
|  | Don't Care: Changes Allowed | Changing: State Not Known |
|  | N/A | Center Line is High Impedance |

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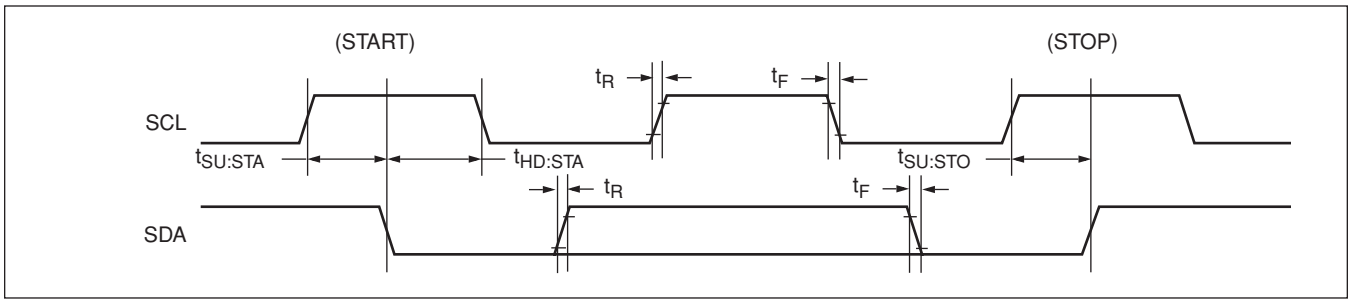
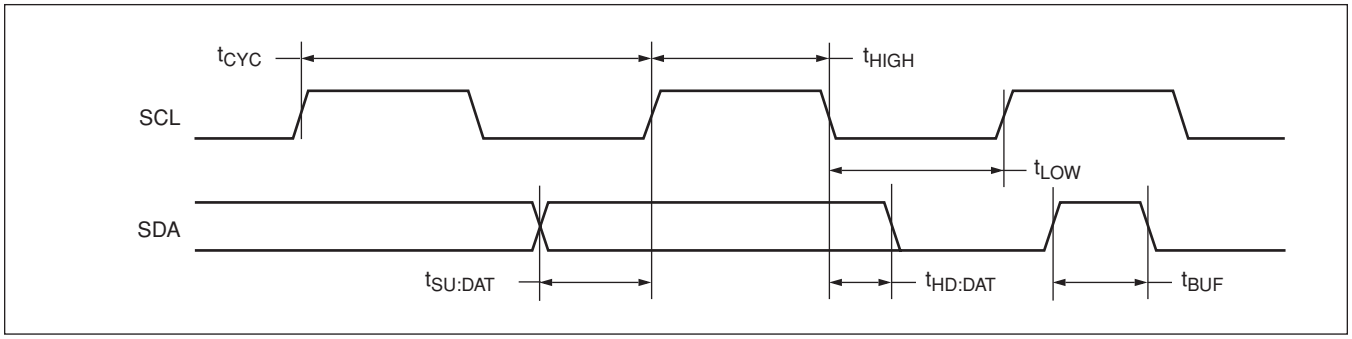
## TIMING DIAGRAMS

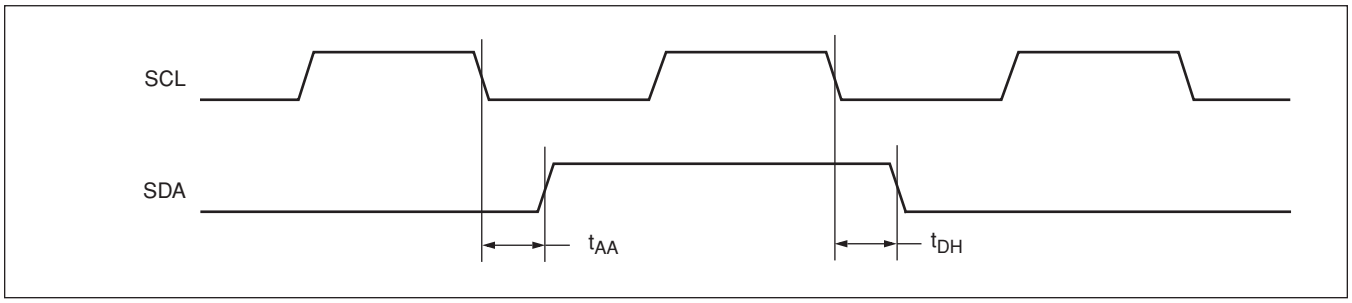
### Start and Stop Timing



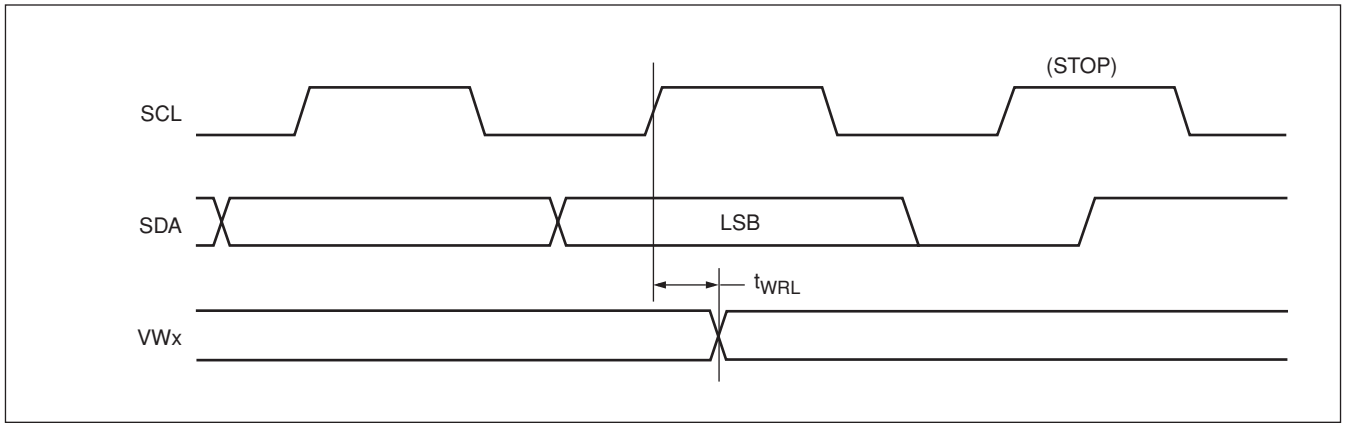

### Input Timing



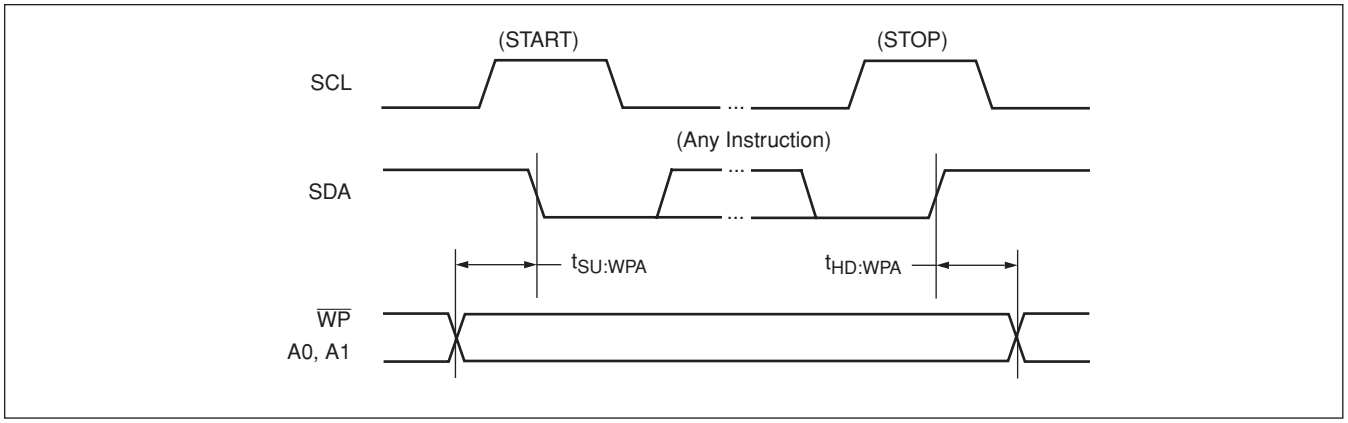

### Output Timing



### XDCP Timing (for All Load Instructions)

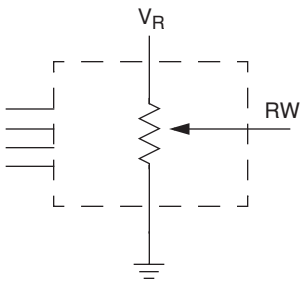



### Write Protect and Device Address Pins Timing

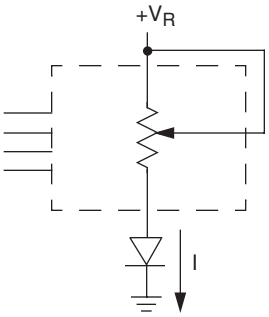


## APPLICATIONS INFORMATION

### Basic Configurations of Electronic Potentiometers



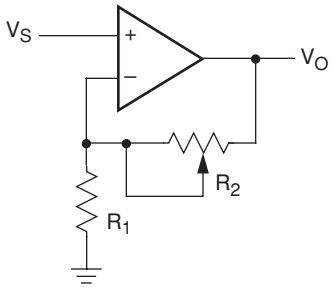

Three terminal Potentiometer;
Variable voltage divider




Two terminal Variable Resistor;
Variable current

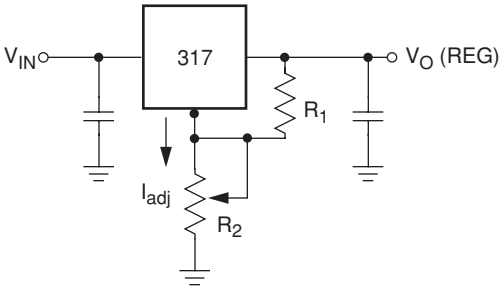
### Application Circuits

#### Noninverting Amplifier



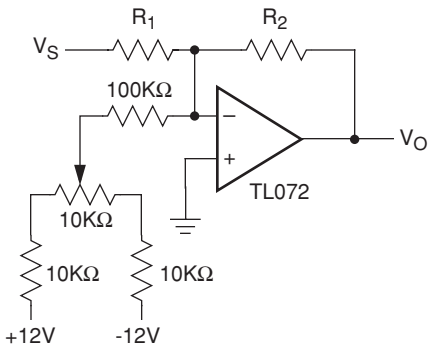

$V_O = (1+R_2/R_1)V_S$

#### Voltage Regulator

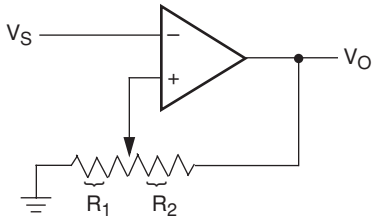



$V_O$ (REG) = 1.25V $(1+R_2/R_1)+I_{adj}$ $R_2$

#### Offset Voltage Adjustment



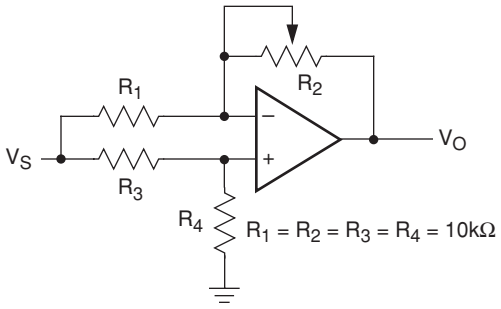

#### Comparator with Hysterisis




$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$RL_L = \{R_1/(R_1+R_2)\}\ V_O(min)$

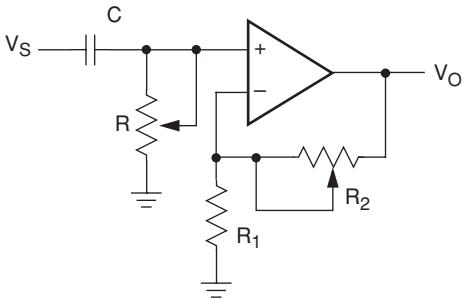
## Application Circuits (continued)

### Attenuator



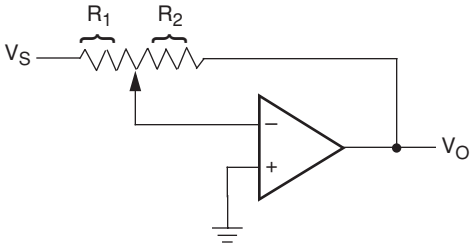

$V_O = G V_S$
$-1/2 \le G \le +1/2$

### Filter



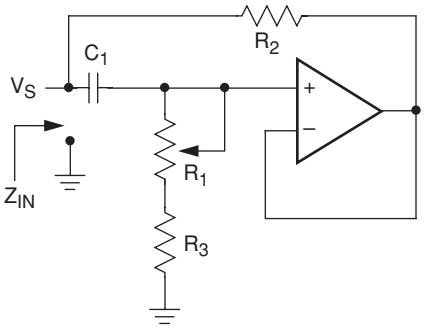

$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

### Inverting Amplifier



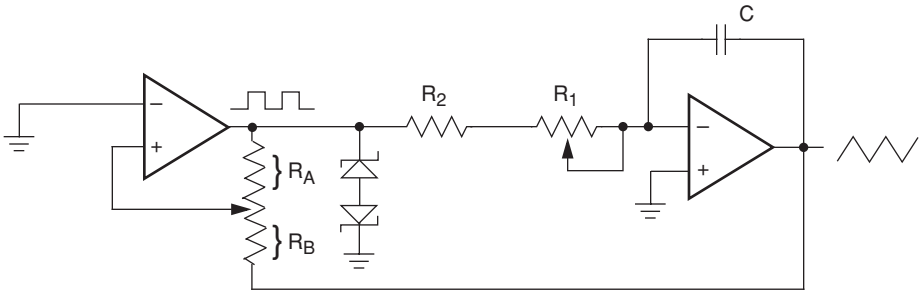

$V_O = G V_S$
$G = - R_2/R_1$

### Equivalent L-R Circuit




$Z_{IN} = R_2 + s\, R_2 (R_1 + R_3)\, C_1 = R_2 + s\, Leq$
$(R_1 + R_3) >> R_2$

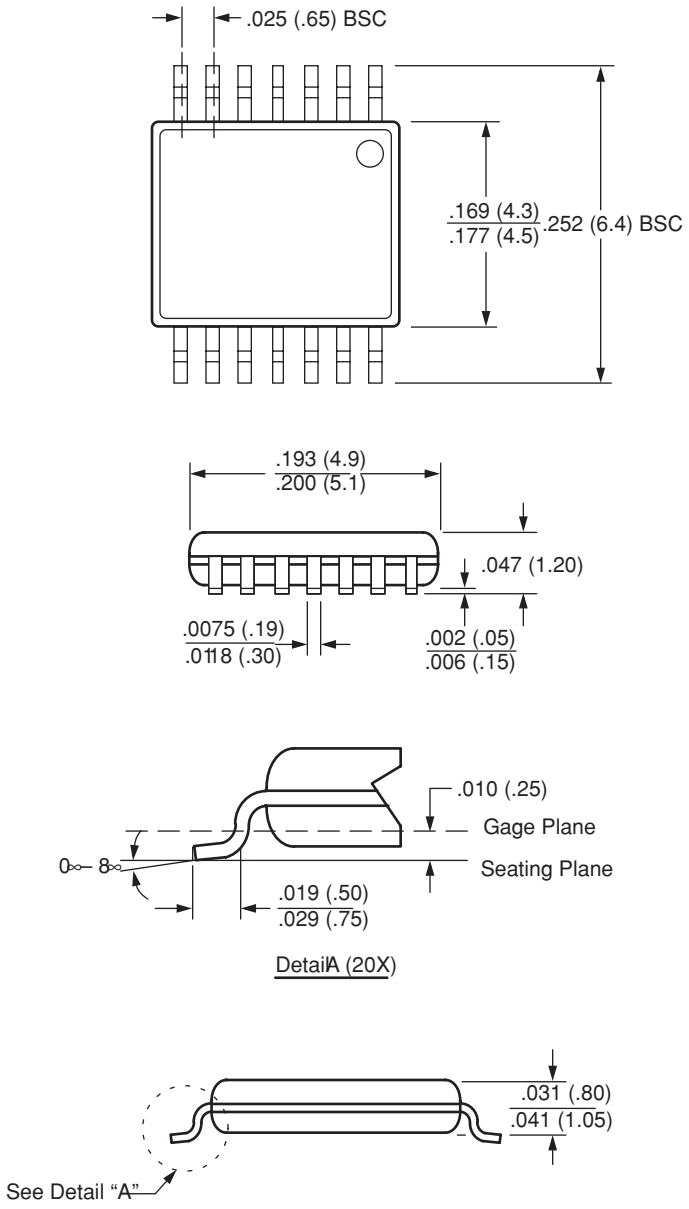
### Function Generator




frequency ∝ $R_1$, $R_2$, C
amplitude ∝ $R_A$, $R_B$

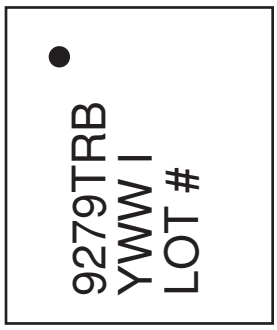
## PACKAGING INFORMATION

### 14-LEAD PLASTIC, TSSOP, PACKAGE TYPE V

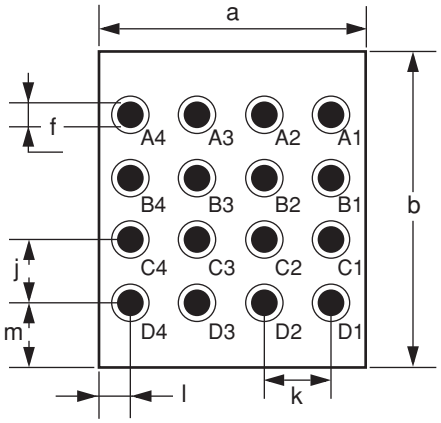



**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

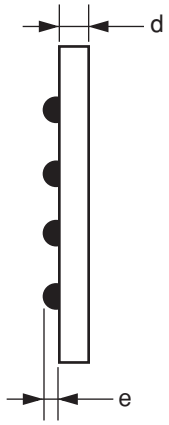
# 16-Bump Chip Scale Package (CSP B16)
# Package Outline Drawing




Top View (Marking Side)

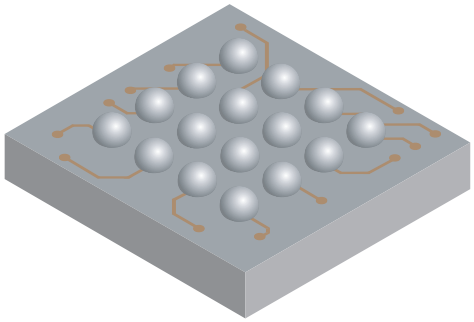



Bottom View (Bumped Side)




Side View


Side View



## Package Dimensions

| | Symbol | Millimeters | | |
|---|---|---|---|---|
| | | Min | Nominal | Max |
| Package Width | a | 2.593 | 2.623 | 2.653 |
| Package Length | b | 2.771 | 2.801 | 2.831 |
| Package Height | c | 0.644 | 0.677 | 0.710 |
| Body Thickness | d | 0.444 | 0.457 | 0.470 |
| Ball Height | e | 0.200 | 0.220 | 0.240 |
| Ball Diameter | f | 0.300 | 0.320 | 0.340 |
| Ball Pitch – Width | j | | 0.5 | |
| Ball Pitch – Length | k | | 0.5 | |
| Ball to Edge Spacing – Width | l | 0.537 | 0.562 | 0.587 |
| Ball to Edge Spacing – Length | m | 0.626 | 0.651 | 0.676 |

## Ball Matrix:

| | 4 | 3 | 2 | 1 |
|---|---|---|---|---|
| **A** | A0 | Vcc | $R_L$ | $R_H$ |
| **B** | A2 | NC | NC | $R_W$ |
| **C** | SCL | NC | NC | A3 |
| **D** | SDA | Vss | $\overline{WP}$ | A1 |

## ORDERING INFORMATION