DATA SHEET

I²C BUS

PCA9545

4-channel I²C switch with interrupt logic and reset

Product data

Supersedes data of 2001 Nov 08

2002 Mar 28

Philips Semiconductors

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4-channel I^{2}C switch with interrupt logic and reset   **PCA9545**

passed by the PCA9545. This allows the use of different bus voltages on each pair, so that 1.8 V or 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.
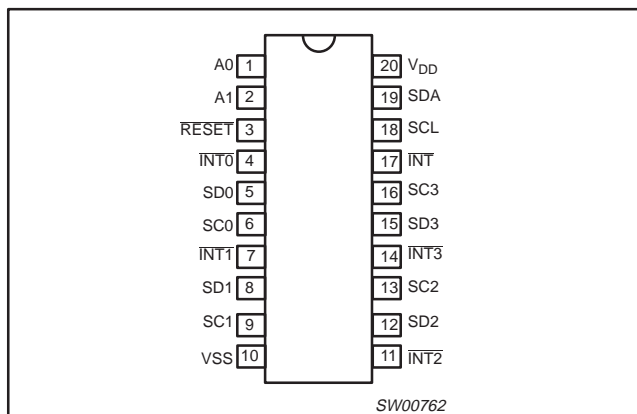
PIN CONFIGURATION


```
        A0   1          20   V_DD
        A1   2          19   SDA
     RESET   3          18   SCL
      INT0   4          17   INT
       SD0   5          16   SC3
       SC0   6          15   SD3
      INT1   7          14   INT3
       SD1   8          13   SC2
       SC1   9          12   SD2
       VSS  10          11   INT2
                              SW00762
```

Figure 1. Pin configuration

FEATURES

- 1-of-4 bi-directional translating switches
- I^{2}C interface logic; compatible with SMBus standards
- 4 active low interrupt inputs
- Active low interrupt output
- Active low reset input
- 2 address pins allowing up to 4 devices on the I^{2}C bus
- Channel selection via I^{2}C bus, in any combination
- Power up with all switch channels deselected
- Low RDS$_{ON}$ switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant Inputs
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Package Offer: SO20, TSSOP20

DESCRIPTION

The PCA9545 is a quad bi-directional translating switch controlled via the I^{2}C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs, INT0 to INT3, one for each of the downstream pairs, are provided. One interrupt output, INT, acts as an AND of the four interrupt inputs.

An active-LOW reset input allows the PCA9545 to recover from a situation where one of the downstream I^{2}C buses is stuck in a LOW state. Pulling the RESET pin LOW resets the I^{2}C state machine and causes all the channels to be deselected as does the internal power on reset function.

The pass gates of the switches are constructed such that the V$_{DD}$ pin can be used to limit the maximum high voltage which will be

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	A0	Address input 0
2	A1	Address input 1
3	RESET	Active low reset input
4	INT0	Active low interrupt input 0
5	SD0	Serial data 0
6	SC0	Serial clock 0
7	INT1	Active low interrupt input 1
8	SD1	Serial data 1
9	SC1	Serial clock 1
10	V$_{SS}$	Supply ground
11	INT2	Active low interrupt input 2
12	SD2	Serial data 2
13	SC2	Serial clock 2
14	INT3	Active low interrupt input 3
15	SD3	Serial data 3
16	SC3	Serial clock 3
17	INT	Active low interrupt output
18	SCL	Serial clock line
19	SDA	Serial data line
20	V$_{DD}$	Supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic SO	–40 to +85 °C	PCA9545D	SOT163-1
20-Pin Plastic TSSOP	–40 to +85 °C	PCA9545PW	SOT360-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

4-channel I^{2}C switch with interrupt logic and reset   PCA9545

BLOCK DIAGRAM

Figure 2. Block diagram

4-channel I^{2}C switch with interrupt logic and reset

PCA9545

DEVICE ADDRESS

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9545 is shown in Figure 3. To conserve power, no internal pullup resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.
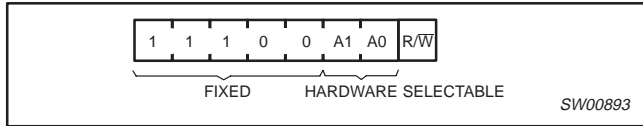

| 1 | 1 | 1 | 0 | 0 | A1 | A0 | R/$\overline{W}$ |

FIXED   HARDWARE SELECTABLE

SW00893

Figure 3. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9545, which will be stored in the control register. If multiple bytes are received by the PCA9545, it will save the last byte received. This register can be written and read via the I^{2}C bus.
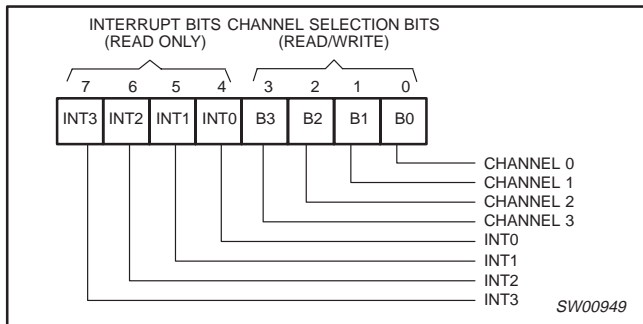

Figure 4. Control Register

CONTROL REGISTER DEFINITION

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9545 has been addressed. The 2 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a stop condition has been placed on the I^{2}C bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 1. Control Register; Write — Channel Selection/ Read — Channel Status

INT3	INT2	INT1	INT0	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1	X	Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled

NOTE: Several channels can be enabled at the same time.
Ex: B3 = 0, B2 = 1, B1 = 1, B0 = 0, means that channel 0 and 3 are disabled and channel 1 and 2 are enabled.
Care should be taken not to exceed the maximum bus capacity.

4-channel I^{2}C switch with interrupt logic and reset

PCA9545

INTERRUPT HANDLING

The PCA9545 provides 4 interrupt inputs, one for each channel, and one open drain interrupt output. When an interrupt is generated by any device, it will be detected by the PCA9545 and the interrupt output will be driven LOW. The channel does not need to be active for detection of the interrupt. A bit is also set in the control register.

Bits 4 – 7 of the control register correspond to channels 0 – 3 of the PCA9545, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PCA9545 and read the contents of the control register to determine which channel contains the device generating the interrupt. The master can then reconfigure the PCA9545 to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can be providing an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{DD} through a pull-up resistor.

Table 2. Control Register Read — Interrupt

INT3	INT2	INT1	INT0	B3	B2	B1	B0	COMMAND
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
X	0	X	X	X	X	X	X	No interrupt on channel 2
	1							Interrupt on channel 2
0	X	X	X	X	X	X	X	No interrupt on channel 3
1								Interrupt on channel 3

NOTE: Several interrupts can be active at the same time.
Ex: INT3 = 0, INT2 = 1, INT1 = 1, INT0 = 0, means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

RESET INPUT

The $\overline{RESET}$ input is an active-LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of t_{WL}, the PCA9545 will reset its registers and I^{2}C state machine and will deselect all channels. The $\overline{RESET}$ input must be connected to V_{DD} through a pull-up resistor.

POWER-ON RESET

When power is applied to V_{DD}, an internal Power On Reset holds the PCA9545 in a reset state until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9545 registers and I^{2}C state machine are initialized to their default states, all zeroes causing all the channels to be deselected.

VOLTAGE TRANSLATION

The pass gate transistors of the PCA9545 are constructed such that the V_{DD} voltage can be used to limit the maximum voltage that will be passed from one I^{2}C bus to another.
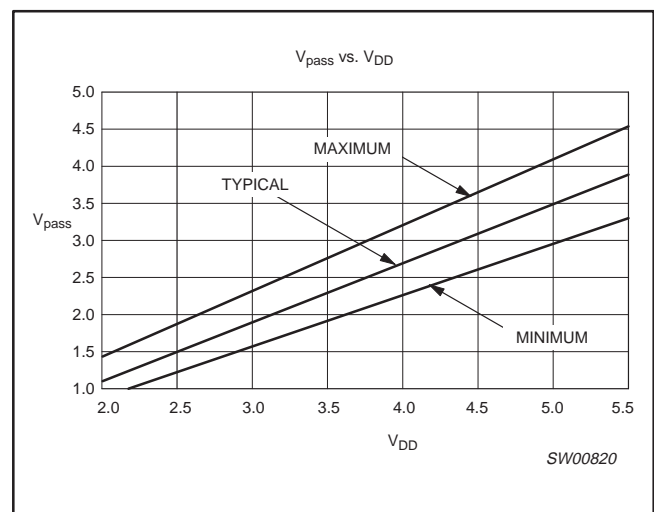
Figure 5. V_{pass} voltage vs. V_{DD}

Figure 5 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in the DC Characteristics section of this datasheet). In order for the PCA9545 to act as a voltage translator, the V_{pass} voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then V_{pass} should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 5, we see that V_{pass} (max.) will be at 2.7 V when the PCA9545 supply voltage is 3.5 V or lower so the PCA9545 supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 12).

More Information can be found in Application Note AN262 *PCA954X family of I^{2}C/SMBus multiplexers and switches.*

CHARACTERISTICS OF THE I^{2}C-BUS

The I^{2}C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).
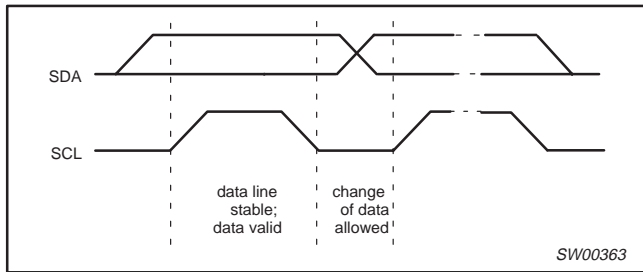

Figure 6. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 7).

System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 8).
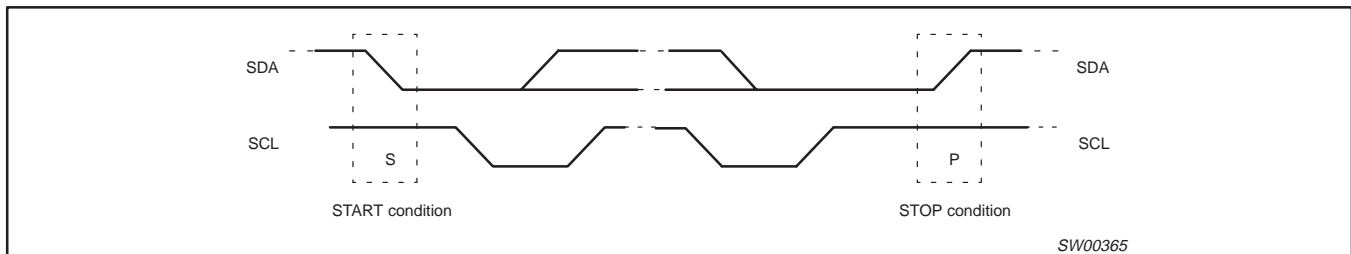

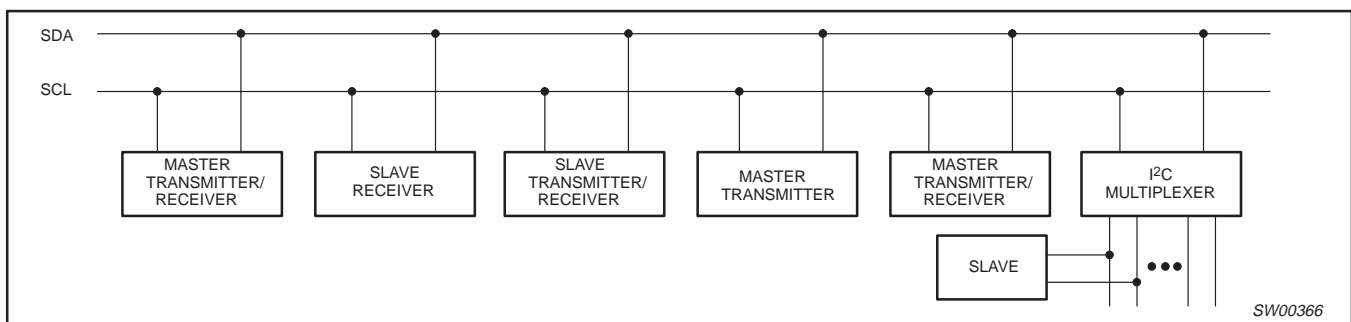**Figure 7. Definition of start and stop conditions**

Figure 8. System configuration

4-channel I²C switch with interrupt logic and reset

PCA9545

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.
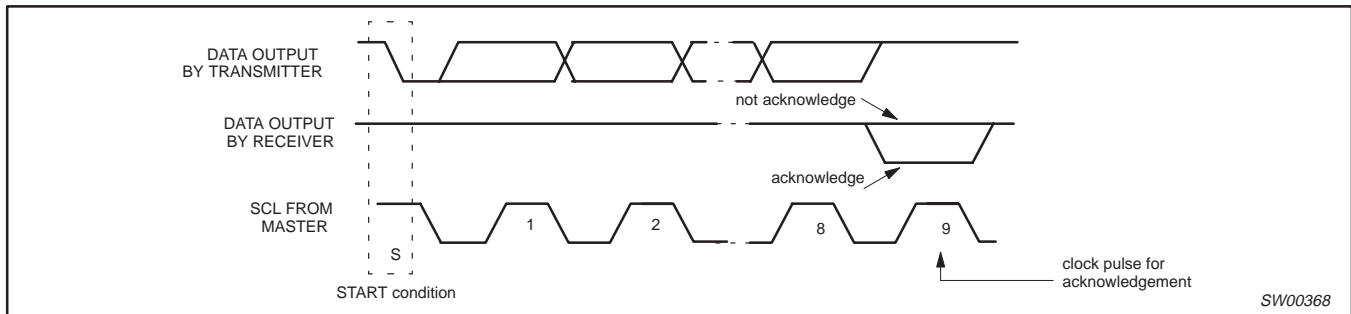

Figure 9. Acknowledgement on the I²C-bus

Bus transactions

Data is transmitted to the PCA9545 control register using the write mode as shown in Figure 10.
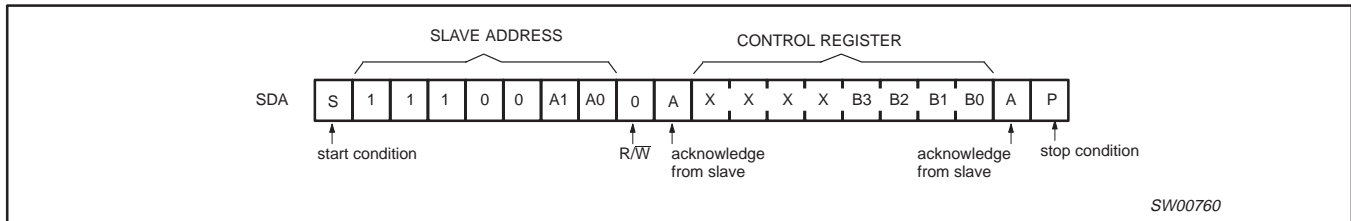

Figure 10. WRITE control register

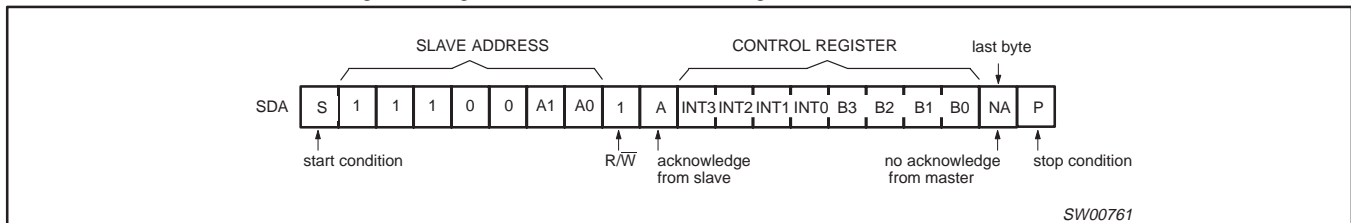Data is read from PCA9545 control register using the read mode as shown in Figure 11.

Figure 11. READ control register

4-channel I²C switch with interrupt logic and reset   PCA9545

TYPICAL APPLICATION
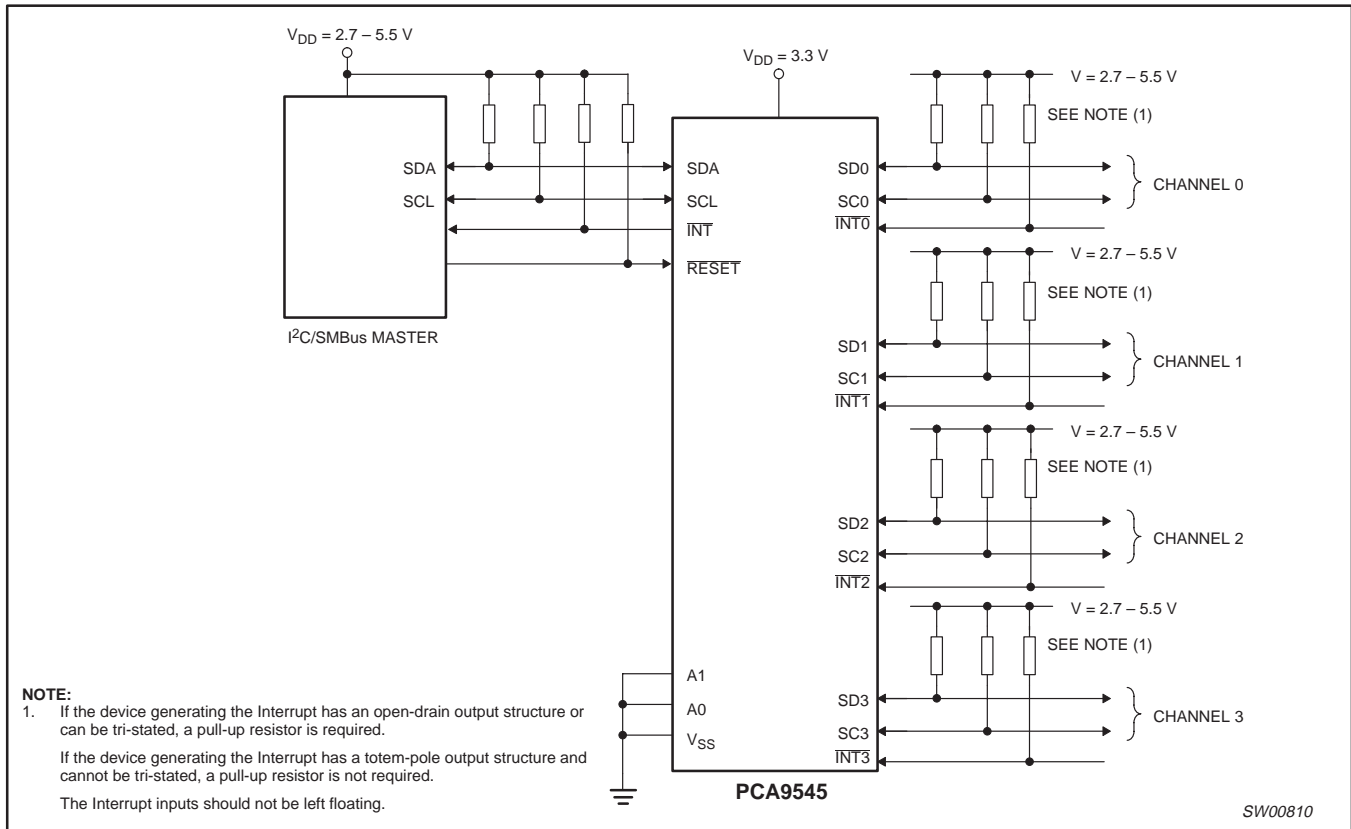
Figure 12. Typical application

NOTE:
1.   If the device generating the Interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required.

If the device generating the Interrupt has a totem-pole output structure and cannot be tri-stated, a pull-up resistor is not required.

The Interrupt inputs should not be left floating.

4-channel I^{2}C switch with interrupt logic and reset   PCA9545

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING		UNIT
			MIN	MAX	
V_{DD}	DC supply voltage		−0.5	+7.0	V
V_I	DC input voltage		−0.5	+7.0	V
I_I	DC input current		—	±20	mA
I_O	DC output current		—	±25	mA
I_{DD}	DC Supply current		—	±100	mA
I_{SS}	DC Supply current		—	±100	mA
P_{tot}	total power dissipation		—	400	mW
T_{stg}	Storage temperature range		−60	+150	°C
T_{amb}	Operating ambient temperature		−40	+85	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

DC CHARACTERISTICS

V_{DD} = 2.3 to 3.6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified. (See page 11 for V_{DD} = 3.6 to 5.5 V.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply						
V_{DD}	Supply voltage		2.3	—	3.6	V
I_{DD}	Supply current	Operating mode; V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	—	30	100	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}	—	20	100	µA
V_{POR}	Power-on reset voltage	no load; V_I = V_{DD} or V_{SS}	—	1.6	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		−0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	—	6	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	mA
		V_{OL} = 0.6 V	6	—	—	
I_L	Leakage current	V_I = V_{DD} or V_{SS}	−1	—	+1	µA
C_i	Input capacitance	V_I = V_{SS}	—	12	13	pF
Select inputs A0 to A1 / INT0 to INT3 / RESET						
V_{IL}	LOW level input voltage		−0.5	—	+0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	—	V_{DD} + 0.5	V
I_{LI}	Input leakage current	pin at V_{DD} or V_{SS}	−1	—	+1	µA
C_i	Input capacitance	V_I = V_{SS}	—	1.6	3	pF
Pass Gate						
R_{ON}	Switch resistance	V_{DD} = 3.0 to 3.6 V, V_O = 0.4 V, I_O = 15 mA	5	20	30	Ω
		V_{DD} = 2.3 to 2.7 V, V_O = 0.4 V, I_O = 10 mA	7	26	55	
V_{Pass}	Switch output voltage	V_{swin} = V_{DD} = 3.3 V; I_{swout} = −100 µA	—	2.2	—	V
		V_{swin} = V_{DD} = 3.0 to 3.6 V; I_{swout} = −100 µA	1.6	—	2.8	
		V_{swin} = V_{DD} = 2.5 V; I_{swout} = −100 µA	—	1.5	—	
		V_{swin} = V_{DD} = 2.3 to 2.7 V; I_{swout} = −100 µA	1.1	—	2.0	
I_L	Leakage current	V_I = V_{DD} or V_{SS}	−1	—	+1	µA
C_{io}	Input/output capacitance	V_I = V_{SS}	—	3	5	pF
INT Output						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	mA
I_{OH}	HIGH level output current		—	—	+100	µA

4-channel I^{2}C switch with interrupt logic and reset

PCA9545

DC CHARACTERISTICS

V_{DD} = 3.6 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified. (See page 10 for V_{DD} = 2.3 to 3.6 V.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply						
V_{DD}	Supply voltage		3.6	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	—	575	600	μA
I_{stb}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}	—	130	200	μA
V_{POR}	Power-on reset voltage	no load; V_I = V_{DD} or V_{SS}	—	1.6	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		–0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	—	6	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	mA
		V_{OL} = 0.6 V	6	—	—	mA
I_{IL}	LOW level input current	V_I = V_{SS}	–10	—	+10	μA
I_{IH}	HIGH level input current	V_I = V_{DD}	—	—	+100	μA
C_i	Input capacitance	V_I = V_{SS}	—	12	13	pF
Select inputs A0 to A1 / INT0 to INT3 / RESET						
V_{IL}	LOW level input voltage		–0.5	—	+0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	—	V_{DD} + 0.5	V
I_{LI}	Input leakage current	pin at V_{DD} or V_{SS}	–1	—	+50	μA
C_i	Input capacitance	V_I = V_{SS}	—	1.6	3	pF
Pass Gate						
R_{ON}	Switch resistance	V_{CC} = 4.5 to 5.5 V, V_O = 0.4 V, I_O = 15 mA	4	11	24	Ω
V_{Pass}	Switch output voltage	V_{swin} = V_{DD} = 5.0 V; I_{swout} = –100 μA	—	3.5	—	V
		V_{swin} = V_{DD} = 4.5 to 5.5 V; I_{swout} = –100 μA	2.6	—	4.5	V
I_L	Leakage current	V_I = V_{DD} or V_{SS}	–1	—	+100	μA
C_{io}	Input/output capacitance	V_I = V_{SS}	—	3	5	pF
INT Output						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	mA
I_{OH}	HIGH level output current		—	—	+100	μA

4-channel I^{2}C switch with interrupt logic and reset

PCA9545

AC CHARACTERISTICS

SYMBOL	PARAMETER	STANDARD-MODE I^{2}C-BUS		FAST-MODE I^{2}C-BUS		UNIT
		MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay from SDA to SD$_n$ or SCL to SC$_n$	—	0.3[1]	—	0.3[1]	ns
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs
$t_{HD;STA}$	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	—	0.6	—	μs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	μs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	—	0.6	—	μs
$t_{HD;DAT}$	Data hold time	0[2]	3.45	0[2]	0.9	μs
$t_{SU;DAT}$	Data set-up time	250	—	100	—	ns
t_R	Rise time of both SDA and SCL signals	—	1000	20 + 0.1C$_b$[3]	300	ns
t_F	Fall time of both SDA and SCL signals	—	300	20 + 0.1C$_b$[3]	300	μs
C_b	Capacitive load for each bus line	—	400	—	400	μs
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	—	50	—	50	ns
$t_{VD:DATL}$	Data valid (HL)	—	1	—	1	μs
$t_{VD:DATH}$	Data valid (LH)	—	0.6	—	0.6	μs
$t_{VD:ACK}$	Data valid Acknowledge	—	1	—	1	μs
$\overline{INT}$						
t_{iv}	$\overline{INTn}$ to $\overline{INT}$ active valid time	—	4	—	4	μs
t_{ir}	$\overline{INTn}$ to $\overline{INT}$ inactive delay time	—	2	—	2	μs
L_{pwr}	LOW level pulse width rejection or $\overline{INTn}$ inputs	1	—	1	—	μs
H_{pwr}	HIGH level pulse width rejection or $\overline{INTn}$ inputs	0.5	—	0.5	—	μs
RESET						
$t_{WL(rst)}$	Pulse width low reset	4	—	4	—	ns
t_{rst}	Reset time (SDA clear)	500	—	500	—	ns
$t_{REC:STA}$	Recovery to Start	0	—	0	—	ns

NOTES:
1. Pass gate propagation delay is calculated from the 20 Ω typical R$_{ON}$ and the 15 pF load capacitance.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH$_{min}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
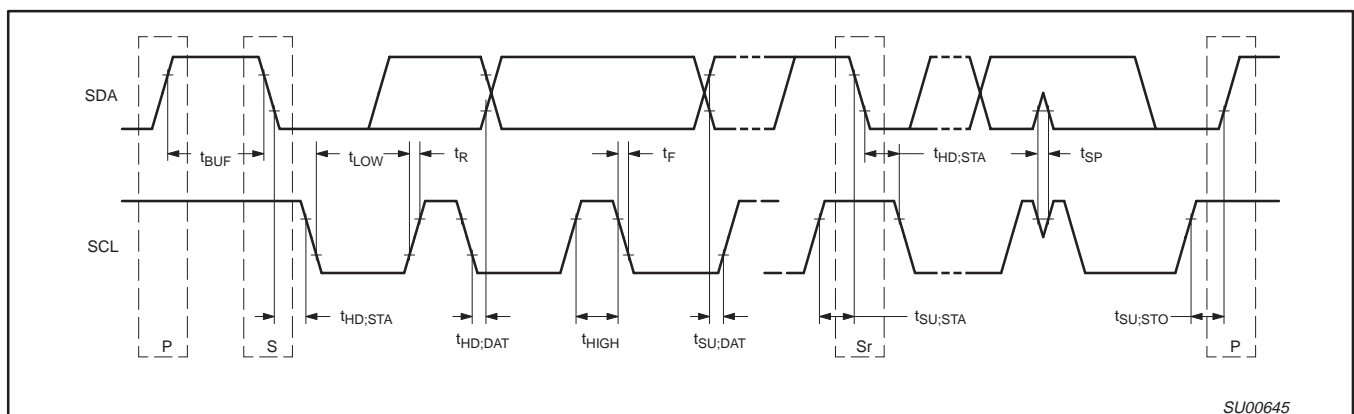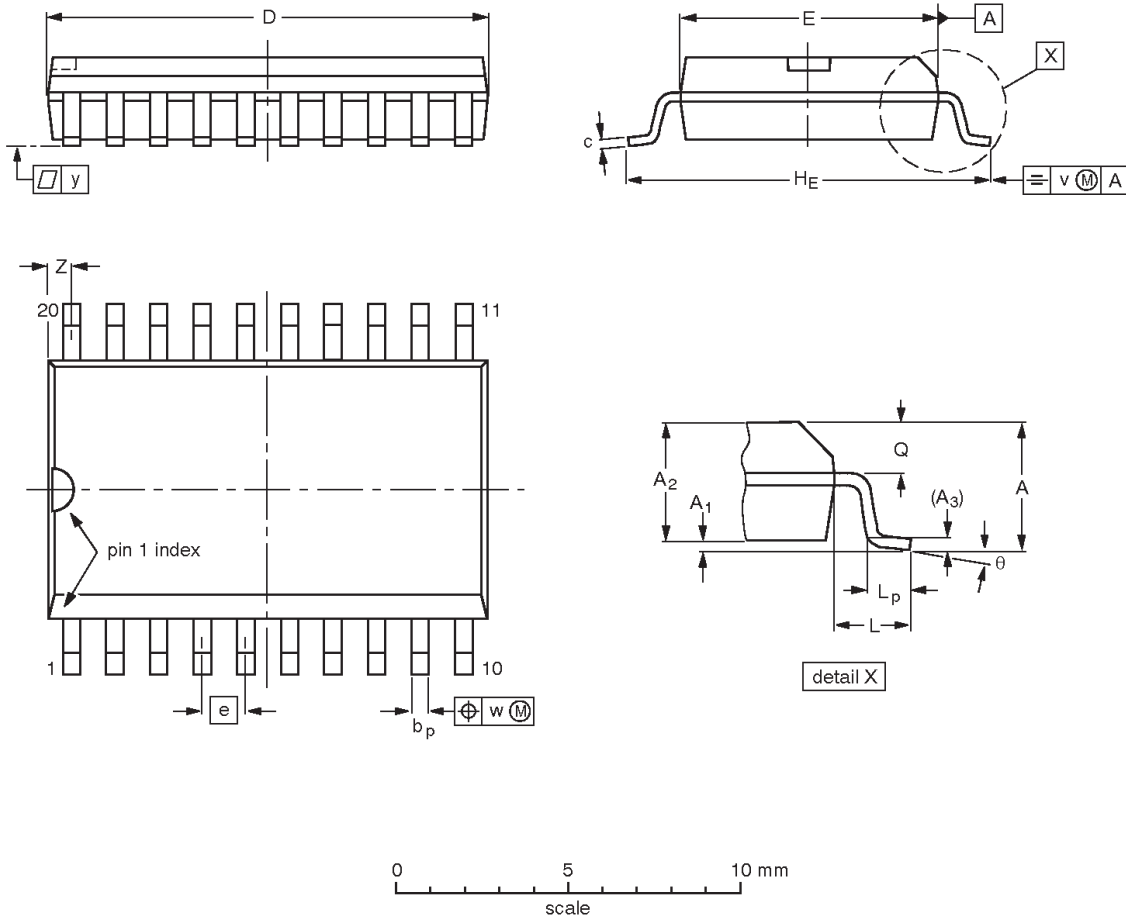3. C$_b$ = total capacitance of one bus line in pF.

Figure 13. Definition of timing on the I^{2}C-bus

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

detail X

scale 0 5 10 mm

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[1]	e	HₑE	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

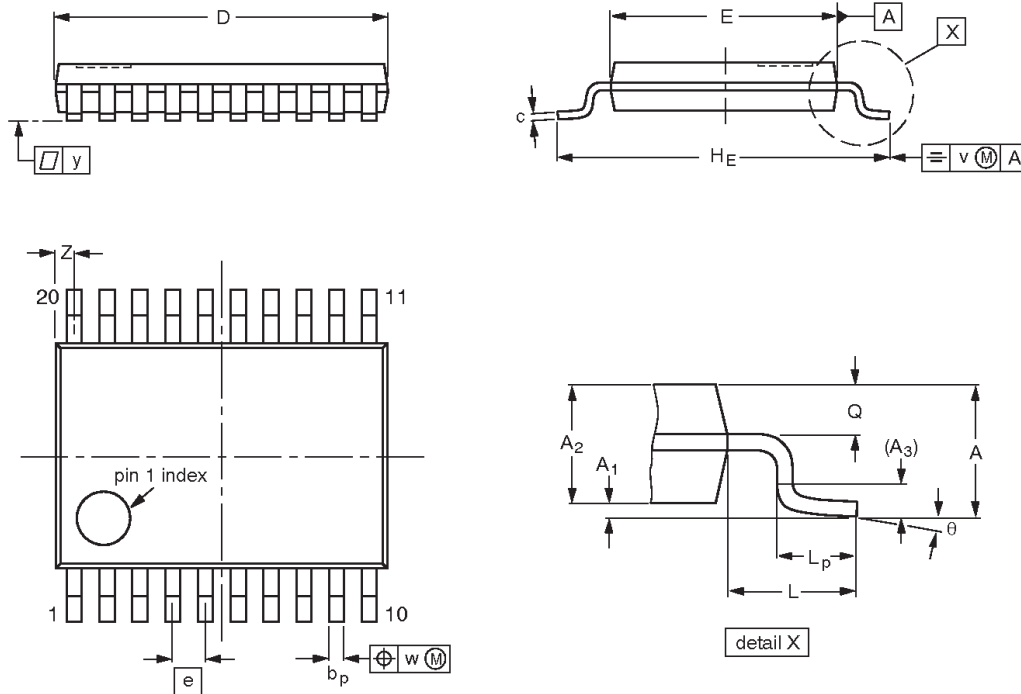1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				97-05-22 99-12-27

4-channel I²C switch with interrupt logic and reset

PCA9545

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1


```
0        2.5        5 mm
|__|__|__|__|__|__|__|__|
         scale
```

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D (1)	E (2)	e	Hₑ	L	Lₚ	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~95-02-04~~ 99-12-27

4-channel I^{2}C switch with interrupt logic and reset

PCA9545

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Data sheet status[1]	Product status[2]	Definitions
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Date of release: 03-02

Document order number: 9397 750 09608

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