3-1/2 DIGIT A/D CONVERTER WITH HOLD AND DIFFERENTIAL REFERENCE INPUTS

FEATURES

- Differential Reference Input
- Display Hold Function
- Fast Over-Range Recovery, Guaranteed Next Reading Accuracy
- Low Temperature Drift Internal Reference ..... 35ppm/°C (Typ)
- Guaranteed Zero Reading With Zero Input
- Low Noise ..... 15μV_{p-p}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- High Impedance Differential Input
- Low Input Leakage Current ..... 1pA Typ
  10pA Max
- Direct LCD Drive – No External Components
- Precision Null Detection with True Polarity at Zero
- Crystal Clock Oscillator
- Available in DIP, Compact Flat Package or PLCC
- Convenient 9V Battery Operation with Low Power Dissipation (600µA Typical, 1mW Maximum)

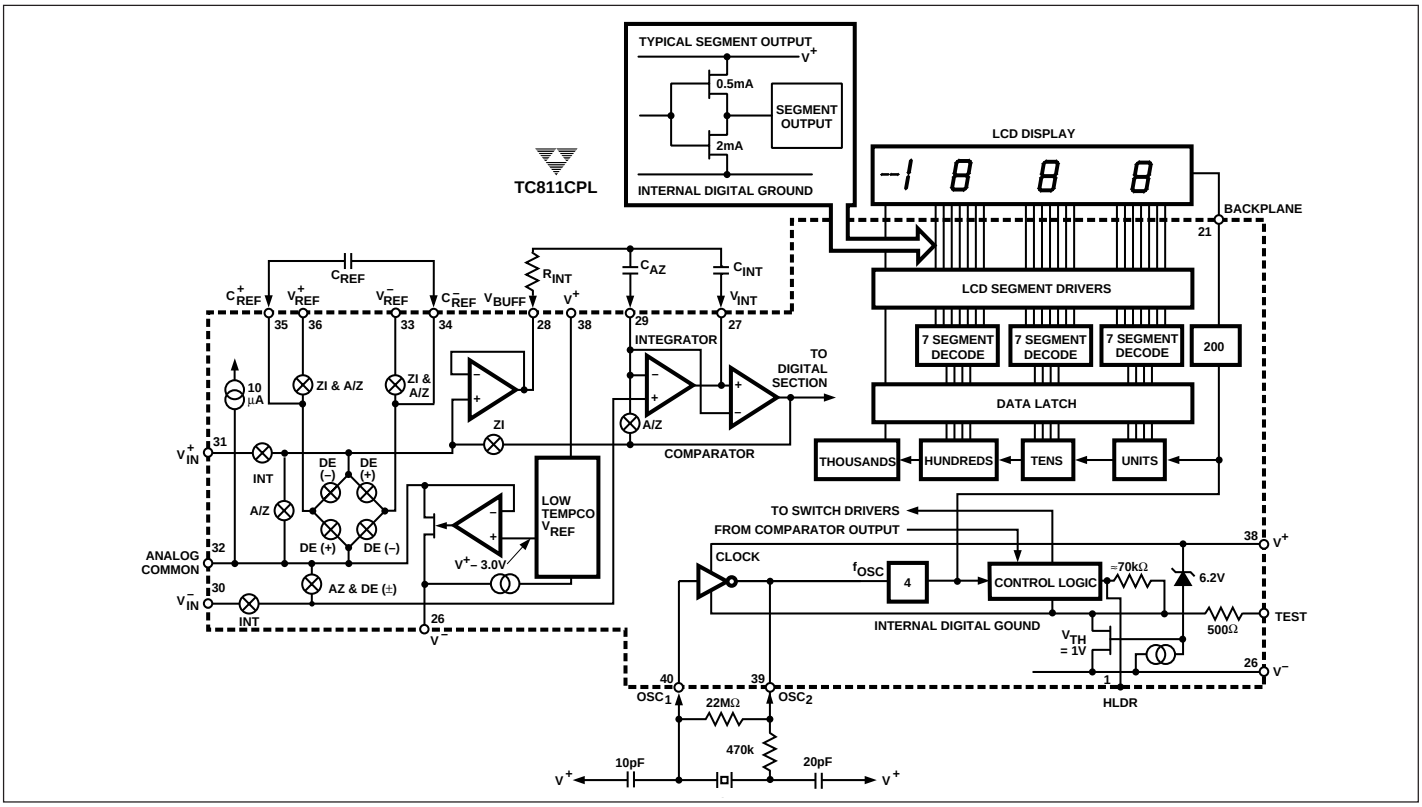
TYPICAL APPLICATIONS

- Thermometry
- Digital Meters
  - — Voltage/Current/Power
  - — pH Measurement
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity
  - — Humidity
  - — Position
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Digital Scales
- Process Monitors
- Gaussometers
- Photometers

ORDERING INFORMATION

Part No.	Package	Temp. Range	Max V_{REF} Tempco
TC811CKW	44-PQFP	0°C to +70°C	75 ppm/°C
TC811CPL	40-Pin Plastic DIP	0°C to +70°C	75 ppm/°C

FUNCTIONAL BLOCK DIAGRAM



TC811

GENERAL DESCRIPTION

The TC811 is a low power, 3-1/2 digit, LCD display analog-to-digital converter. This device incorporates both a display hold feature and differential reference inputs. A crystal oscillator, which only requires two pins, permits added features while retaining a 40-pin package. An additional feature is an "Integrator Output Zero" phase which guarantees rapid input overrange recovery.

The TC811 display hold (HLDR) function can be used to "freeze" the LCD display. The displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The TC811 also includes a differential reference for easy ratiometric measurements. Circuits which use the 7106/26/36 can easily be upgraded to include the hold function with the TC811.

The TC811 has an improved internal zener reference voltage circuit which maintains the Analog Common temperature drift to 35ppm/°C (typical) and 75ppm/°C (maximum). This represents an improvement of two to four times over similar 3-1/2 digit converters, eliminating the need for a costly, space consuming external reference source.

The TC811 limits linearity error to less than one count on both the 200mV and the 2.00V full-scale ranges. Rollover error—the difference in readings for equal magnitude but opposite polarity input signals—is below ±1 count. High impedance differential inputs offer 1pA leakage currents and a $10^{12}\Omega$ input impedance. The $15\mu V_{p-p}$ noise performance guarantees a “rock solid” reading. The Auto Zero cycle guarantees a zero display readout for a zero volt input.

The single chip CMOS TC811 incorporates all the active devices for a 3-1/2 digit analog to digital converter to directly drive an LCD display. Onboard oscillator, precision voltage reference and display segment and backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution (0.05%) indicating meter requires only a TC811, an LCD display, five resistors, six capacitors, a crystal, and a 9V battery. Compact, hand held multimeter designs benefit from the TelCom Semiconductor small footprint package option.

The TC811 uses a dual slope conversion technique which will reject interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400Hz line frequency signals are present.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V^+ to V^-) 15V
Analog Input voltage (Either Input)[1] ..... V^+ to V^-
Reference Input Voltage ..... V^+ to V^-
Clock Input ..... TEST to V^+
Power Dissipation[2] ($T_A \leq 70°C$)
- 44-Pin Flat Package 1.00W
- 40-Pin Plastic DIP 1.23W

Operating Temperature Range
- Commercial Package (C) ..... 0°C to +70°C
- Industrial Package (I) ..... – 25°C to +85°C

Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{Supply} = 9V, f_{CLOCK} = 32.768kHz, and T_A = 25°C, unless otherwise noted.

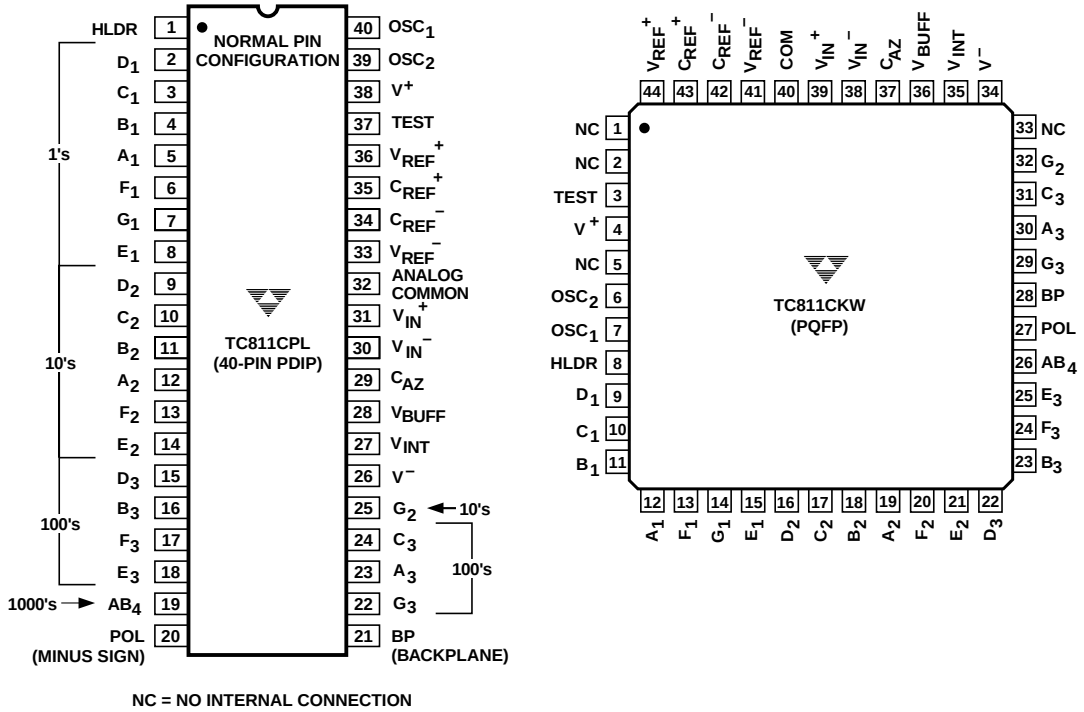
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
—	Zero Input Reading	V_{IN} = 0V V_{FS} = 200mV	– 000.0	±000.0	+000.0	Digital Reading
—	Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ 70°C	—	0.2	1	µV/°C
—	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
NL	Linearity Error	V_{FS} = 200mV or 2.000V	– 1	±0.2	+1	Counts
E_R	Roll Over Error	V_{IN}– = V_{IN}+ ≈ 200mV	– 1	±0.2	+1	Counts
e_N	Noise	V_{IN} = 0V, V_{FS} = 200mV	—	15	—	μV_{P-P}
I_L	Input Leakage Current	V_{IN} = 0V	—	1	10	pA
CMRR	Common-Mode Rejection	V_{CM} = ±1V, V_{IN} = 0V, V_{FS} = 200mV	—	50	—	µV/V

ELECTRICAL CHARACTERISTICS: V_{Supply} = 9V, f_{CLOCK} = 32.768kHz, and T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TC_{SF}	Scale Factor Temperature Coefficient	V_{IN} = 199mV, 0°C ≤ T_A ≤ 70°C (ext. V_{REF} tc = 0ppm)	—	1	5	ppm/°C
Analog Common Section						
V_{CTC}	Analog Common Temperature Coefficient	250KΩ from V+ to Analog Common	—	—	—	—
		0°C ≤ T_A ≤ 70°C	—	—	—	—
		"C" Commercial	—	35	75	ppm/°C
		"I" Industrial	—	35	100	ppm/°C
V_C	Analog Common Voltage	250kΩ from V+ to Analog Common	2.7	3.05	3.35	Volts
Hold Pin Input Section						
	Input Resistance	Pin 1 to Pin 37	—	70	—	kΩ
V_{IL}	Input Low Voltage	Pin 1	—	—	Test +1.5	V
V_{IH}	Input High Voltage	Pin 1	V^+ – 1.5	—	—	V
LCD Drive Section[3]						
V_{SD}	LCD Segment Drive Voltage	V^+ to V_- = 9V	4	5	6	V_{P-P}
V_{SD}	LCD Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
Power Supply						
I_{SUP}	Power Supply Current	V_{IN} = 0V, V^+ to V^- = 9V	—	—	—	—
		f_{OSC} = 16kHz	—	70	100	µA
		f_{OSC} = 48kHz	—	90	125	µA

NOTES:
1. Input voltages may exceed supply voltages when input current is limited to 100µA.
2. Dissipation rating assumes device is mounted with all leads soldered to a printed circuit board.
3. Backplane drive is in phase with the segment drive for "segment off" 180° out of phase for "segment on." Frequency is 20 times the conversion rate. Average DC component is less than 50mV.

PIN CONFIGURATIONS



TC811

PIN DESCRIPTION

Pin No. 40-Pin Plastic DIP	Symbol	Description
1	HLDR	Hold pin, logic 1 holds present display reading.
2	D_1	Activates the D section of the units display.
3	C_1	Activates the C section of the units display.
4	B_1	Activates the B section of the units display.
5	A_1	Activates the A section of the units display.
6	F_1	Activates the F section of the units display.
7	G_1	Activates the G section of the units display.
8	E_1	Activates the E section of the units display.
9	D_2	Activates the D section of the tens display.
10	C_2	Activates the C section of the tens display.
11	B_2	Activates the B section of the tens display.
12	A_2	Activates the A section of the tens display.
13	F_2	Activates the F section of the tens display.
14	E_2	Activates the E section of the tens display.
15	D_3	Activates the D section of the hundreds display.
16	B_3	Activates the B section of the hundreds display.
17	F_3	Activates the F section of the hundreds display.
18	E_3	Activates the E section of the hundreds display.
19	AB_4	Activates both halves of the 1 in the thousands display.
20	POL	Activates the negative polarity display.
21	BP	Backplane drive output.
22	G_3	Activates the G section of the hundreds display.
23	A_3	Activates the A section of the hundreds display.
24	C_3	Activates the C section of the hundreds display.
25	G_2	Activates the G section of the tens display.
26	V^-	Negative power supply voltage.
27	V_{INT}	Integrator output, connection for C_{INT}.
28	V_{BUFF}	Buffer output, connection for R_{INT}.
29	C_{AZ}	Integrator input, connection for C_{AZ}.
30	$V_{IN}-$	Analog input low.
31	$V_{IN}+$	Analog input high.
32	COM	Analog Common: Internal zero reference.
33	$V_{REF}-$	Reference input low.
34	$C_{REF}-$	Negative connection for reference capacitor.
35	$C_{REF}+$	Positive connection for reference capacitor.
36	$V_{REF}+$	Reference input high.
37	TEST	All LCD segment test when pulled high (V^+).
38	V^+	Positive power supply voltage.
39	OSC_2	Crystal oscillator output.
40	OSC_1	Crystal oscillator input.

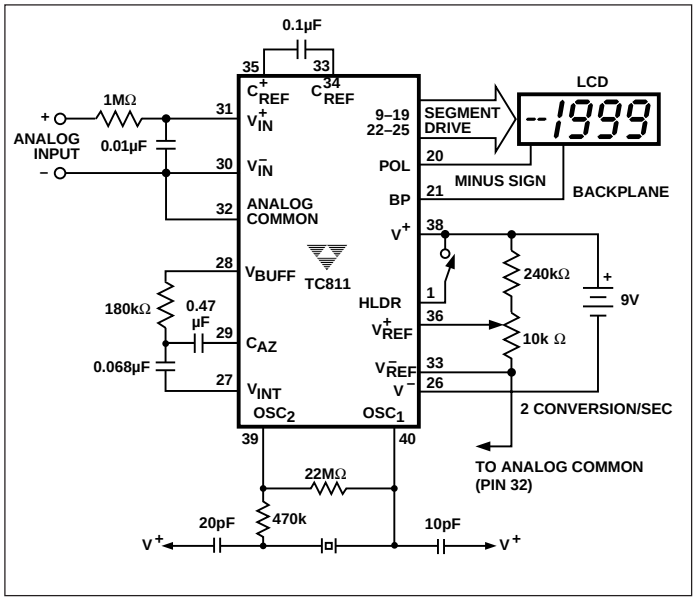


Figure 1. Typical Operating Circuit

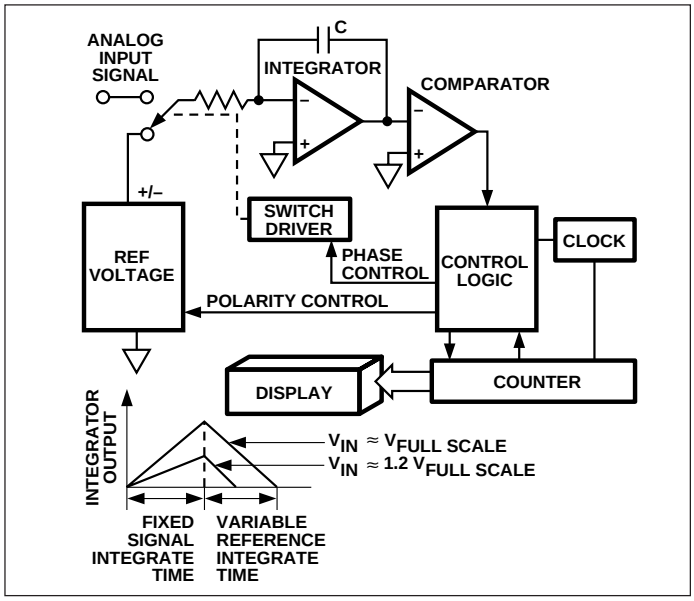


Figure 2. Basic Dual Slope Converter

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

(All Pin Designations Refer to 40-Pin DIP Package)

The TC811 is a dual slope, integrating analog-to-digital converter. An understanding of the dual slope conversion technique will aid the user in following the detailed TC811 theory of operation following this section. A conventional dual slope converter measurement cycle has two distinct phases:

1) Input Signal Integration
2) Reference Voltage Integration (Deintegration)

Referring to Figure 2, the unknown input signal to be converted is integrated from zero for a fixed time period (T_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (deintegration) time (T_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

In a simple dual slope converter, a complete conversion requires the integrator output to “ramp-up” from zero and “ramp-down” back to zero. A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}}\int_{0}^{t_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where:

V_{REF} = Reference voltage
t_{INT} = Integration Time
t_{DEINT} = Deintegration Time

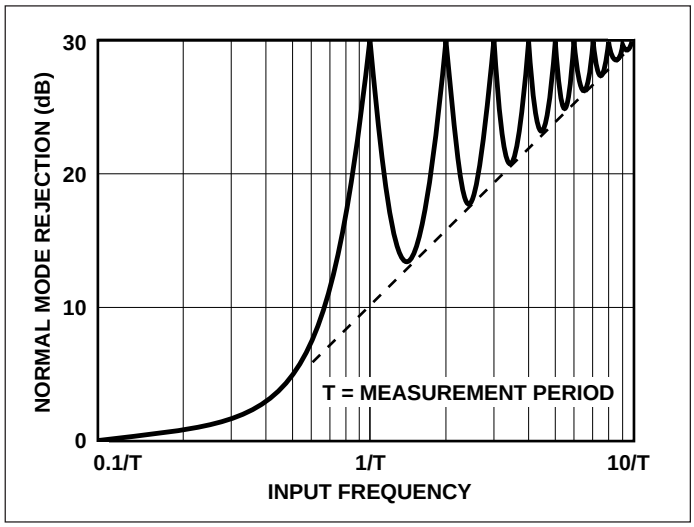


Figure 3. Normal-Mode Rejection of Dual Slope Converter

For a constant V_{INT}:

$$V_{IN} = V_{REF}\left[\frac{t_{DEINT}}{t_{INT}}\right]$$

Accuracy in a dual slope converter is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit of the dual slope technique is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integration ADCs immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated. (see Figure 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60Hz power line period.

THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual-slope cycles discussed above, the TC811 design incorporates an "Integrator Output Zero" cycle and an "Auto Zero" cycle. These additional cycles ensure the integrator starts at 0V (even after a severe overrange conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Integrator Output Zero Cycle
(2) Auto Zero Cycle
(3) Signal Integrate Cycle
(4) Reference Deintegrate Cycle

Integrator Output Zero Cycle

This phase guarantees that the integrator output is at zero volts before the system zero phase is entered, ensuring that the true system offset voltages will be compensated for even after an overrange conversion. The duration of this phase is variable, being a function of the number of counts (clock cycles) required for deintegration.

The Integrator Output Zero cycle will last from 11 to 140 counts for non-over-range conversions and from 31 to 640 counts for overrange conversions.

Auto Zero Cycle

During the Auto Zero cycle, the differential input signal is disconnected from the measurement circuit by opening internal analog switches and the internal nodes are shorted to Analog Common (0V ref.) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages

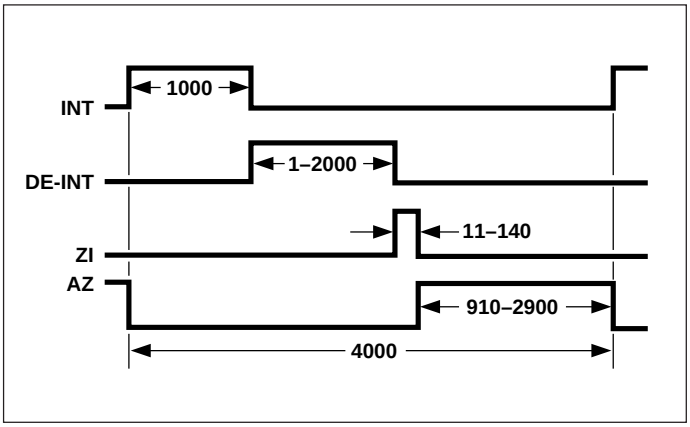


Figure 4a. Conversion Timing During Normal Operation

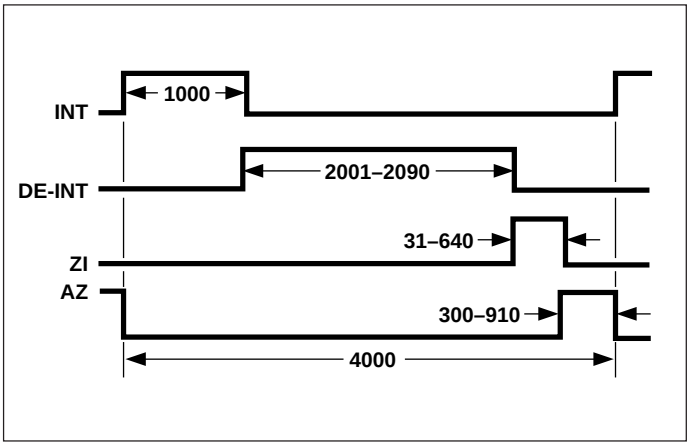


Figure 4b. Conversion Timing During Overrange Operation

during the measurement cycle. The Auto Zero cycle residual is typically 10 to 15μV.

The Auto Zero duration is from 910 to 2,900 counts for non-over-range conversions and from 300 to 910 counts for overrange conversions.

Signal Integration Cycle

Upon completion of the Auto Zero cycle, the Auto Zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is then integrated for a fixed time period which, in the TC811 is 1000 counts (4000 clock periods). The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{INT} = \frac{4000}{f_{OSC}}$$

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground).

If the converter and measured system do not share the same power supply common, as in battery powered applications, V_{IN}^- should be tied to Analog Common.

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication in that signals less than 1 LSB are correctly determined. This allows precision null detection which is limited only by device noise and Auto Zero residual offsets.

Reference Integrate (Deintegrate) Cycle

The reference capacitor, which was charged during the Auto Zero cycle, is connected to the input of the integrating amplifier. The internal sign logic insures that the polarity of the reference voltage is always connected in the phase which is opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate which is determined by the reference potential.

The amount of time required (T_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration cycle:

$$T_{DEINT} = \frac{R_{INT}\, C_{INT}\, V_{INT}}{V_{REF}}$$

The digital reading displayed Is:

$$\text{Digital Count} = 1000\ \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

1) Auto Zero: 300 to 2900 Counts
2) Signal Integrate: 1000 Counts

This time period is fixed. The integration period is:

$$T_{INT} = \frac{4000}{f_{OSC}} = 1000 \text{ Counts}$$

Where f_{OSC} is the crystal oscillator frequency.

3) Reference Integrate: 0 to 2000 Counts
4) Integrator Output Zero: 11 to 640 Counts

The TC811 can replace the ICL7106/26/36 in circuits which require both the hold function and a differential reference. The TC811 offers a greatly improved internal reference temperature coefficient, which can often eliminate the need for an external reference. Some minor component changes are required to upgrade existing designs, reduce power dissipation, and improve the overall performance. (see Oscillator Components)

Digital Section

The TC811 contains all the segment drivers necessary to directly drive a 3-1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal the segment of "OFF". An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}+ and V_{IN}– are reversed then this indicator would reverse.

TEST Function (TEST)

On the TC811, when TEST is pulled to a logical "HIGH", all segments are turned "ON". The display will read "-1888". During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and segment drive assignment are shown in Figure 5.

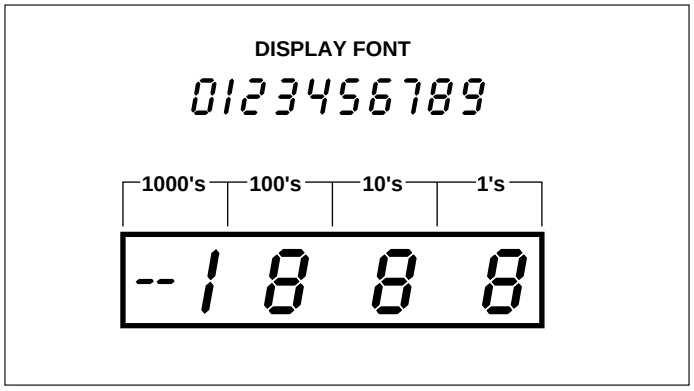


Figure 5. Display FONT and Segment Assignment

HOLD Reading Input (HLDR)

When HLDR is at a logic "HI" the latch will not be updated. Conversions will continue but will not be updated until HLDR is returned to "LOW". To continuously update the display, connect HLDR to ground or leave it open. This input is CMOS compatible and has an internal resistance of 70kΩ (typical) tied to TEST.

COMPONENT VALUE SELECTION

Auto Zero Capacitor - C_{AZ}

The value of the Auto Zero capacitor (C_{AZ}) has some influence on system noise. A 0.47µF capacitor is recommended for 200mV full-scale applications where 1LSB is 100µV. A 0.10µF capacitor should be used for 2.0V full-scale applications. A capacitor with low dielectric absorption (Mylar) is required.

Reference Voltage Capacitor -C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1µF capacitor is typical. If the application requires a sensitivity of 200mV full-scale, increase C_{REF} to 1.0µF. Rollover error will be held to less than 1/2 count. A good quality, low leakage capacitor, such as Mylar, should be used.

Integrating Capacitor - C_{INT}

CINT should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case a ±2V integrator output swing is optimum when the analog input is near full-scale. For 2 or 2.5 reading/second (f_{OSC} = 32kHz or 40kHz) and V_{FS} = 200mV, a .068µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing. An exact expression for C_{INT} is :

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT}\ R_{INT}\ f_{OSC}}$$

where:
f_{OSC} = Clock frequency at Pin 39
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor -R_{INT}

The input buffer amplifier and integrator are designed with class A output stages which have idling currents of 6µA. The integrator and buffer can supply 1µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200mV full-scale, R_{INT} should be about 180kΩ. A 2.0V full-scale requires abut 1.8MΩ.

Oscillator Components

The internal oscillator has been designed to operate with a quartz crystal, such as the Statek CX-1V series. Such crystals are very small and are available in a variety of standard frequencies. Note that f_{OSC} is divided by four to generate the TC811 internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of ac-line noise pickup, a 40kHz crystal should be used. This frequency will yield an integration period of 100msec and will reject both 50Hz and 60Hz noise. For prototyping or cost-sensitive applications a 32.768kHz watch crystal can be used, and will produce about 25dB of line-noise rejection. Other crystal frequencies, from 16kHz to 48kHz, can also be used.

Pins 39 and 40 make up the oscillator section of the TC811. Figures 6a and 6b show some typical conversion rate component values.

The LCD backplane frequency is derived by dividing the oscillator frequency by 800. Capacitive loading of the LCD may compromise display performance if the oscillator is run much over 48kHz.

Reference Voltage (V_{REF})

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

In some applications a scale factor other than unity may exist, such as between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400mV for 2000lb/in^2. Rather than dividing the input voltage by two, the reference voltage should be set to 200mV. This permits the transducer input to be used directly.

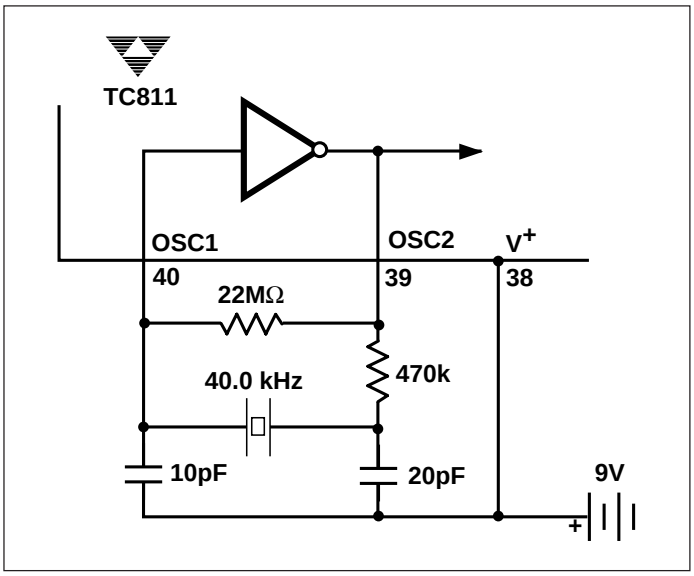


Figure 6a. TC811 Oscillator

Oscillator Freq. (kHz)	Full-Scale Voltage (V_{FS})			
	200mV		2.0V	
	RINT	CINT	RINT	CINT
32.768	180k	0.068µF	1.8M	0.068µF
40	150k	0.068µF	1.5M	0.068µF

Figure 6b.

DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs (V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30))

The TC811 is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V^+ – 1.0 to V^- + 1.5V. Common-mode voltages are removed from the system when the TC811 operates from a battery or floating power source (isolated from measured system) and V_{IN}^- is connected to Analog Common. (see Figure 8)

In systems where common-mode voltages exist, the 86dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 8). For such applications the integrator output swing can be reduced below the recommended 2.0V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increased linearity error.

Reference (V_{REF}^+ (Pin 36), V_{REF}^- (Pin 33)

Unlike the ICL7116, the TC811 has a differential reference as well as the "hold" function. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors such as load cells and temperature sensors. The TC811 is ideally suited to applications in handheld multimeters, panel meters, and portable instrumentation. The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors from being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance. A 0.1µF capacitor is a typical value.

The TC811 offers a significantly improved Analog Common temperature coefficient. This provides a very stable voltage suitable for use as a voltage reference. The temperature coefficient of Analog Common is typically 35ppm/°C.

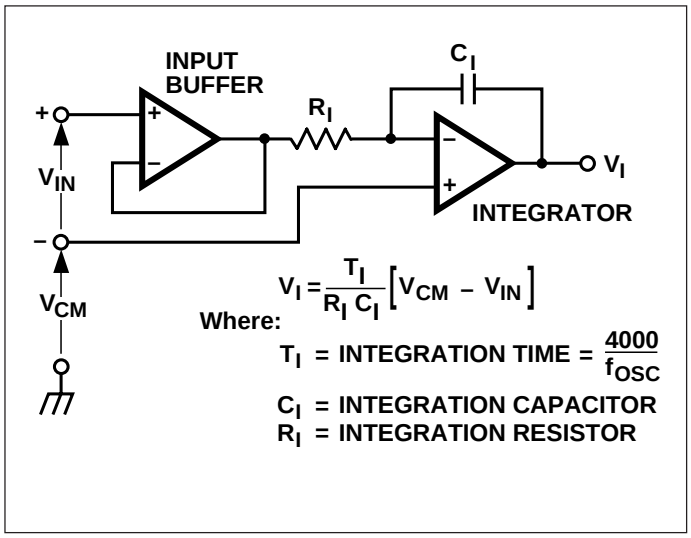


Figure 8. Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

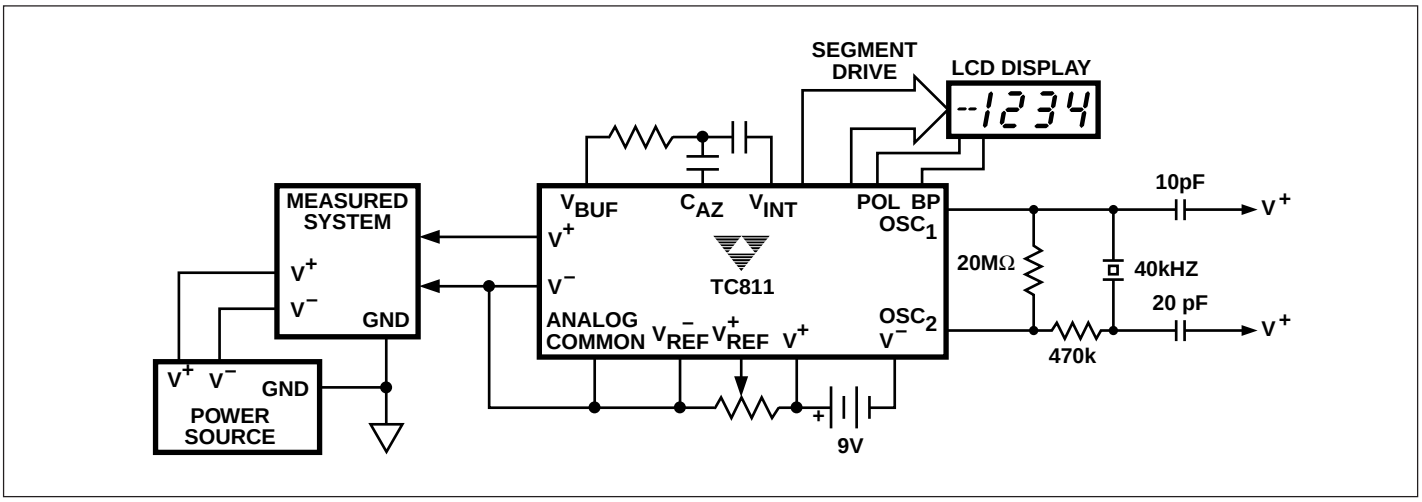


Figure 7. Common-Mode Voltage Removed in Battery Operation With V_{IN}^- = Analog Common

Analog Common (Pin 32)

The Analog Common pin is set at a voltage potential approximately 3.0V below V^+. This potential is guaranteed to be between 2.70V and 3.35V below V^+. Analog common is tied internally to an N channel FET capable of sinking 100µA. This FET will hold the common line at 3.0V below V^+ should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 1µA. Analog common is therefore easily pulled to a more negative voltage (i.e. below V^+– 3.0V).

The TC811 connects the internal V_{IN}^+ and V_{IN}^- inputs to Analog Common during the Auto Zero cycle. During the reference integrate phase V_{IN}^- is connected to Analog Common. If V_{IN}^- is not externally connected to Analog Common, a common-mode voltage exists. This is rejected by the converter's 86dB common-mode rejection ratio. In battery powered applications, Analog Common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, Analog Common should be connected to V_{IN}^-.

The Analog Common pin serves to set the analog section reference or common point. The TC811 is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC811 power source. The Analog Common potential of V^+ – 3.0V gives a 7V end of battery life voltage. The analog common potential has a voltage coefficient of 0.001%/%.

With a sufficiently high total supply voltage ($V^+ – V^- >$ 7.0V), Analog Common is a very stable potential with excellent temperature stability (typically 35ppm/°C). This potential can be used to generate the TC811 reference voltage. An external voltage reference will be unnecessary in most cases because of the 35ppm/°C temperature coefficient. See TC811 Internal Voltage Reference discussion.

TEST (Pin 37)

The TEST pin potential is 5V less the V^+. TEST may be used as the negative power supply connection when interfacing the TC811 to external CMOS logic. The TEST pin is tied to the internally generated negative logic supply through a 500Ω resistor. The TEST pin may be used to sink up to 1mA. See the applications section for additional information on using TEST as a negative digital logic supply.

If TEST is pulled "HIGH" (V^+), all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes, because when TEST is pulled to V^+, the LCD Segments are impressed with a DC voltage which may cause damage to the LCD.

APPLICATIONS INFORMATION

Decimal Point and Annunciator Drive

The TEST pin is connected to the internally generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1mA should be supplied by the TEST pin. The TEST pin potential is approximately 5V below V^+.

Internal Voltage Reference

The TC811 Analog Common voltage temperature stability has been significantly improved. This improved device can be used to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed, however, noise performance will be improved by increasing C_{AZ} (See Auto Zero Capacitor section). Figure 10 shows Analog Common supplying the necessary voltage reference for the TC811.

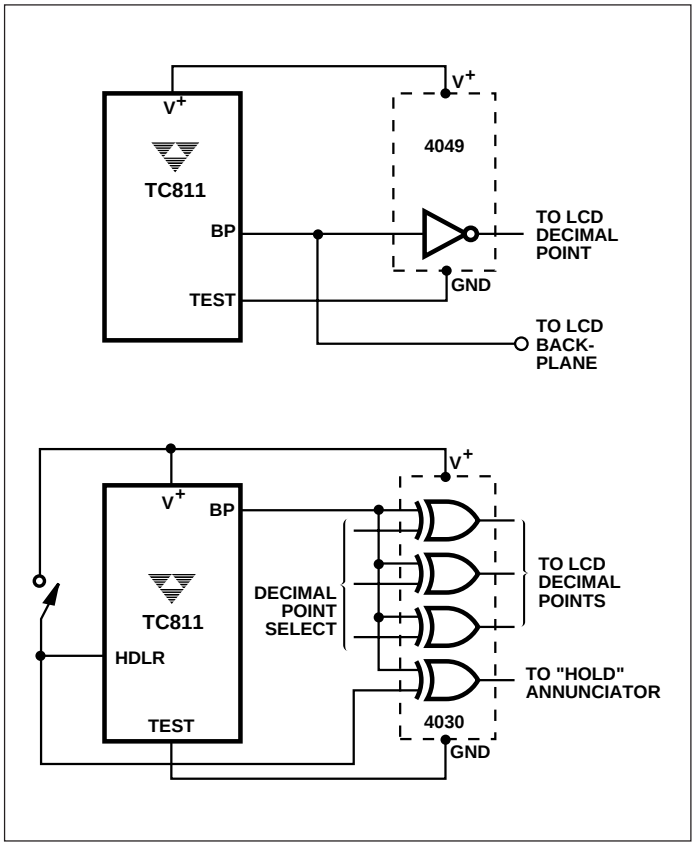


Figure 9. Display Annunciator Drivers

Liquid Crystal Display Sources

Several LCD manufactures supply standard LCD displays to interface with the TC811 3-1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415-347-9916	FE 0801, FE 0203
EPSON	3415 Kashikawa St., Torrence, CA 90505 212-534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414-648-2361	3902, 3933, 3903

*NOTE: Contact LCD manufacturer for full product listing/specifications.

Oscillator Crystal Source

Manufacturer	Address/Phone	Representative Part Numbers
STATEK	512 N-Main Orange, CA 92668 714-639-7810	CX-1V 40.0

Ratiometric Resistance Measurements

The TC811 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 11). The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

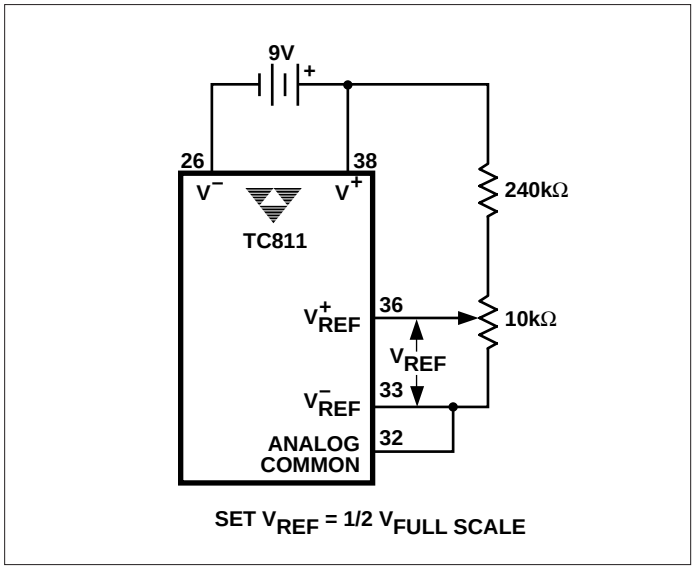


Figure 10. TC811 Internal Voltage Reference Connection

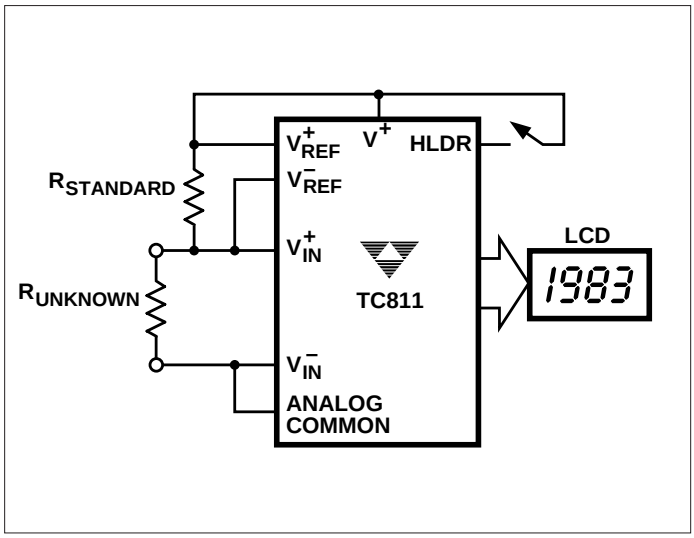


Figure 11. Low Parts Count Ratio Metric Resistance Measurement

TC811

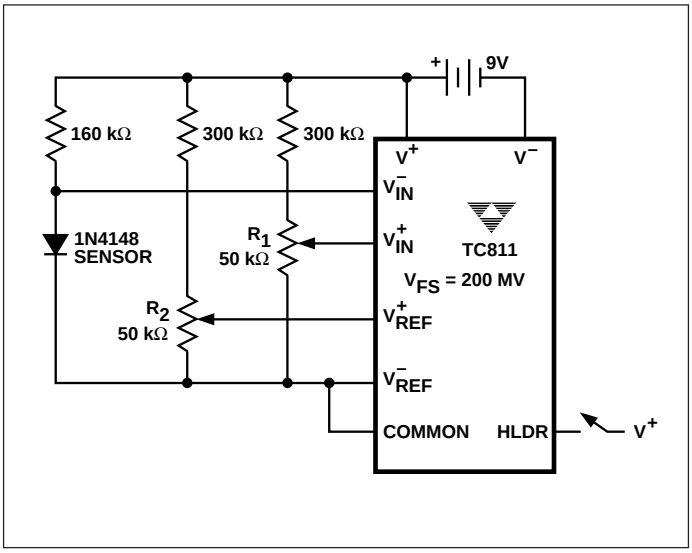


Figure 12. Temperature Sensor

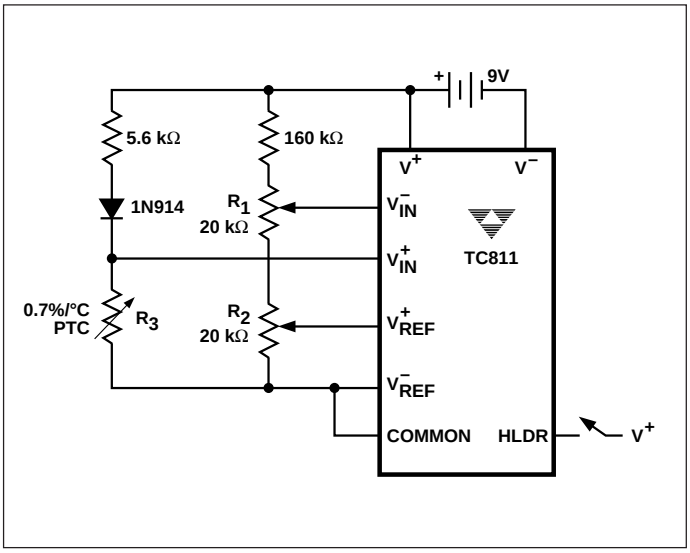


Figure 13. Positive Temperature Coefficient Resistor Temperature Sensor