BURR-BROWN®

PCM1800

Single-Ended Analog Input 20-Bit Stereo ANALOG-TO-DIGITAL CONVERTER

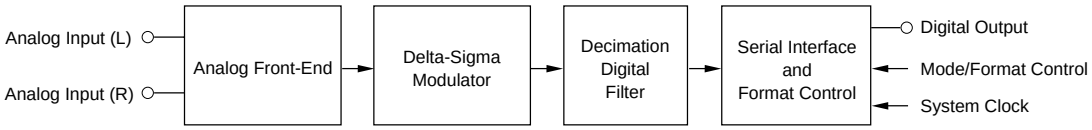
FEATURES

- **DUAL 20-BIT MONOLITHIC ΔΣ ADC**
- **SINGLE-ENDED VOLTAGE INPUT**
- **64X OVERSAMPLING DECIMATION FILTER:**
  Passband Ripple: ±0.05dB
  Stopband Attenuation: –65dB
- **HIGH PERFORMANCE:**
  THD+N: -88dB (typ)
  SNR: 95dB (typ)
  Dynamic Range: 95dB (typ)
  Internal High Pass Filter
- **PCM AUDIO INTERFACE:**
  Master/Slave Modes
  4 Data Formats
- **SAMPLING RATE: 32kHz, 44.1kHz, 48kHz**
- **SYSTEM CLOCK: 256f_S, 384f_S, or 512f_S**
- **SINGLE +5V POWER SUPPLY**
- **SMALL 24-PIN SSOP PACKAGE**

DESCRIPTION

PCM1800 is a low cost, single chip stereo analog-to-digital converter with single-ended analog voltage inputs. The PCM1800 uses a delta-sigma modulator with 64X oversampling, including a digital decimation filter and serial interface which supports both Master and Slave Modes and four data formats. PCM1800 is suitable for a wide variety of cost-sensitive consumer applications where high performance is required.

PCM1800 is fabricated on a highly advanced CMOS process.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1387
Printed in U.S.A. August, 1997

SPECIFICATIONS

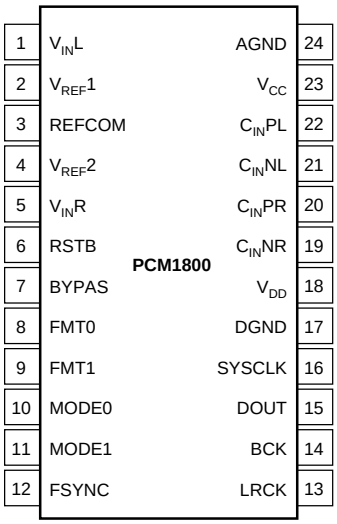
All specifications at +25°C, $+V_{DD}$ = $+V_{CC}$ = +5V, f_S = 44.1kHz, and 20-bit input data, SYSCLK = 384f_S, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1800E MIN	PCM1800E TYP	PCM1800E MAX	UNITS
RESOLUTION		20			Bits
DIGITAL INPUT/OUTPUT					
Input Logic Level:					
V_{IH}(1)		2.0			V
V_{IL}(1)				0.8	V
Input Logic Current:					
I_{IN}(2)				±1	µA
I_{IN}(3)				+100	µA
Output Logic Level:					
V_{OH}(4)	I_{OH} = –1.6mA	4.5			V
V_{OL}(4)	I_{OL} = +3.2mA			0.5	V
Sampling Frequency		32	44.1	48	kHz
System Clock Frequency	256f_S	8.1920	11.2896	12.2880	MHz
	384f_S	12.2880	16.9344	18.4320	MHz
	512f_S	16.3840	22.5792	24.5760	MHz
DC ACCURACY					
Gain Mismatch Channel-to-Channel			±1.0	±2.5	% of FSR
Gain Error			±2.0	±5.0	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error	High Pass Filter Bypass		±2.0		% of FSR
Bipolar Zero Drift	High Pass Filter Bypass		±20		ppm of FSR/°C
DYNAMIC PERFORMANCE(5)					
THD+N at FS (–0.5dB)			–88	–80	dB
THD+N at –60dB			–92		dB
Dynamic Range	EIAJ, A-weighted	90	95		dB
Signal-To-Noise Ratio	EIAJ, A-weighted	90	95		dB
Channel Separation		88	93		dB
DYNAMIC PERFORMANCE(5)					
Dynamic Range	16-Bit, A-weighted		94		dB
Signal-To-Noise Ratio	16-Bit, A-weighted		94		dB
Channel Separation	16-Bit		92		dB
ANALOG OUTPUT					
Input Range	FS (V_{IN} = 0dB)		2.828		Vp-p
Center Voltage			2.1		V
Input Impedance			30		kΩ
Anti-Aliasing Filter Frequency Response	C_{EXT} = 470pF, –3dB		170		kHz
DIGITAL FILTER PERFORMANCE					
Passband				0.454f_S	Hz
Stopband		0.583f_S			Hz
Passband Ripple				±0.05	dB
Stopband Attenuation		–65			dB
Delay Time (Latency)			17.4/f_S		sec
High Pass Frequency Response	–3dB			0.019f_S	mHz
POWER SUPPLY REQUIREMENTS					
Voltage Range	$+V_{CC}$	+4.5	+5.0	+5.5	VDC
	$+V_{DD}$	+4.5	+5.0	+5.5	VDC
Supply Current(6)	$+V_{CC}$ = $+V_{DD}$ = +5V		18	25	mA
Power Dissipation	$+V_{CC}$ = $+V_{DD}$ = +5V		90	125	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTES: (1) Pins 6, 7, 8, 9, 10, 11, 16 and 12, 13, 14: RSTB, BYPAS, FMT0, FMT1, MODE0, MODE1, SYSCLK, and FSYNC, LRCK, BCK under Slave Mode. (2) Pins 16 and 12, 13, 14: SYSCLK and FSYNC, LRCK, BCK under Slave Mode (Schmitt Trigger input). (3) Pins 6, 7, 8, 9, 10, 11: RSTB, BYPAS, FMT0, FMT1, MODE0, MODE1 (Schmitt Trigger input, with 100kΩ typical pull-down resistor). (4) Pins 15 and 12, 13, 14: DOUT and FSYNC, LRCK, BCK under Master Mode. (5) f_{IN} = 1kHz, using Audio Precisions System II, rms Mode with 20kHz LPF and 400Hz HPF in calculation. (6) No load on DOUT (pin 15) in the Slave Mode.

PIN CONFIGURATION

Top View SSOP



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1800E	24-Pin SSOP	338

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage: $+V_{DD}$, $+V_{CC}$	+6.5V
Supply Voltage Differences	±0.1V
GND Voltage Differences	±0.1V
Digital Input Voltage	–0.3V to (V_{DD} + 0.3V)
Analog Input Voltage	–0.3V to (V_{CC} + 0.3V)
Input Current (any pin except supplies)	±10mA
Power Dissipation	300mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
(reflow, 10s)	+235°C

PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	$V_{IN}L$	IN	Analog Input, Lch
2	$V_{REF}1$	—	Reference 1 Decoupling Capacitor
3	REFCOM	—	Reference Decoupling Common
4	$V_{REF}2$	—	Reference 2 Decoupling Capacitor
5	$V_{IN}R$	IN	Input Reference, Rch
6	RSTB	IN	Reset Input, Active LOW(1)
7	BYPAS	IN	High Pass Filter Bypass Control(1)
8	FMT0	IN	Audio Data Format 0(1)
9	FMT1	IN	Audio Data Format 1(1)
10	MODE0	IN	Master/Slave Mode Selection 0(1)
11	MODE1	IN	Master/Slave Mode Selection 1(1)
12	FSYNC	IN/OUT	Frame Synchronization
13	LRCK	IN/OUT	Sampling Clock Input/Output (f_S)
14	BCK	IN/OUT	Bit Clock Input/Output
15	DOUT	OUT	Audio Data Output
16	SYSCLK	IN	System Clock Input, 256f_S, 384f_S, or 512f_S
17	DGND	—	Digital Ground
18	V_{DD}	—	Digital Power Supply
19	$C_{IN}NR$	—	Anti-alias Filter Capacitor (–), Rch
20	$C_{IN}PR$	—	Anti-alias Filter Capacitor (+), Rch
21	$C_{IN}NL$	—	Anti-alias Filter Capacitor (–), Lch
22	$C_{IN}PL$	—	Anti-alias Filter Capacitor (+), Lch
23	V_{CC}	—	Analog Power Supply
24	AGND	—	Analog Ground

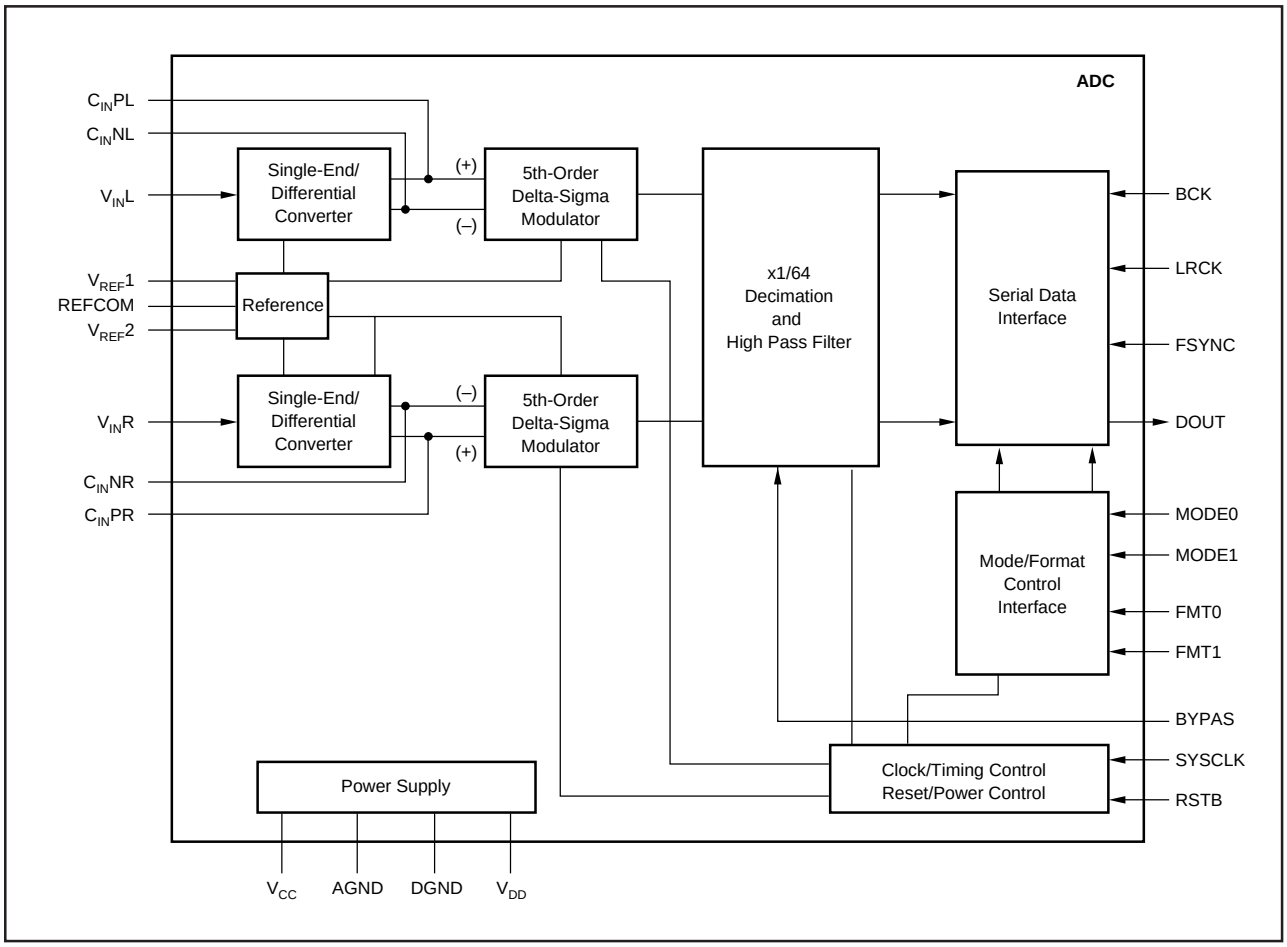
NOTE: (1) With 100kΩ typical pull-down resistor.

ELECTROSTATIC DISCHARGE SENSITIVITY

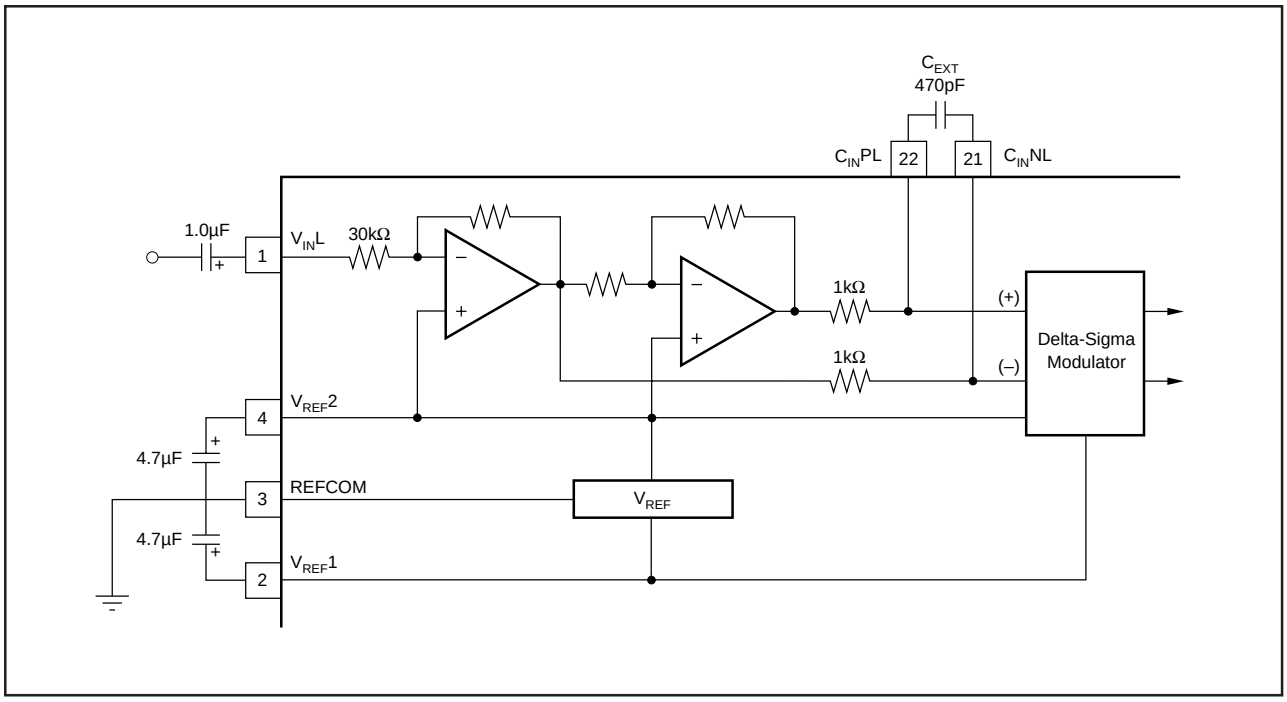
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BLOCK DIAGRAM



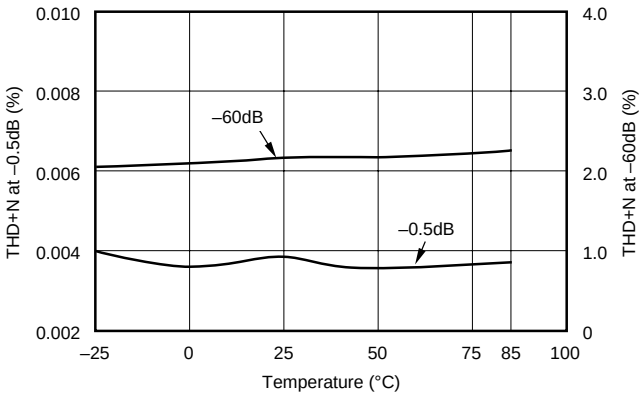
ANALOG FRONT-END (Single-Channel)



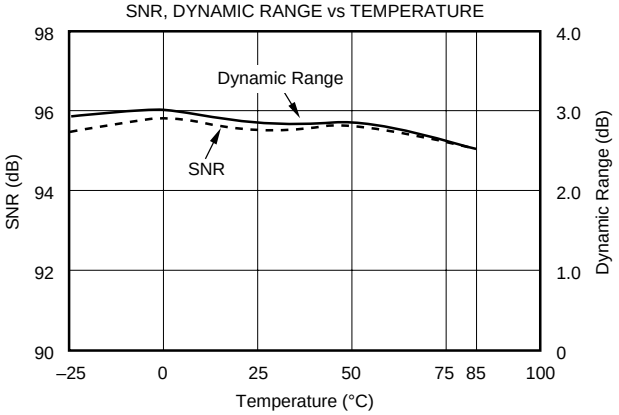
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, $+V_{DD}$ = $+V_{CC}$ = +5V, f_S = 44.1kHz, and 20-bit input data, SYSCLK = 384f_S, unless otherwise noted.

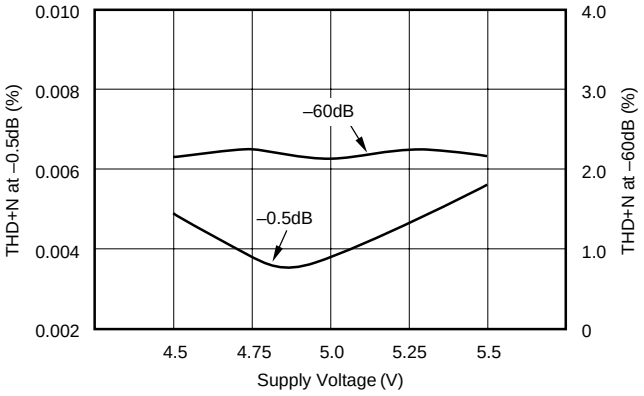
THD+N vs TEMPERATURE



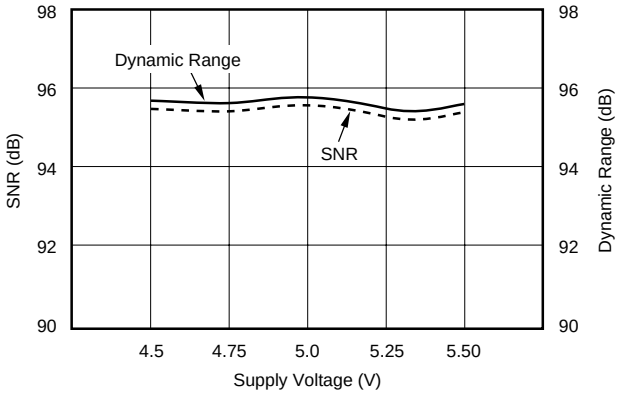
SNR, DYNAMIC RANGE vs TEMPERATURE



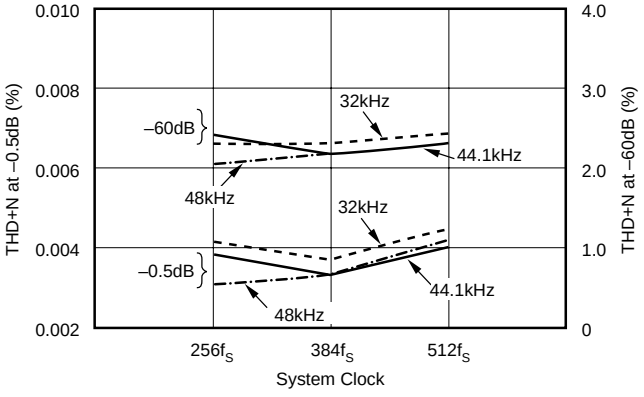
THD+N vs POWER SUPPLY



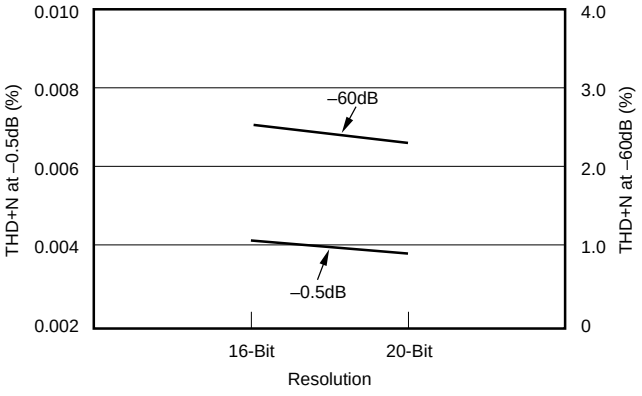
SNR and DYNAMIC RANGE vs POWER SUPPLY



THD+N vs SYSTEM CLOCK
and SAMPLING FREQUENCY

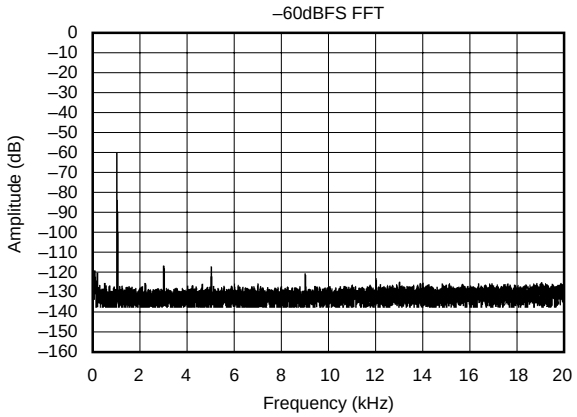


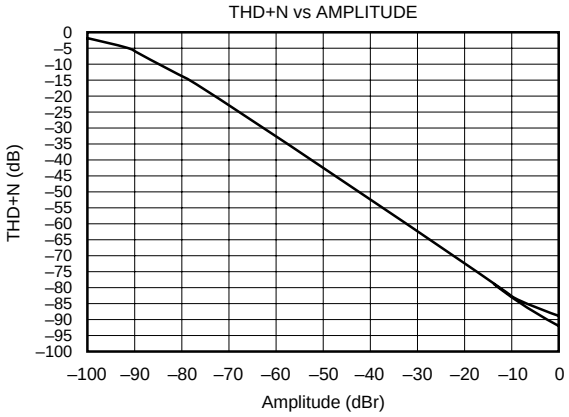
THD+N vs OUTPUT DATA RESOLUTION

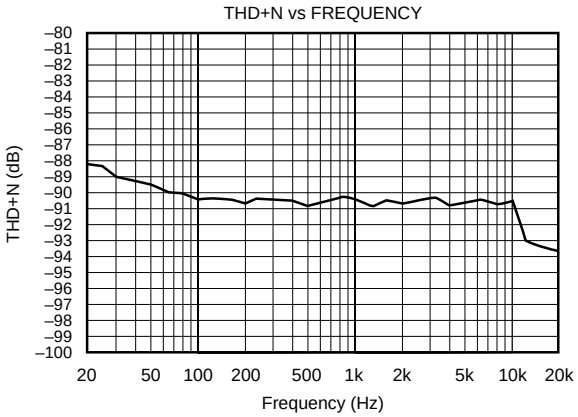


TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $+V_{DD}$ = $+V_{CC}$ = +5V, f_S = 44.1kHz, and 20-bit input data, SYSCLK = 384f_S, unless otherwise noted.



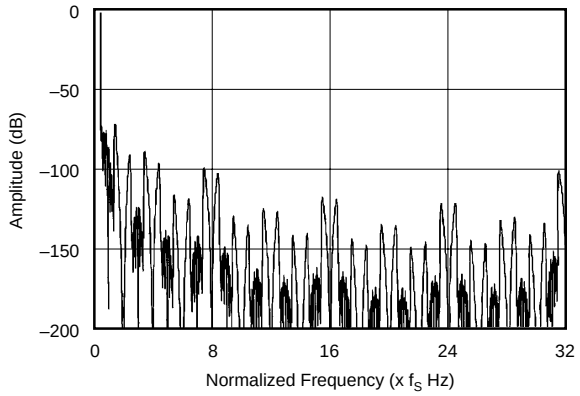




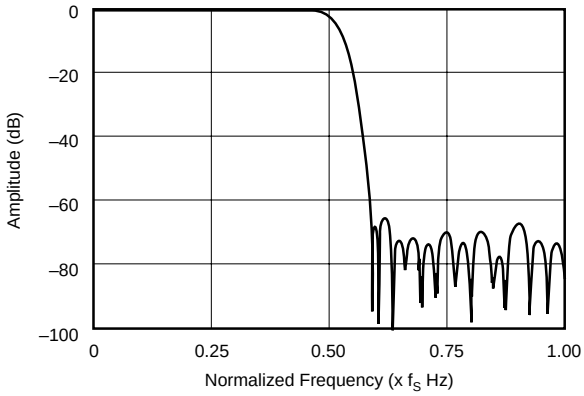
TYPICAL PERFORMANCE CURVES

DIGITAL FILTER

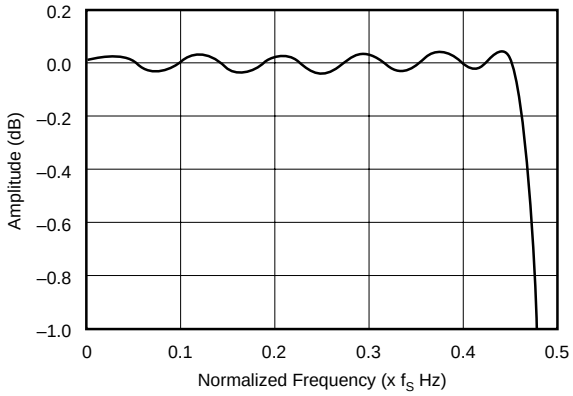
OVERALL CHARACTERISTICS



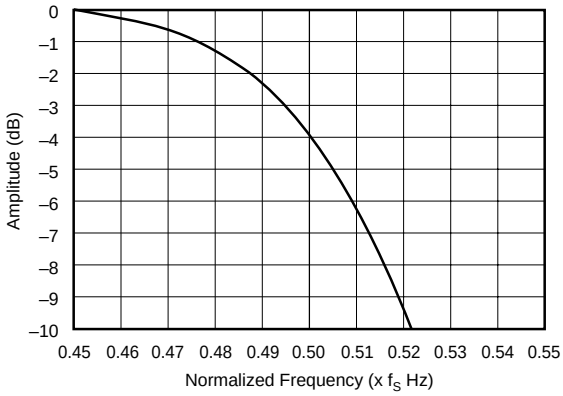
STOPBAND ATTENUATION CHARACTERISTICS



PASSBAND RIPPLE CHARACTERISTICS

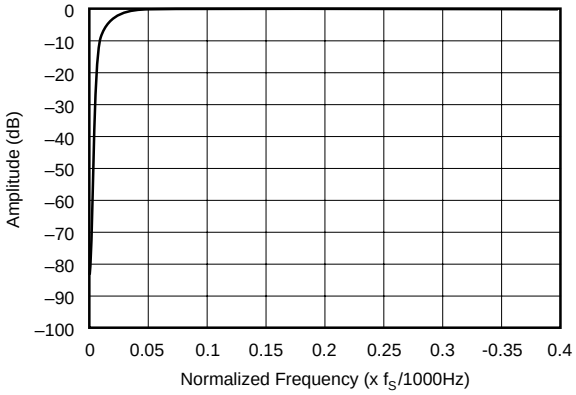


TRANSIENT BAND CHARACTERISTICS

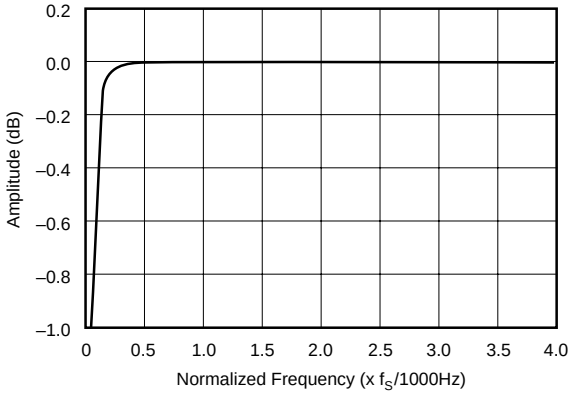


HIGH PASS FILTER

HIGH PASS FILTER RESPONSE



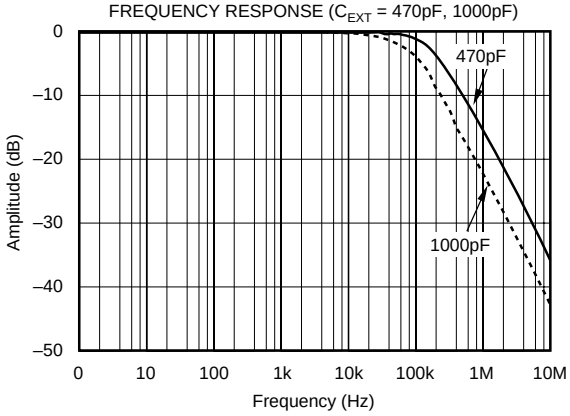
HIGH PASS FILTER RESPONSE



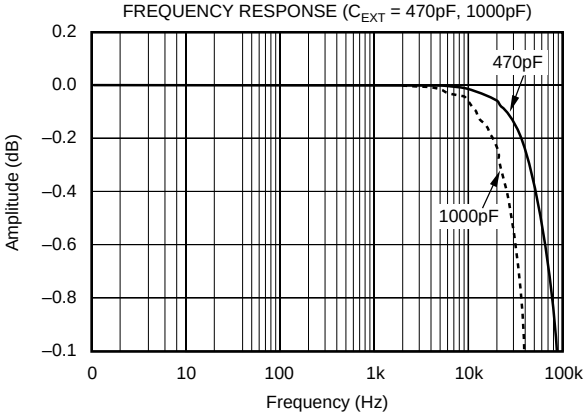
TYPICAL PERFORMANCE CURVES

ANTI-ALIASING FILTER

ANTI-ALIASING FILTER OVERALL
FREQUENCY RESPONSE (C_{EXT} = 470pF, 1000pF)



ANTI-ALIASING FILTER PASSBAND
FREQUENCY RESPONSE (C_{EXT} = 470pF, 1000pF)



THEORY OF OPERATION

PCM1800 consists of a bandgap reference, two channels of a single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The Block Diagram illustrates the total architecture of PCM1800, the Analog Front-End diagram illustrates the architecture of the single-to-differential converter, and the anti-aliasing filter is illustrated in the Block Diagram. Figure 1 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

An internal high precision reference with two external capacitors provides all reference voltages which are required by the converter, and defines the full-scale voltage range of both channels. The internal single-to-differential voltage converter saves the design, space and extra parts needed for external circuitry required by many delta-sigma converters. The internal full differential architecture provides a wide dynamic range and excellent power supply rejection performance.

The input signal is sampled at 64X oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying anti-alias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator and a feedback loop consisting of a 1-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The $64f_S$, 1-bit stream from the modulator is converted to $1f_S$, 20-bit digital data by the decimation filter, which also acts as a low pass filter to remove the shaped quantization noise. The DC components are removed by a high pass filter, and the filtered output is converted to time-multiplexed serial signals through a serial interface which provides flexible serial formats and Master/Slave Modes.

SYSTEM CLOCK

The system clock for PCM1800 must be either $256f_S$, $384f_S$, or $512f_S$, where f_S is the audio sampling frequency. The system clock must be supplied on SYSCLK (pin 16).

PCM1800 also has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$, $384f_S$, or $512f_S$.

When $384f_S$ and $512f_S$ system clock is in Slave Mode, the system clock is divided into $256f_S$ automatically. The $256f_S$ clock is used to operate the digital filter and the modulator. Table I lists the relationship of typical sampling frequencies and system clock frequencies. Figure 2 illustrates the system clock timing.

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	$256f_S$	$384f_S$	$512f_S$
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9340	22.5792
48	12.2880	18.4320	24.5760

TABLE I. System Clock Frequencies.

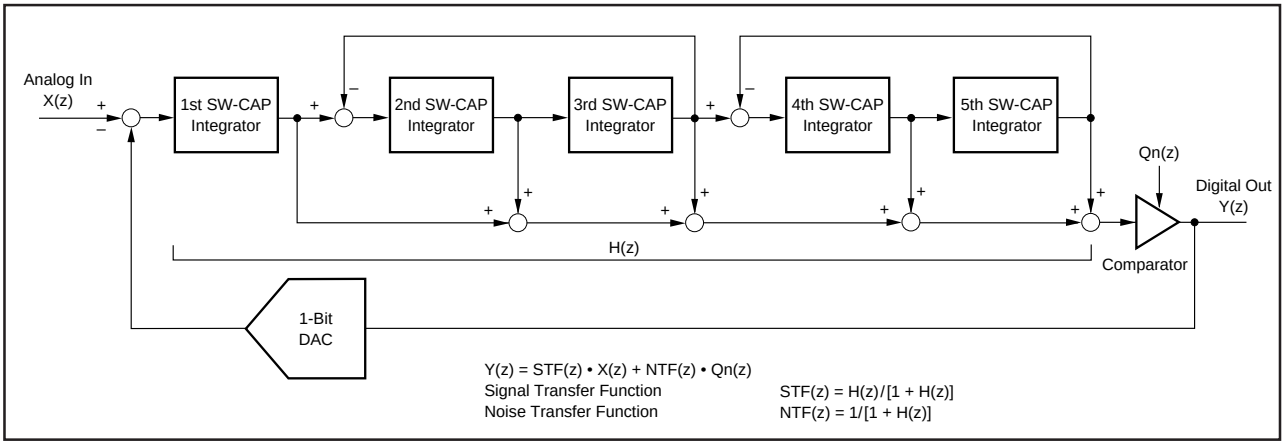


FIGURE 1. Simplified Diagram of the PCM1800 5th-Order Delta-Sigma Modulator.

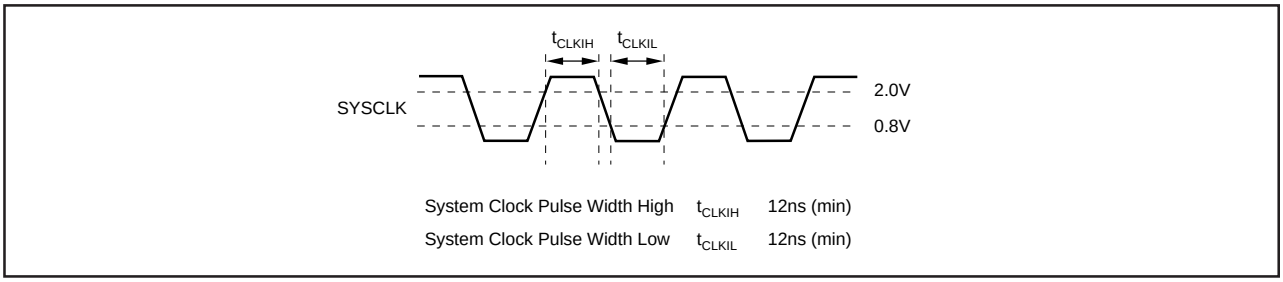


FIGURE 2. System Clock Timing.

RESET

PCM1800 has both an internal power-on reset circuit and an external forced reset (RSTB, pin 6). The internal power-on reset initializes (resets) when the supply voltage (V_{CC}/V_{DD}) exceeds 4.0V (typ). To initiate the reset sequence externally, apply a logic level LOW to the RSTB pin.

The RSTB pin is terminated by an internal pull-down resistor. If the RSTB pin is unconnected, the ADC will remain in the reset state. During V_{CC}/V_{DD} < 4.0V (typ), RSTB = LOW and 1024 system clock periods after V_{CC}/V_{DD} 4.0V and RSTB = HIGH. The PCM1800 stays in the reset state and the digital output is forced to zero. The digital output is valid after reset state release and $18436f_S$ periods. During reset, the logic circuits and the digital filter stop operating. Figures 3 and 4 illustrate the internal power-on reset and external reset timing.

SERIAL AUDIO DATA INTERFACE

The PCM1800 interfaces the audio system through BCK (pin 14), LRCK (pin 13), FSYNC (pin 12) and DOUT (pin 15).

INTERFACE MODE

The PCM1800 supports Master and Slave Modes as interface modes and are selected by MODE1 (pin 11) and MODE0 (pin 10), as shown in Table II. In case of the Master Mode, the PCM1800 provides the timing of serial audio data communications between the PCM1800 and the digital audio processor or external circuit. While in the case of the Slave Mode, the PCM1800 receives the timing of data transfer from an external controller.

MODE1	MODE0	INTERFACE MODE
0	0	Slave Mode ($256/384/512f_S$)
0	1	Master Mode ($512f_S$)
1	0	Master Mode ($384f_S$)
1	1	Master Mode ($256f_S$)

TABLE II. Interface Modes.

Master Mode

In the Master Mode, BCK, LRCK, and FSYNC are output pins and are controlled by timing generated in clock circuitry of the PCM1800.

FSYNC is used to designate the valid data from the PCM1800. The rising edge of FSYNC indicates the starting point of the converted audio data and the following edge of this signal indicates the ending points of data. The frequency of this signal is fixed at 2xLRCK and duty cycle ratio depends on data bit length. The frequency of BCK is fixed at 64X LRCK.

Slave Mode

In Slave Mode, BCK, LRCK, and FSYNC are input pins. FSYNC is used to enable BCK signal, and the PCM1800 can shift out the converted data when FSYNC is HIGH.

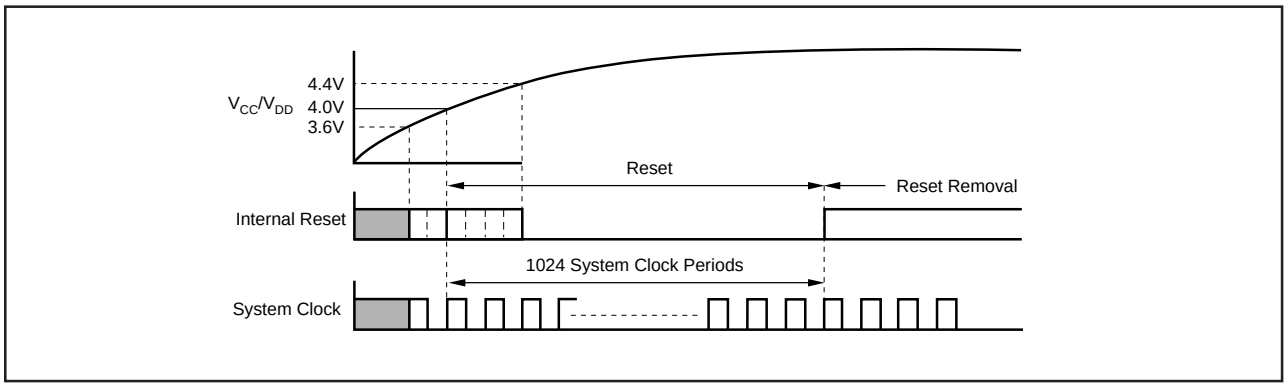


FIGURE 3. Internal Power-On Reset Timing.

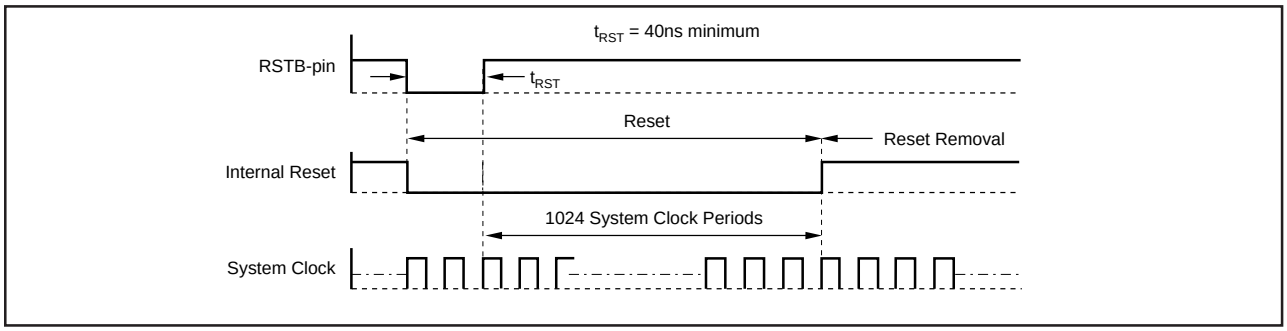


FIGURE 4. RSTB-Pin Reset Timing.

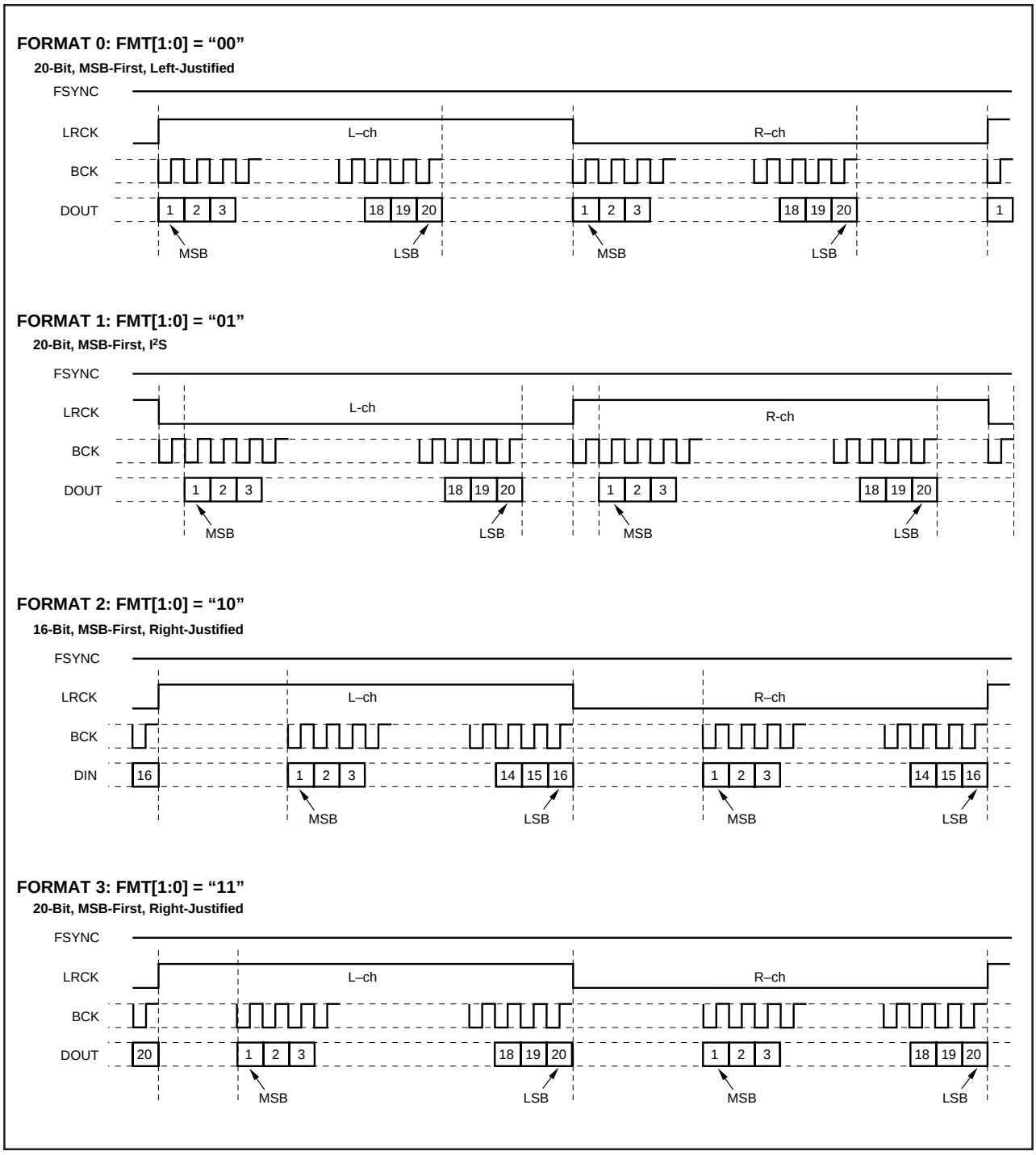


FIGURE 5. Audio Data Format (Slave Mode: FSYNC, LRCK, and BCK are inputs).

DATA FORMAT

PCM1800 supports four audio data formats in both Master and Slave Modes, and are selected by FMT1 (pin 9) and FMT0 (pin 8), as shown in Table III.

FORMAT #	FMT1	FMT0	DATA FORMAT
0	0	0	20-bit, Left-justified
1	0	1	20-bit, I²S
2	1	0	16-bit, Right-justified
3	1	1	20-bit, Right-justified
NOTE: FMT1 and FMT0 must be stable at RSTB changing from LOW to HIGH.			

TABLE III. Data Format.

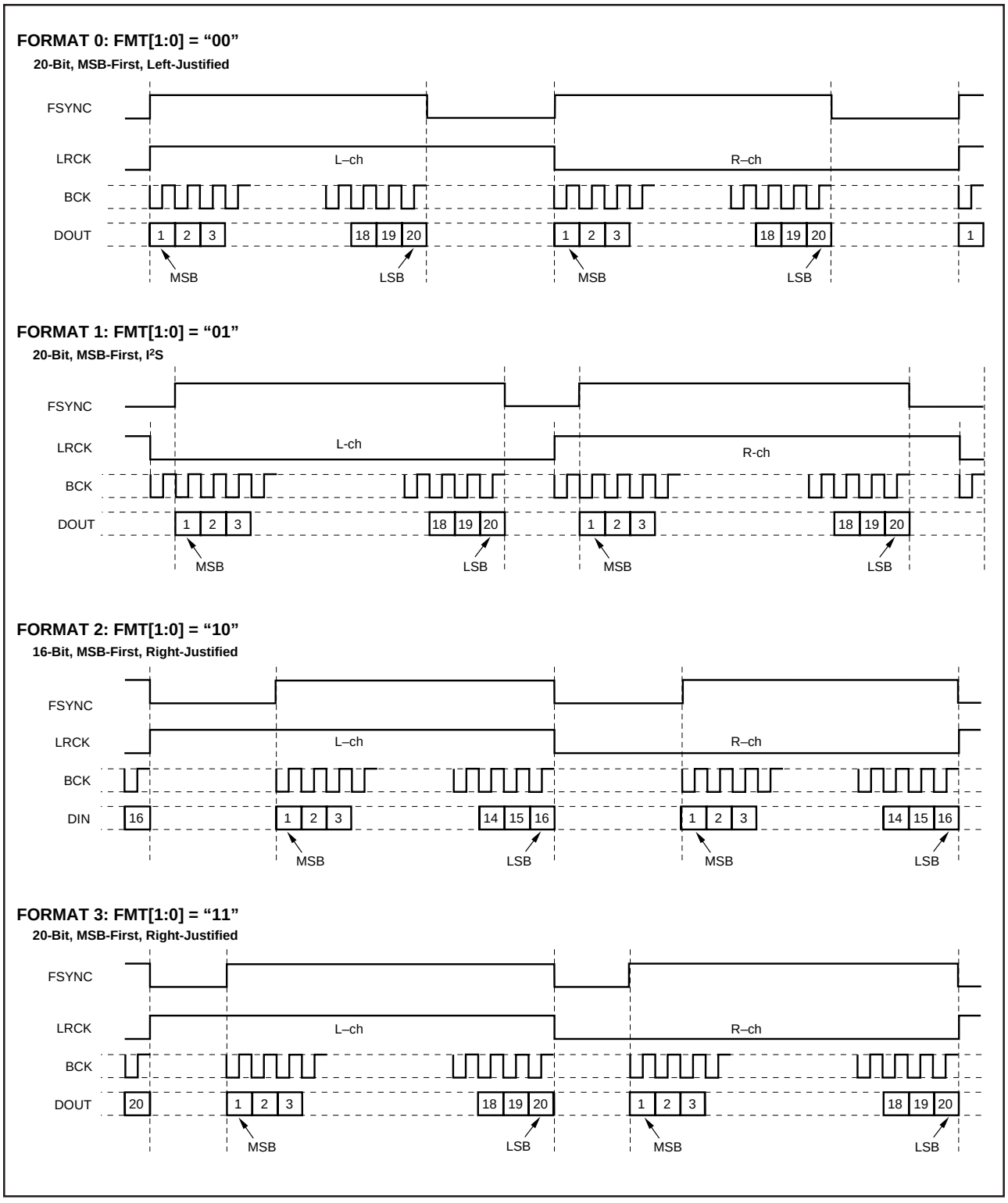
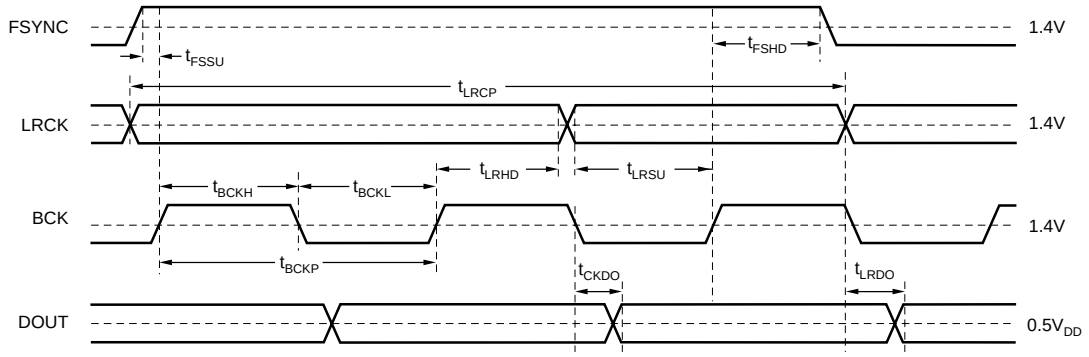


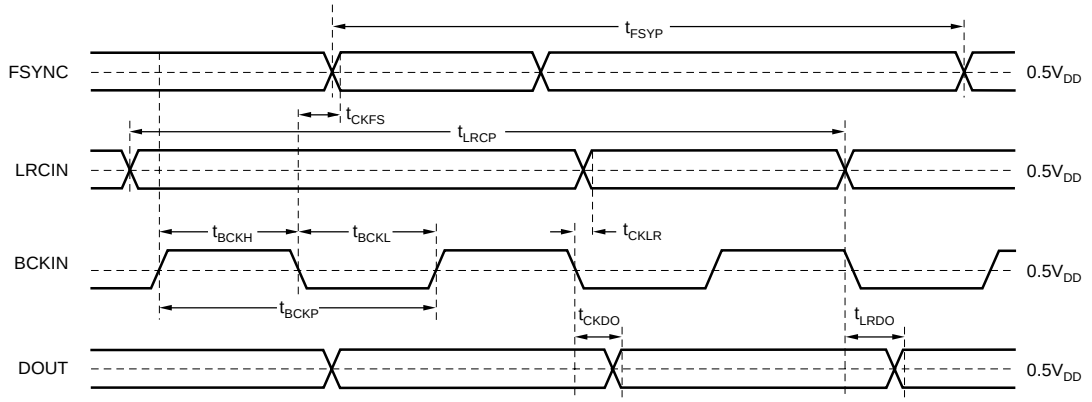
FIGURE 6. Audio Data Format (Master Mode: FSYNC, LRCK, and BCK are outputs).



DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
BCK Period	t_{BCKP}	300			ns
BCK Pulsewidth HIGH	t_{BCKH}	120			ns
BCK Pulsewidth LOW	t_{BCKL}	120			ns
LRCK Set Up Time to BCK Rising Edge	t_{LRSU}	80			ns
LRCK Hold Time to BCK Rising Edge	t_{LRHD}	40			ns
LRCK Period	t_{LRCP}	20			µs
FSYNC Set Up Time to BCK Rising Edge	t_{FSSU}	40			ns
FSYNC Hold Time to BCK Rising Edge	t_{FSHD}	40			ns
Delay Time BCK Falling Edge to DOUT Valid	t_{CKDO}	–20		40	ns
Delay Time LRCK Edge to DOUT Valid	t_{LRDO}	–20		40	ns
Rising Time of All Signals	t_{RISE}			20	ns
Falling Time of All Signals	t_{FALL}			20	ns

NOTE: Timing measurement reference level is $(V_{IH}/V_{IL})/2$. Rising and falling time is measured from 10% to 90% of I/O signals' swing. Load capacitance of DOUT signal is 20pF.

FIGURE 7. Audio Data Interface Timing (Slave Mode: FSYNC, LRCK, and BCK are inputs).



DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
BCK Period	t_{BCKP}	300	1/64f_S	600	ns
BCK Pulsewidth HIGH	t_{BCKH}	150		300	ns
BCK Pulsewidth LOW	t_{BCKL}	150		300	ns
Delay Time BCK Falling Edge to LRCK Valid	t_{CKLR}	–20		40	ns
LRCK Period	t_{LRCP}	20	1/f_S	40	µs
Delay Time BCK Falling Edge to FSYNC Valid	t_{CKFS}	–20		40	ns
FSYNC Period	t_{FSYP}	10	1/2 f_S	40	µs
Delay Time BCK Falling Edge to DOUT Valid	t_{CKDO}	–20		40	ns
Delay Time LRCK Edge to DOUT Valid	t_{LRDO}	–20		40	ns
Rising Time of All Signals	t_{RISE}			20	ns
Falling Time of All SIgnals	t_{FALL}			20	ns

NOTE: Timing measurement reference level is $(V_{IH}/V_{IL})/2$. Rising and falling time is measured from 10% to 90% of I/O signals' swing. Load capacitance of DOUT signal is 20pF.

FIGURE 8. Audio Data Interface Timing (Master Mode: FSYNC, LRCK, and BCK are outputs).

SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

In Slave Mode, PCM1800 operates with LRCK synchronized to the system clock (SYSCLK). PCM1800 does not require a specific phase relationship between LRCK and SYSCLK, but does require the synchronization of LRCK and SYSCLK. If the relationship between LRCK and SYSCLK changes more than 6 bit clocks (BCK) during one sample period due to LRCK or SYSCLK jitter, internal operation of the ADC halts within $1/f_S$ and digital output is forced into BPZ code until resynchronization between LRCK and SYSCLK is completed. In case of changes less than 5 bit clocks (BCK), resynchronization does not occur and above digital output control and discontinuity does not occur.

ADC DATA OUTPUT AT RESET

Figures 9 and 10 illustrate the ADC digital output when the reset operation is done and synchronization is lost. During undefined data, it may generate some noise in the audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal makes a discontinuity of data on the digital output, and may generate some noise in the audio signal.

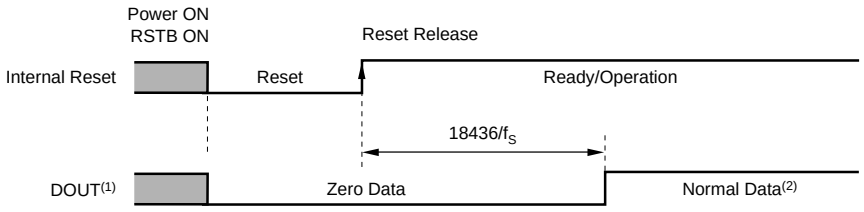
BOARD DESIGN AND LAYOUT CONSIDERATIONS

V_{CC}, V_{DD} PINS

The digital and analog power supply lines to the PCM1800 should be bypassed to the corresponding ground pins with both 0.1µF ceramic and 10µF tantalum capacitors as close to the pins as possible to maximize the dynamic performance of the ADC. Although PCM1800 has two power lines to maximize the potential of dynamic performance, using one common power supply is recommended to avoid unexpected power supply problems, such as latch-up or power supply sequence.

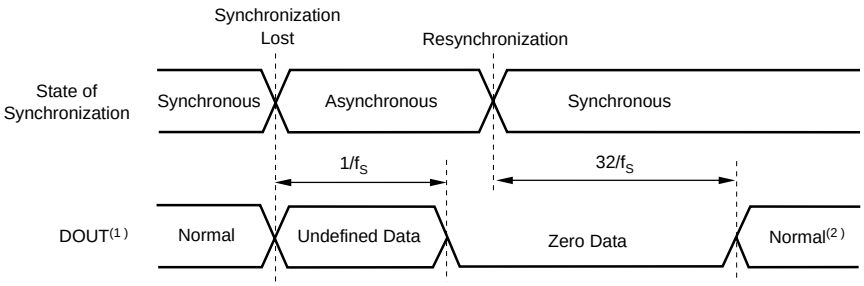
AGND, DGND PINS

To maximize the dynamic performance of the PCM1800, the analog and digital grounds are not internally connected. These points should have very low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the parts to reduce potential noise problems.



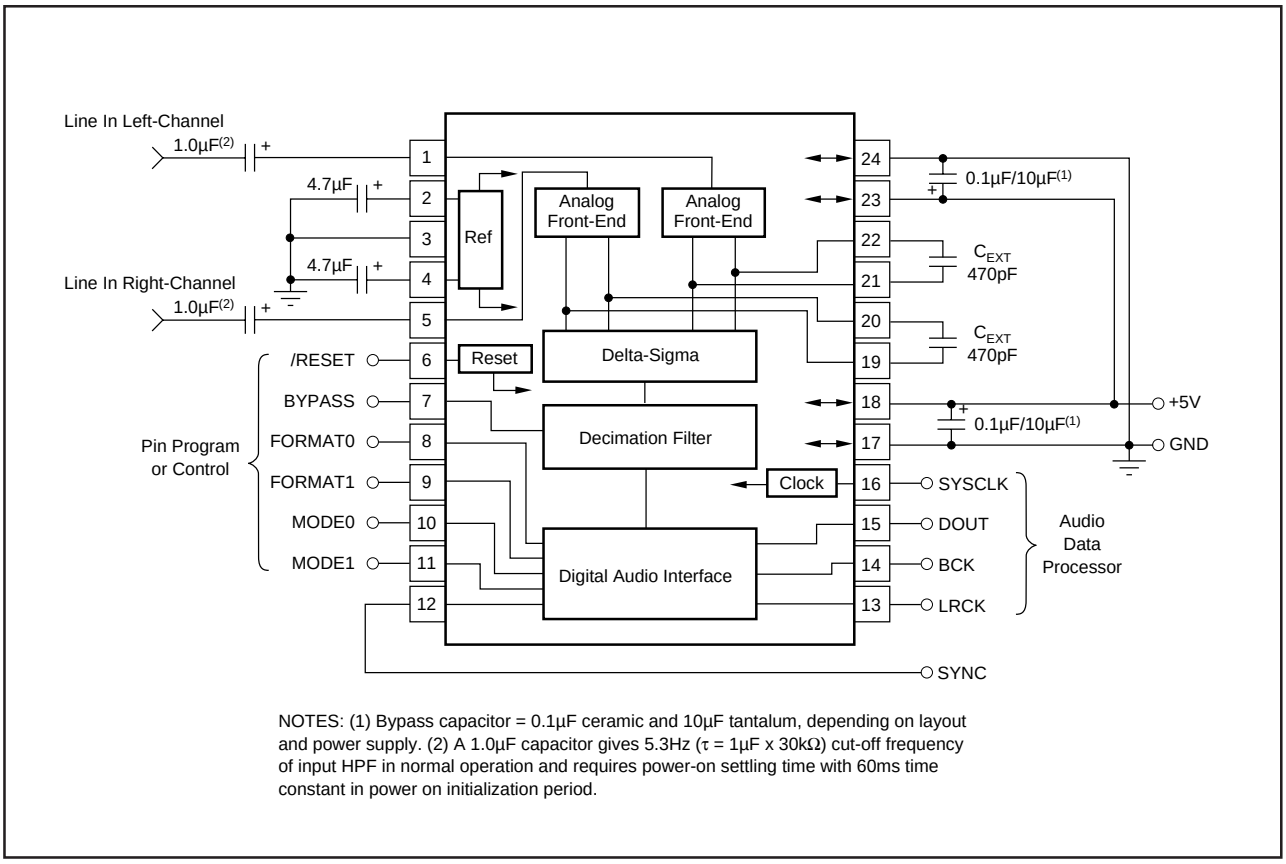
NOTES: (1) In the Master Mode, FSYNC, BCK, and LRCK are outputs similar to DOUT.
(2) The HPF transient response (exponentially attenuationed signal from ±0.2% DC of FSR with 200ms time constant) appears initially.

FIGURE 9. ADC Output for Power-On Reset and RSTB Control.



NOTES: (1) Applies only for Slave Mode—the loss of synchronization never occurs in Master Mode.
(2) The HPF transient response (exponentially attenuationed signal from ±0.2% DC of FSR with 200ms time constant) appears initially.

FIGURE 10. ADC Output When Synchronization is Lost and for Resynchronization.



NOTES: (1) Bypass capacitor = 0.1µF ceramic and 10µF tantalum, depending on layout and power supply. (2) A 1.0µF capacitor gives 5.3Hz (τ = 1µF x 30kΩ) cut-off frequency of input HPF in normal operation and requires power-on settling time with 60ms time constant in power on initialization period.

FIGURE 11. Typical Circuit Connection.

V_{IN} PINS

A 1.0µF tantalum capacitor is recommended as an AC-coupling capacitor which establishes a 5.3Hz cut-off frequency. If a higher full-scale input voltage is required, the input voltage range can be increased by adding a series resistor to the V_{IN} pins.

V_{REF} INPUTS

A 4.7µF tantalum capacitor is recommended between $V_{REF}1$, $V_{REF}2$, and REFCOM to ensure low source impedance for the ADC's references. These capacitors should be located as close as possible to the $V_{REF}1$ or $V_{REF}2$ pin to reduce dynamic errors on the ADC's references. The REFCOM pin should also be connected directly to AGND under the parts.

$C_{IN}P$ and $C_{IN}N$ INPUTS

A 470pF to 1000pF film capacitor is recommended between $C_{IN}PL$ and $C_{IN}NL$, $C_{IN}PR$ and $C_{IN}NR$ to create an anti-aliasing filter, which will have an 170kHz to 80kHz cut-off frequency. These capacitors should be located as close as possible to the $C_{IN}P$ and $C_{IN}N$ pins to avoid introducing unexpected noise or dynamic errors into the delta-sigma modulator.

DOUT, BCK, LRCK, FSYNC PINS

The DOUT, BCK, LRCK and FSYNC pins in Master Mode have a large load drive capability, but locating the buffer near the PCM1800 and minimizing the load capacitance is recommended in order to minimize the digital analog crosstalk and to maximize dynamic performance potential.

SYSTEM CLOCK

The quality of the system clock can influence dynamic performance in the PCM1800. The duty cycle, jitter, and threshold voltage at the system clock input pin must be carefully managed. When power is supplied to the part, the system clock, bit clock (BCK), and a word clock (LRCK) should also be supplied simultaneously. Failure to supply the audio clocks will result in a power dissipation increase of up to three times normal dissipation and may degrade long-term reliability if the maximum power dissipation limit is exceeded.

RSTB Control

If the capacitance between $V_{REF}1$ and $V_{REF}2$ exceeds 4.7µF, an external reset control delay time circuit must be used.