BURR-BROWN®

PCM1712U

SoundPLUS Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

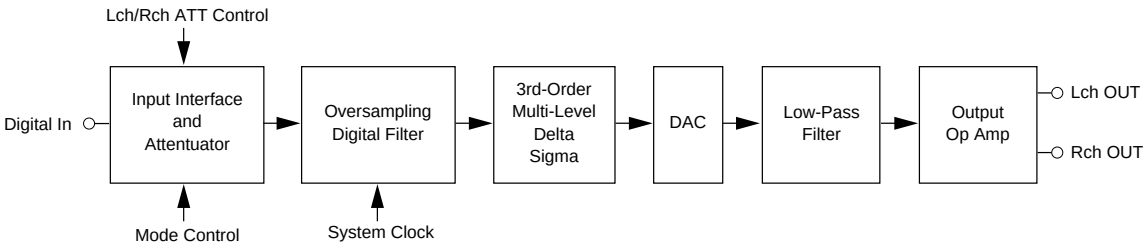
- 16-BIT RESOLUTION
- COMPLETE STEREO DAC:
  - 8X Oversampling Digital Filter
  - Multi-Level Delta-Sigma DAC
  - Analog Low Pass Filter
  - Output Amplifier
- HIGH PERFORMANCE:
  - –87dB THD + N
  - 94dB Dynamic Range
  - 98dB SNR
- SYSTEM CLOCK: 384fs
- SINGLE +5V POWER SUPPLY
- ON-CHIP DIGITAL FILTER:
  - Soft Mute and Attenuation
  - Digital De-emphasis
  - Double Speed Dubbing Mode
- SMALL 28-PIN SOIC PACKAGE

DESCRIPTION

The PCM1712 is a complete low cost stereo, audio digital-to-analog converter, including digital interpolation filter, 3rd-order delta-sigma DAC, and analog output amplifiers. PCM1712 accepts 16-bit normal input data (MSB first, right justified), or 16-bit IIS data (32-bits per word, continuous clock).

The digital filter performs an 8X interpolation function, as well as special functions such as soft mute, digital attenuation, de-emphasis and double-speed dubbing.

PCM1712 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Its low cost, small size and single +5V power supply make it ideal for automotive CD players, bookshelf CD players, BS tuners, keyboards, MPEG audio, MIDI applications, set-top boxes, CD-ROM drives, CD-Interactive and CD-Karaoke systems. PCM1712 has the same pinout functions as PCM1710.



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PDS-1245B
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SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 16-bit data, SYSCLK = 384fs, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1712U MIN	PCM1712U TYP	PCM1712U MAX	UNITS
RESOLUTION			16		Bits
DIGITAL INPUT/OUTPUT					
Logic Family					
Input Logic Level (pins 1 to 3)					
V_{IH}		2.0			VDC
V_{IL}				0.8	VDC
Input Logic Current (pins 1 to 3)					
I_I				–200	µA
Input Logic Level (pins 24 to 28)					
V_{IH}		3.5			VDC
V_{IL}				1.5	VDC
Input Logic Level (pins 24 to 28)					
I_I				–200	µA
Input Logic Level (XTI)					
V_{IH}		3.2			VDC
V_{IL}				1.4	VDC
Input Logic Current (XTI)					
I_I				–120	µA
Output Logic Level (CLKO):					
V_{OH}		4.5			VDC
V_{OL}				0.5	VDC
Output Logic Current					
I_O		±10			mA
Data Format		Normal/IIS (see Timing) SELECTABLE			
Data Bit		16-Bit/MSB First, Two's Complement			
Sampling Frequency		32	44.1	48	kHz
System Clock Frequency	384fs	12.288	16.934	18.432	MHz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mis-Match Channel-To-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_O = 1/2V_{CC} at Bipolar Zero		±20		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Gain Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE(1)					
THD+N at F/S (0dB)	f_{IN} = 991Hz	–82	–87		dB
THD+N at –60fdB	f_{IN} = 991kHz		–34		dB
Dynamic Range	EIAJ A-weighted		94		dB
S/N Ratio	EIAJ A-weighted	92	98		dB
Channel Separation	f_{IN} = 991Hz	90	96		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple	Normal Mode			±0.17	dB
Pass Band Ripple	Double Speed Mode			±0.22	dB
Stop Band Attenuation	Normal Mode	–35			dB
Stop Band Attenuation	Double Speed Mode	–34			dB
Pass Band	Normal Mode		0.4535		fs
Pass Band	Double Speed Mode		0.4535		fs
Stop Band	Normal Mode		0.5465		fs
Stop Band	Double Speed Mode		0.5465		fs
De-emphasis Error	(f_S 32kHz ~ 48kHz)	–0.2		+0.55	dB
ANALOG OUTPUT					
Voltage Range			3.1		Vp-p
Load Impedance		5k			Ω
Center Voltage			+1/2V_{CC}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.5	+5.0	+5.5	VDC
$+V_{DD}$		+4.5	+5.0	+5.5	VDC
Supply Current $+I_{CC}$ $+I_{DD}$	$+V_{CC}$ = $+V_{DD}$ = +5.0V		28	40	mA
Power Dissipation	$+V_{CC}$ = $+V_{DD}$ = +5.0V		140	200	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTE: (1) Tested with Shibasoku #725 THD. Meter 400Hz HPF, 30kHz LPF On, Average Mode with 20kHz bandwidth limiting.

PIN ASSIGNMENTS

PIN NAME	NUMBER	FUNCTION
Input Interface Pins		
LRCIN	1	Sample Rate Clock Input. Controls the update rate (fs).
DIN	2	Serial Data Input. MSB first, right justified format contains a frame of 16-bit or 20-bit data.
BCKIN	3	Bit Clock Input. Clocks in the data present on DIN input.
Mode Controls and Clock Signals		
CLKO	4	Buffered Output of Oscillator. Equivalent to fs.
XTI	5	Oscillator Input (External Clock Input). For an internal clock, tie XTI to one side of the crystal oscillator. For an external clock, tie XTI to the output of the chosen external clock.
XTO	6	Oscillator Output. When using the internal clock, tie to the opposite side (from pin 5) of the crystal oscillator. When using an external clock, leave XTO open.
MODE	24	Operation Mode Select. For serial mode, tie MODE “High”. For parallel mode, tie MODE “Low”.
MUTE	25	Mute Control. To disable soft mute, tie MUTE “High”. To enable soft mute, tie MUTE “Low”.
MD/DM1	26	Mode Control for Data/De-emphasis. See “Mode Control Functions” on page 10.
MC/DM2	27	Mode Control for BCKIN/De-emphasis. See “Mode Control Functions” on page 10.
ML/DSD	28	Mode Control for WDCK/Double speed dubbing. See “Mode Control Functions” on page 10.
Analog Functions		
$V_{OUT}R$	13	Right Channel Analog Output.
$V_{OUT}L$	16	Left Channel Analog Output.
Power Supply Connections		
DGND	7, 22	Digital Ground.
V_{DD}	8, 21	Digital Power Supply (+5V).
$V_{CC}2R$	9	Analog Power Supply (+5V), Right Channel DAC.
AGND2R	10	Analog Ground (DAC), Right Channel.
EXT1R	11	Output Amplifier Common, Right Channel. Bypass to ground with a 10µF capacitor.
EXT2R	12	Output Amplifier Bias, Right Channel. Connect to EXT1R.
AGND	14	Analog Ground.
V_{CC}	15	Analog Power Supply (+5V).
EXT2L	17	Output Amplifier Bias, Left Channel. Connect to EXT1L.
EXT1L	18	Output Amplifier Common, Left Channel. Bypass to ground with a 10µF capacitor.
AGND2L	19	Analog Ground (DAC), Left Channel.
$V_{CC}2L$	20	Analog Power Supply (+5V), Left Channel DAC.
NC	23	No Connection.

ABSOLUTE MAXIMUM RATINGS

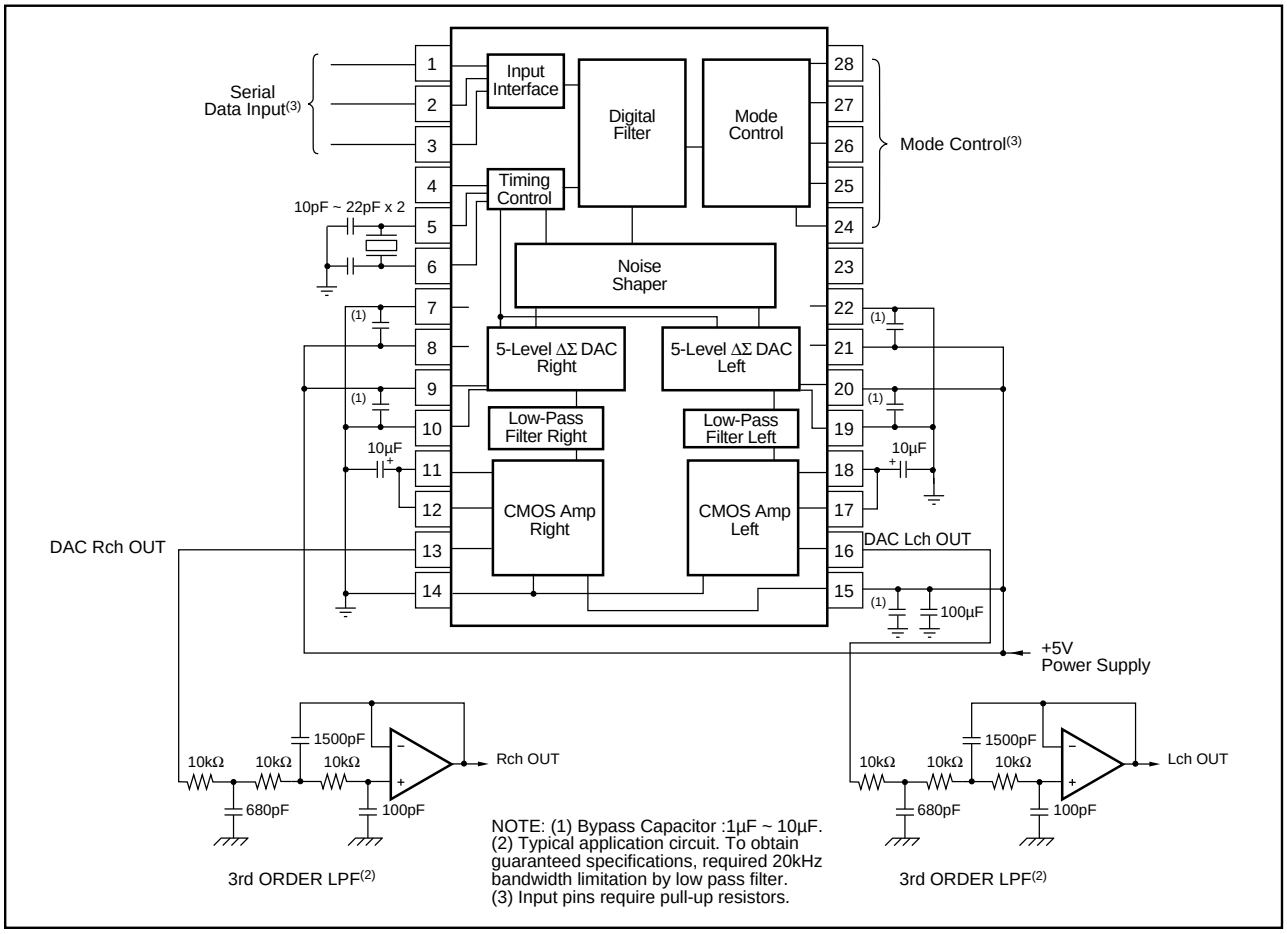
Power Supply Voltage	+6.5V
$+V_{CC}$ to V_{DD} Voltage	±0.1V
Input Logic Voltage	–0.3V~V_{DD}+0.3V
Power Dissipation	300mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature Range	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C

PACKAGE INFORMATION

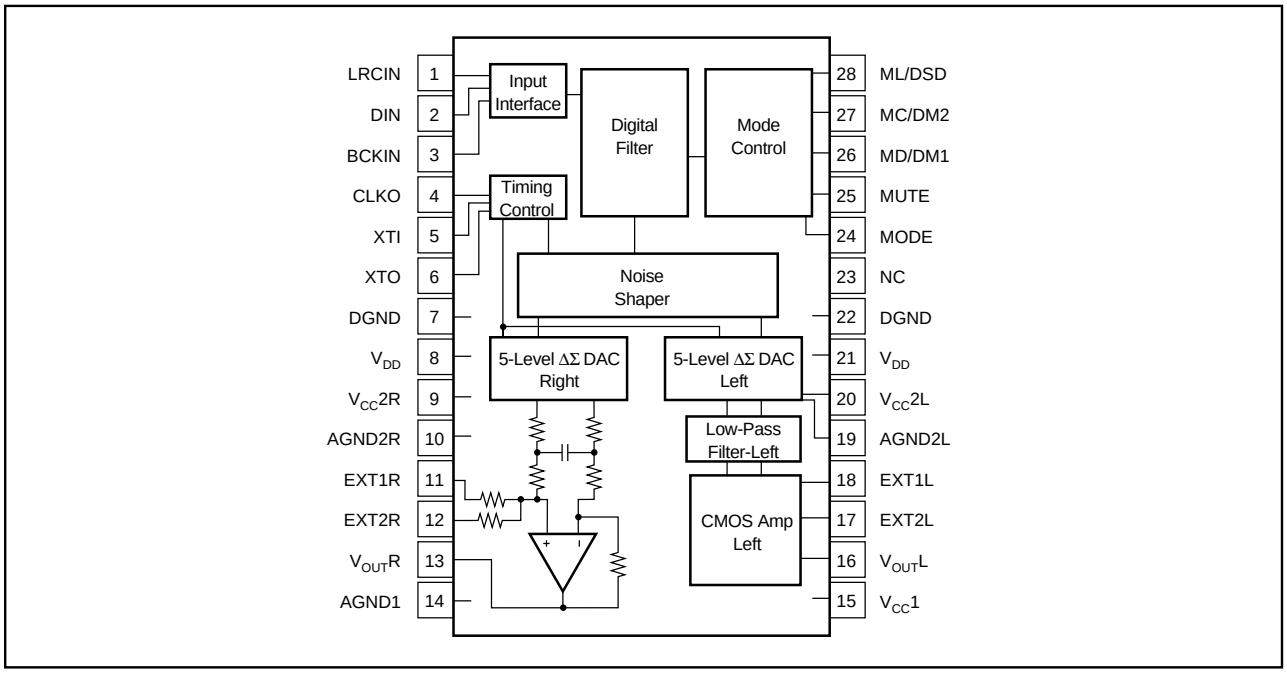
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1712U	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

CONNECTION DIAGRAM



PIN CONFIGURATION



DATA INPUT TIMING

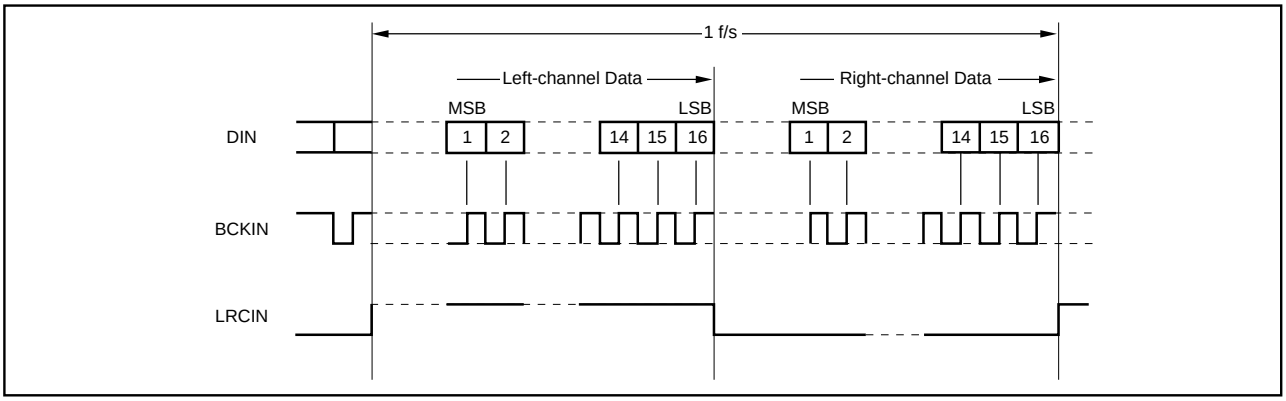


FIGURE 1. Normal Format, 16-Bit (LRCIN H: Lch).

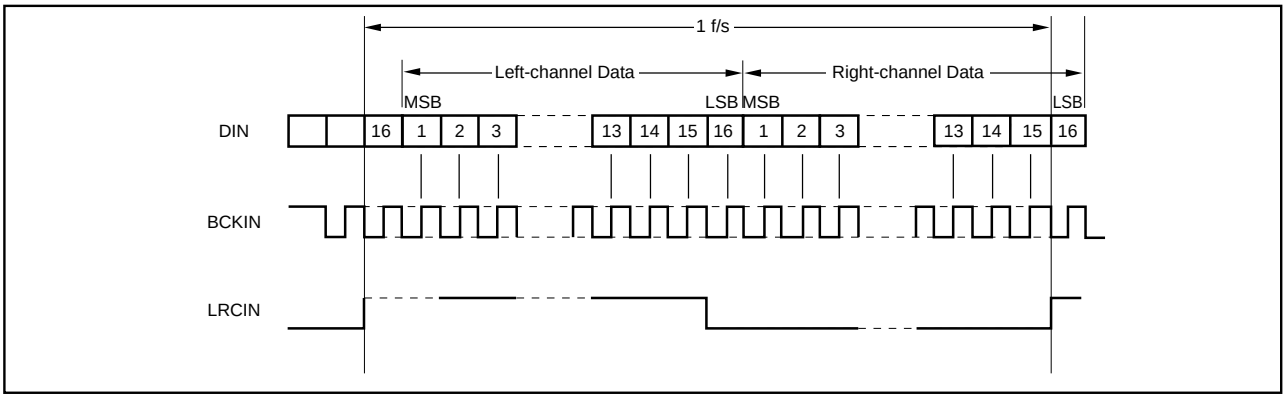


FIGURE 2 . IIS Format, 16-Bit (32 BCKIN/fs, continuous data).

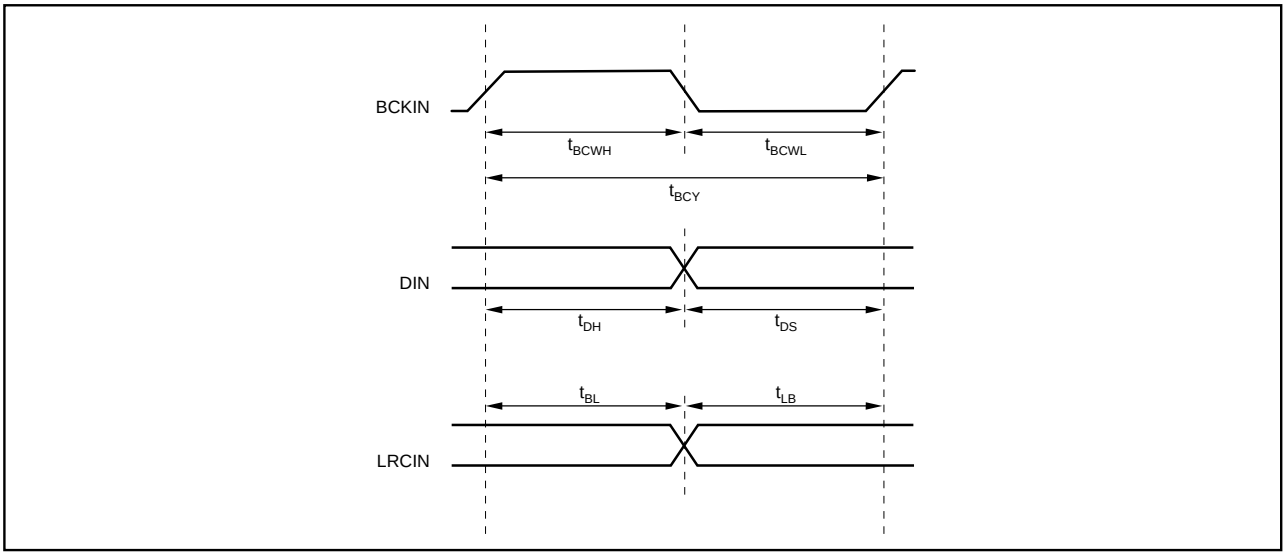


FIGURE 3. Data Input Timing.

BCK Pulsewidth (H Level)	t_{BCWH}	70ns (min)
BCK Pulsewidth (L Level	t_{BCWL}	70ns (min)
BCK Pulse Cycle Time	t_{BCY}	140ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)
BCK Rising Edge → LRCI Edge	t_{BL}	30ns (min)
LRC I Edge → BCK Rising Edge	t_{LB}	30ns (min)

TABLE I. Data Input Timing Specifications.

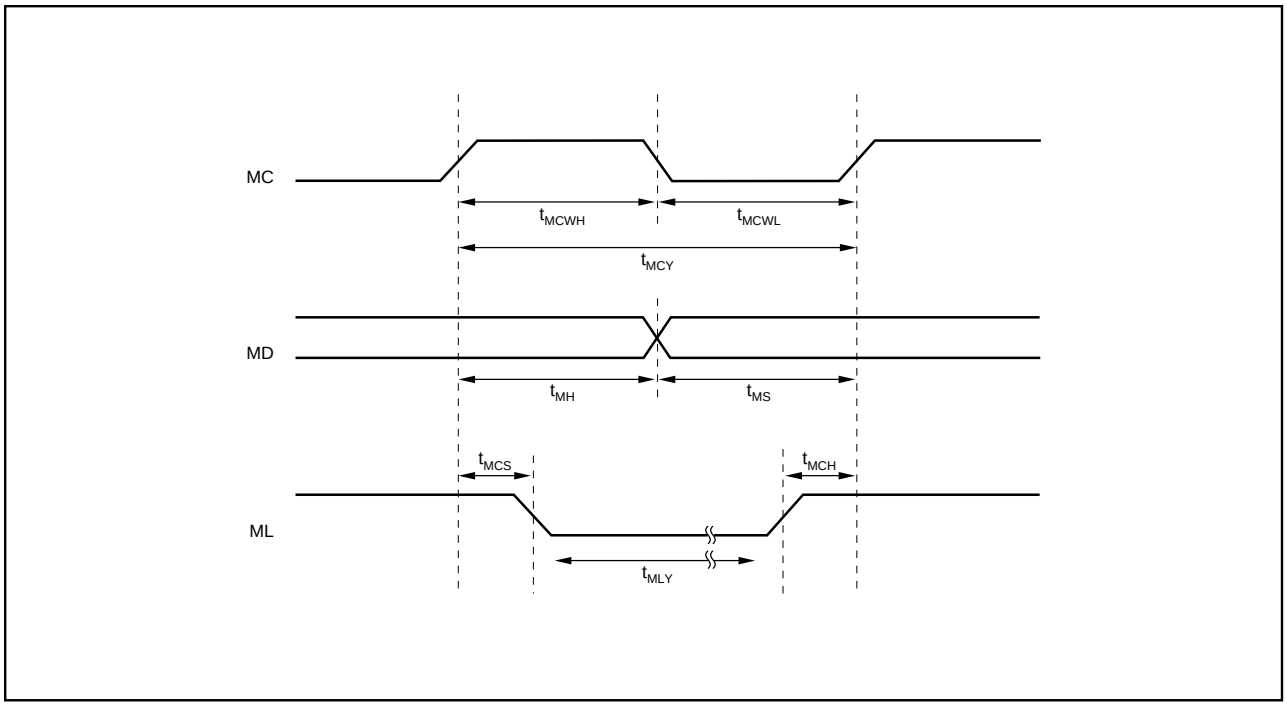


FIGURE 4. Serial Mode Control Timing.

MC Pulsewidth (H Level)	t_{MCWH}	50ns (min)
MC Pulsewidth (L Level)	t_{MCWL}	50ns (min)
MC Pulse Cycle Time	t_{MCY}	100ns (min)
MD Setup Time	t_{MS}	30ns (min)
MD Hold Time	t_{MH}	30ns (min)
ML Setup Time	t_{MCS}	30ns (min)
ML Hold Time	t_{MCH}	30ns (min)
ML Low-Level Time	t_{MLY}	1/sysclk + 20ns (min)

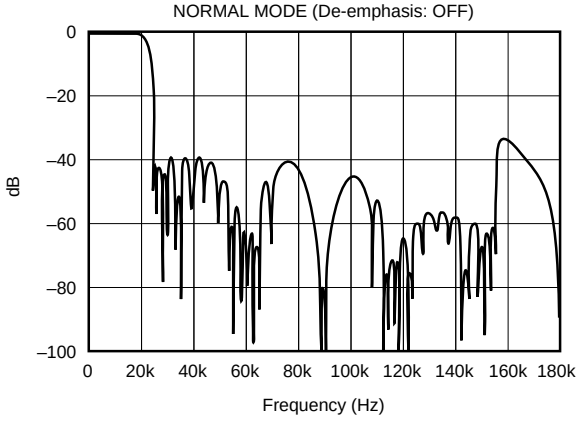
TABLE II. Serial Mode Control Timing Specifications (Refer to Figure 5).

TYPICAL PERFORMANCE CURVES

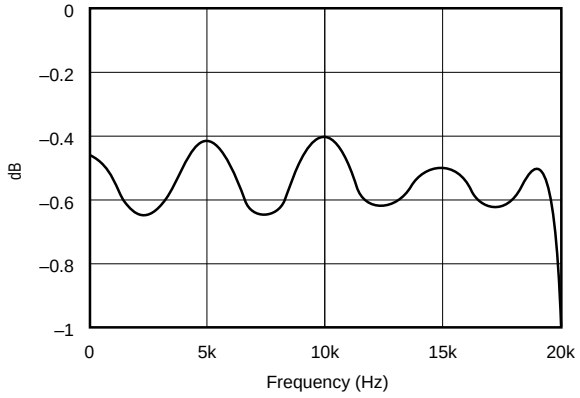
All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, f_{SYS} = 384fs, and 16-bit data, unless otherwise noted.

DIGITAL FILTER

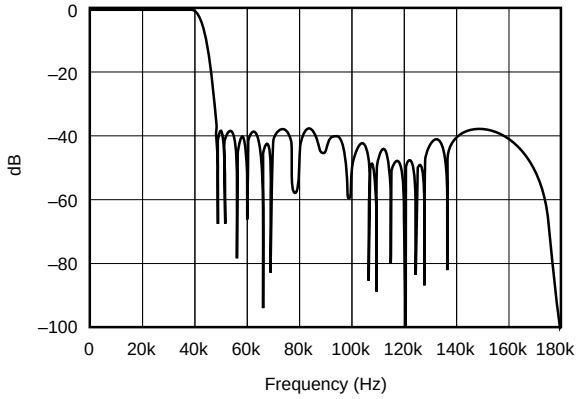
OVERALL FREQUENCY CHARACTERISTICS
NORMAL MODE (De-emphasis: OFF)



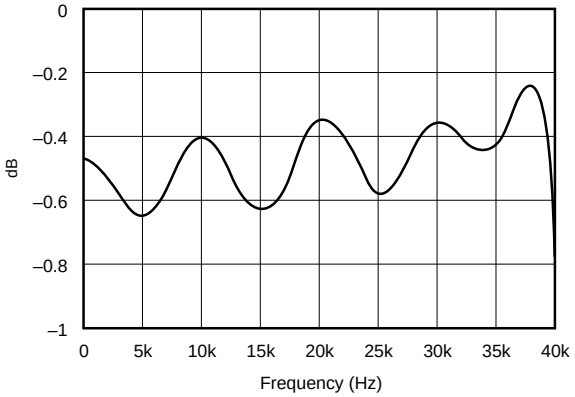
PASSBAND RIPPLE CHARACTERISTIC
NORMAL MODE (De-emphasis: OFF)



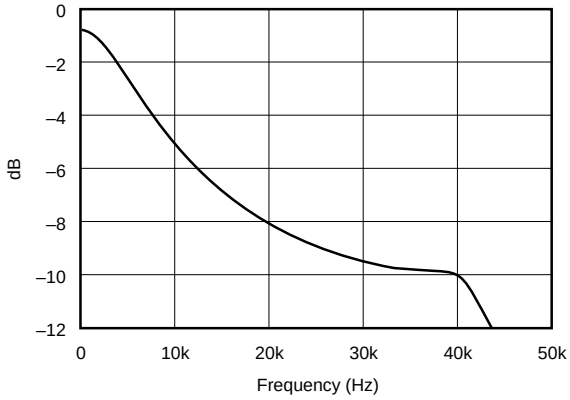
OVERALL FREQUENCY CHARACTERISTICS
DOUBLE-SPEED MODE (De-emphasis: OFF)



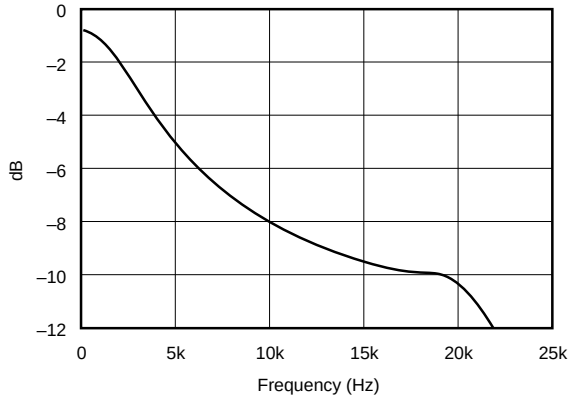
PASSBAND RIPPLE FREQUENCY CHARACTERISTIC
DOUBLE-SPEED MODE (De-emphasis: OFF)



DE-EMPHASIS CHARACTERISTIC
DOUBLE-SPEED MODE



DE-EMPHASIS CHARACTERISTIC
NORMAL MODE

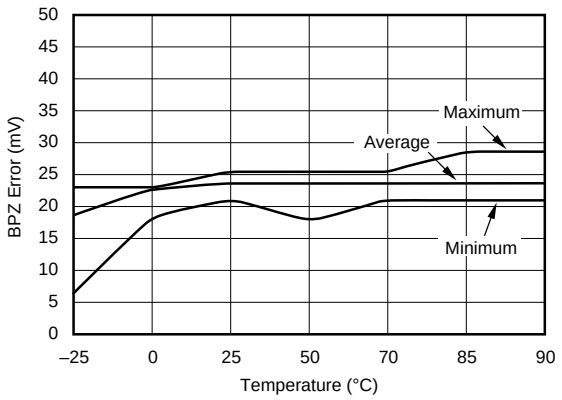


TYPICAL PERFORMANCE CURVES (CONT)

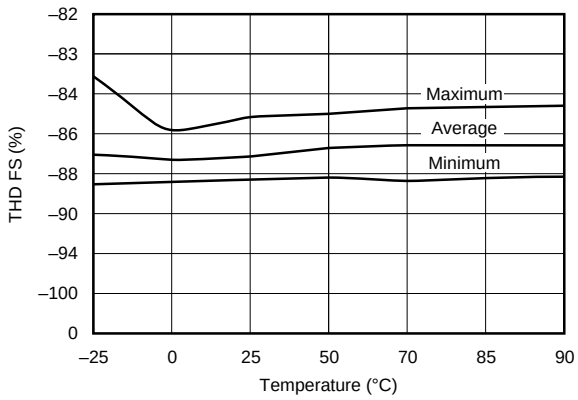
All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, f_{SYS} = 384fs, and 16-bit data, unless otherwise noted.

DYNAMIC PERFORMANCE (Based on 200 piece sample from 3 diffusion runs)

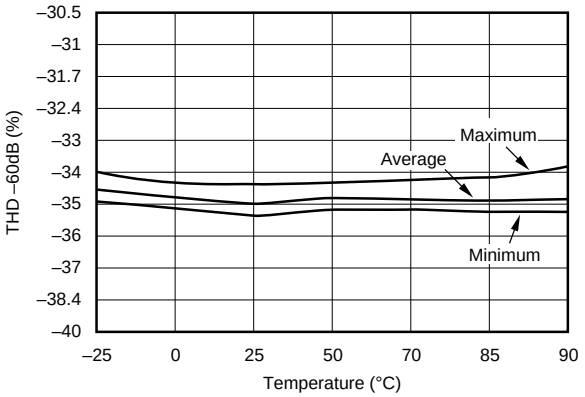
BPZ ERROR vs TEMPERATURE



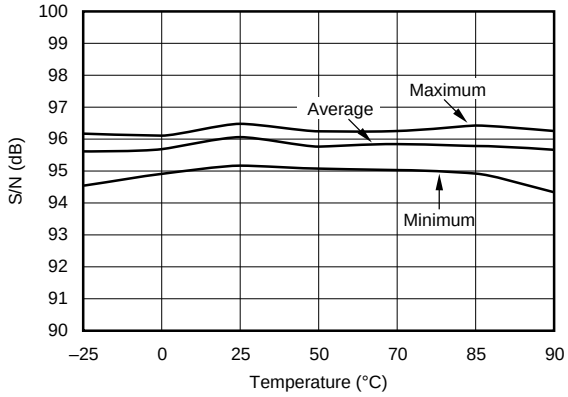
THD FS vs TEMPERATURE



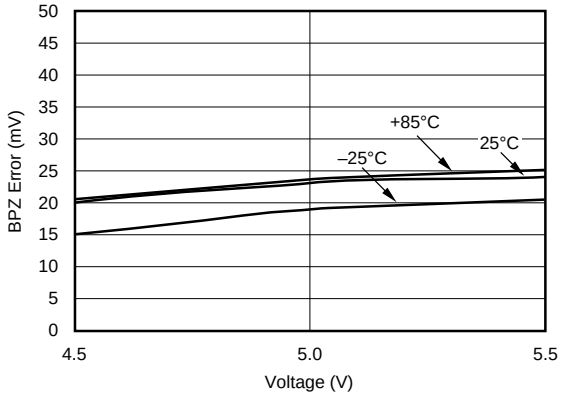
THD –60dB vs TEMPERATURE



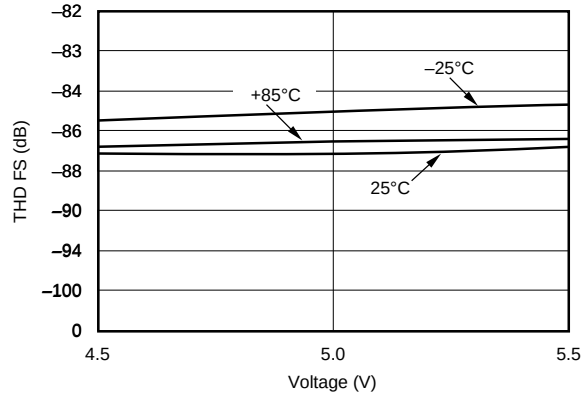
SNR vs TEMPERATURE



BPZ ERROR vs SUPPLY VOLTAGE



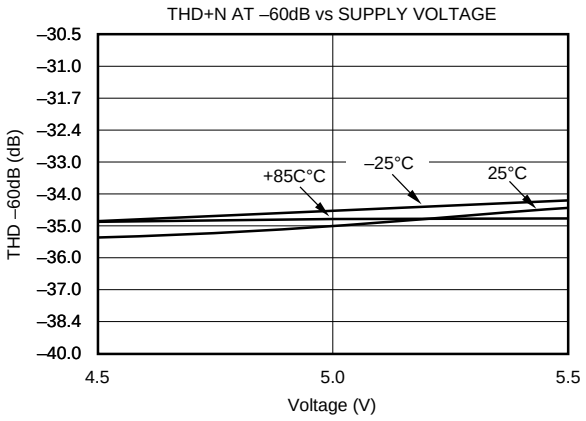
THD+N AT FS vs SUPPLY VOLTAGE

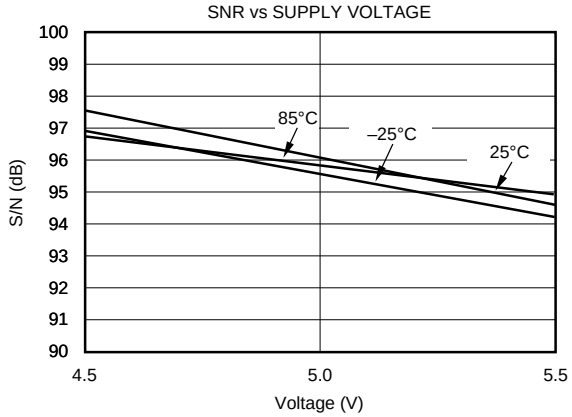


TYPICAL PERFORMANCE CURVES (CONT)

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, f_{SYS} = 384fs, and 16-bit data, unless otherwise noted.

DYNAMIC PERFORMANCE (Based on 200 piece sample from 3 diffusion runs)





CAUTION: Minimum and maximum values on typical performance curves are not meant to imply a guarantee. Curves should be used for reference only. Refer to specifications for guaranteed performance.

FUNCTIONAL DESCRIPTION

PCM1712 has several built-in functions including digital attenuation, digital de-emphasis and soft mute. These functions are software controlled. PCM1712 can be operated in two different modes, **Serial** or **Parallel**. Serial Mode is a three-wire interface using pin 26 (MD), pin 27 (MC), and pin 28 (ML). Data on these pins are used to control de-emphasis modes, mute, double-speed dubbing, input resolution and input formats. PCM1712 can also be operated in parallel mode, where static control signals are used on pins 26 (DM1), pin 27 (DM2), and pin 28 (DSD). Operation of both of these modes are covered in detail in the next sections.

CAUTION: Mode control signals operate on level triggered logic. The minimum timing conditions detailed in Figures 4 and 5 MUST be observed.

MODE CONTROL: SERIAL/PARALLEL SELECTION

MODE = H	Serial Mode
MODE = L	Parallel Mode

TABLE III. Serial and Parallel Mode are Selectable by MODE Pin (Pin 24).

MODE CONTROL: SELECTABLE FUNCTIONS

FUNCTION	SERIAL MODE (MODE = H)	PARALLEL MODE (MODE = L)
Input Data Format Selection	0	X (Normal Mode Fixed)
Input LRCI Polarity Selection	0	X
De-emphasis Control	0	0
Mute	0	0
Attenuation	0	X
Double-Speed Dubbing	0	0
NOTE: 0: Selectable, X: Not Selectable.		

TABLE IV. Selectable Functions in Serial Mode and Parallel Mode.

Table IV indicates which functions are selectable within the user's chosen mode. All of the functions shown are selectable within the serial mode, but only de-emphasis control, mute and double-speed dubbing may be selected when using PCM1712 in the parallel mode.

PARALLEL-MODE: DE-EMPHASIS CONTROL (PIN 24 [MODE] = L)

DM1 (Pin 26)	DM2 (Pin 27)	De-emphasis
L	L	OFF
H	L	32kHz
L	H	48kHz
H	H	44.1kHz

TABLE V. De-emphasis (Pins 26 and 27).

In the parallel mode, de-emphasis conditions are controlled by the logic levels on pin 26 (DM1) and pin 27 (DM2). For PCM1712, de-emphasis can operate at 32kHz, 44.1kHz, 48kHz, or disabled.

PARALLEL-MODE: DOUBLE-SPEED DUBBING CONTROL (PIN 24 [MODE] = L)

DSD = H	Normal Mode
DSD = L	Double Speed Dubbing Mode

TABLE VI. DSD (Pin 28).

In the parallel mode, double-speed dubbing can be enabled by holding pin 28 (DSD) at logic "low".

SERIAL MODE CONTROL

In order to use all of PCM1712's functionality, the **serial mode control** should be used. PCM1712 must be addressed three separate times to set all of the various registers and flags that control these functions.

Table VII together with Figure 6 details the control of the PCM1712 in the serial mode. Internal latches are used to hold this serial data until the PCM1712 is enabled to use the data. The serial mode is used by applying clocked data to the following pins:

NAME	PIN	FUNCTION
MC	27	Clock for Strobing in Data
ML	28	Latches Data into the Registers
MD	26	8-bit Data Word Defining Operation

DIGITAL ATTENUATION

One of the functions which can be implemented through use of the serial mode control is attenuation. This function allows the user to control the level of the output, independent of the input level set by the actual input data supplied to the DAC.

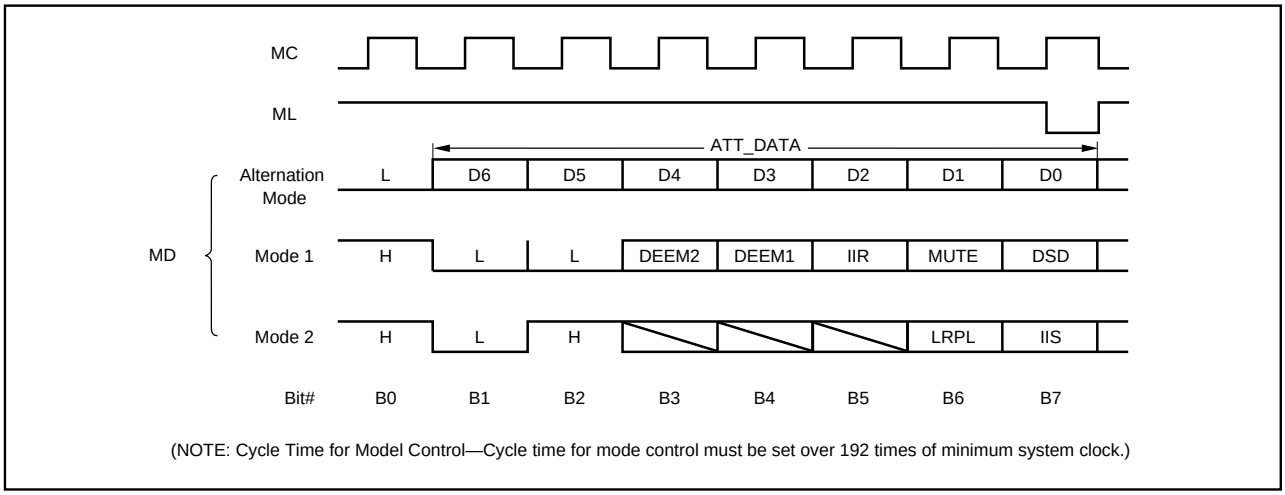
Referring to Figure 5, when the first data bit (B0) on MD (pin 26) is low, the attenuation function is enabled. The next seven bits (B1 - B6) define a binary value, ATT_DATA, that indicates the desired level of attenuation. The attenuation level is given by:

$$\text{Level} = 20\log_{10}(1 - \text{ATT\_DATA}/127)\ \text{dB}$$

When all 7 bits of the ATT_DATA word are high (ATT_DATA = 127), attenuation is infinite and the output of PCM1712 will be zero.

	B0	B1	B2	BIT NO.	MODE FLAG	FUNCTION MODE SELECTION			MODE BY DEFAULT
						MODE	BIT VALUE	SELECTED FUNCTION	
Mode 1	1	0	0	B3	DEEM2	Sampling Frequency for De-emphasis		DEEM2: 0 / 1; DEEM1: 0 → 48kHz; 1 → 32kHz / 44.1kHz	44.1kHz
				B4	DEEM1				
				B5	IIR	De-emphasis	0	De-emphasis OFF	OFF
							1	De-emphasis ON	
				B6	MUTE	Mute	0	Mute OFF	OFF
							1	Mute ON	
				B7	DSD	Double-Speed	0	Double-speed OFF	OFF
							1	Double-speed ON	
Mode 2	1	0	1	B3		Not Assigned			
				B4		Not Assigned			
				B5		Not Assigned			
				B6	LRPL	Polarity for LRCI	0	Lch:high/Rch:low	Lch:HIGH Rch:LOW
							1	Lch:low/Rch:high	
				B7	IIS	Input Format	0	Normal	Normal
							1	IIS	

TABLE VII. Serial-Mode Control Input Format (MODE: H, Pin 24).



(NOTE: Cycle Time for Model Control—Cycle time for mode control must be set over 192 times of minimum system clock.)

FIGURE 5. Mode Control Input Format, Serial Mode.

MODE 1 CONTROLS

This mode can be enabled with the sequence of 1, 0, 0 as the first three bits on MD (pin 26). This mode allows for the following functions:

De-emphasis	On/Off
De-emphasis Frequency	32kHz, 44.1kHz, 48kHz
Soft Mute	On/Off
Double-Speed Dubbing	On/Off

DIGITAL DE-EMPHASIS

PCM1712 allows three different sampling rates for digital de-emphasis. B3 and B4 are used for binary control of the de-emphasis frequency:

B3	B4	FREQUENCY
0	0	OFF
0	1	48kHz
1	0	32kHz
1	1	44.1kHz

Once the reset has been established on pin 27 (MC), the de-emphasis frequency defaults to 44.1kHz. B5 can be used to override B3 and B4; a logic low on B5 disables de-emphasis, and a logic high on B5 forces de-emphasis at 44.1kHz.

SOFT MUTE

Soft mute is enabled when B6 is high. The soft mute occurs gradually, unlike the forced infinite zero detection. When the mute data bit is high, complete muting will occur in 127/fs seconds.

DOUBLE-SPEED DUBBING

Double-speed dubbing is enabled when B7 is high. Since f_S is set at 44.1kHz, the system clock in double-speed mode is at 192fs.

MODE 2 CONTROLS

This mode is enabled when the first three bits on MD are 1, 0, 1. Mode 2 allows for the following functions:

LR Polarity	Controls Left/Right Channel Select
Input Format	Normal/IIS (Philips format)

SAMPLE RATE CLOCK POLARITY

B6 controls the polarity of the sample rate clock (LRCIN) polarity. When B6 is low, data will be accepted on the left channel when LRCIN is high, and on the right channel when LRCIN is low. When B6 is high, data will be accepted on the right channel when LRCIN is high, and on the left channel when LRCIN is low.

INPUT FORMAT

Normal input mode for PCM1712 is MSB first, right justified. PCM1712 may also be operated with IIS input format. When B7 is low, the input format is “normal”. When B7 is high, the input format is “IIS”.

DEFAULT MODE

At initial power-on, default settings for PCM1712 are 44.1kHz f_S, de-emphasis off, mute off, double speed off, infinite zero detect on, 16-bit input LRCIN left channel high, and normal input mode.

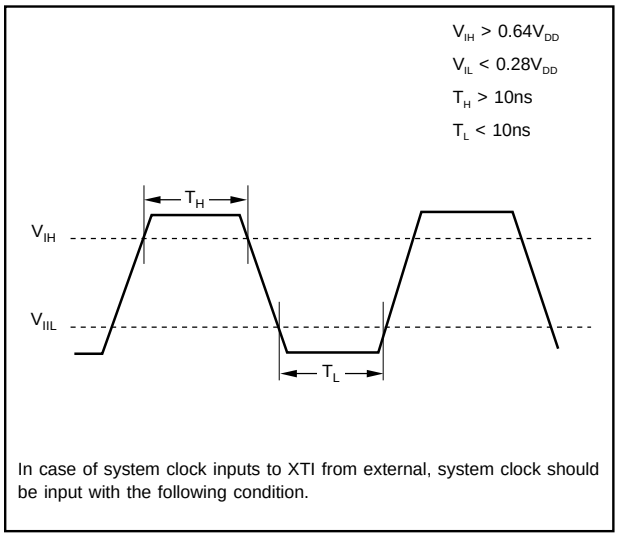


FIGURE 6. Timing Requirement for External System Clock (XTi).

SYSTEM CLOCK

SAMPLING FREQUENCY	SYSTEM CLOCK	FREQUENCY
32kHz	384fs	12.2880MHz
44.1kHz	384fs	16.9344MHz
48kHz	384fs	18.4320MHz

NORMAL/DOUBLE-SPEED DUBBING

For most CD playback applications operating at 384fs, the system clock frequency must be 16.9344MHz, in both the normal mode and double-speed dubbing mode. Table VIII illustrates the relationship between fs and output clock frequency in both modes.

PARAMETER	DSD	
	H (Normal)	L (Double Speed)
XTI Input Clock Frequency	384fs	192fs
XTI Frequency	16.9344MHz (f_S = 44.1kHz)	16.9344MHz (f_S = 88.2kHz)
CLKO Output Clock Frequency	384fs	192fs

TABLE VIII. Relationship Between Normal/Double Speed and fs.

EXTERNAL SYSTEM CLOCK

Figure 7 is a diagram showing the internal clock in conjunction with an external crystal oscillator.

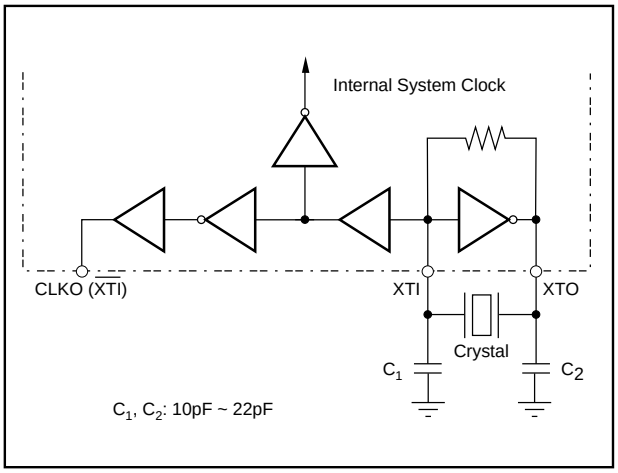


FIGURE 7. External Crystal Oscillator.

Figure 8 is a diagram showing the internal clock with an external clock source, instead of an oscillator. An external system clock (input to XTI) must meet timing requirement which is shown in Figure 6.

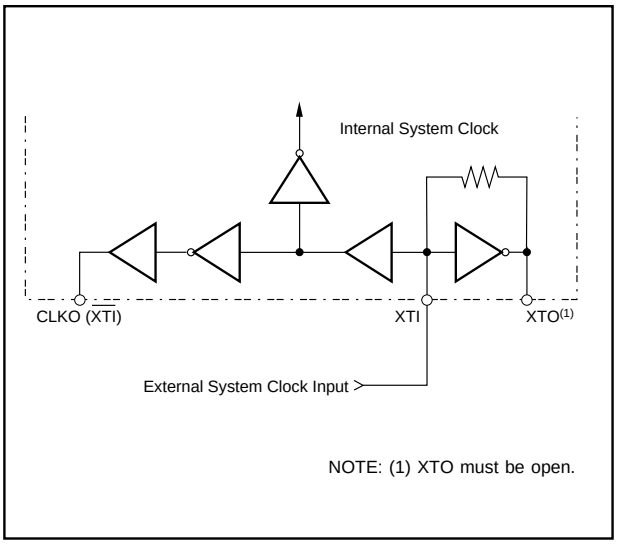


FIGURE 8. Latch-up Prevention Circuit.

POWER SUPPLY CONNECTIONS

PCM1712 has two power supply connections: digital (V_{DD}) and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.6V.

An application circuit to avoid a latch-up condition is shown in Figure 9.

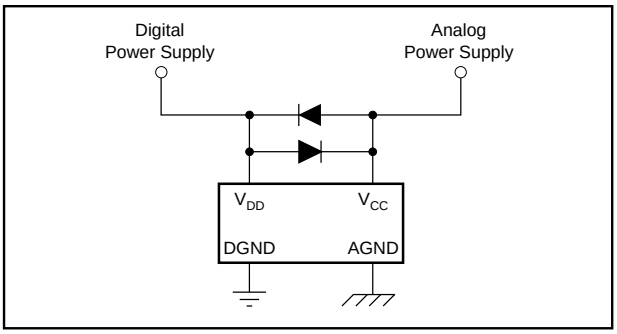


FIGURE 9. Latch-up Prevention Circuit.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 16 for optimal values of bypass capacitors. For applications which require very high performance at low levels (such as keyboards, synthesizers, etc.), it may be beneficial to provide additional bypassing on pin 15 (V_{CC1}) with a low ESR 100µF capacitor. This will eliminate stray tones which may be above the noise floor.

THEORY OF OPERATION

The delta-sigma section of PCM1712 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled 16-bit input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 10. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

Multi Level Delta Sigma

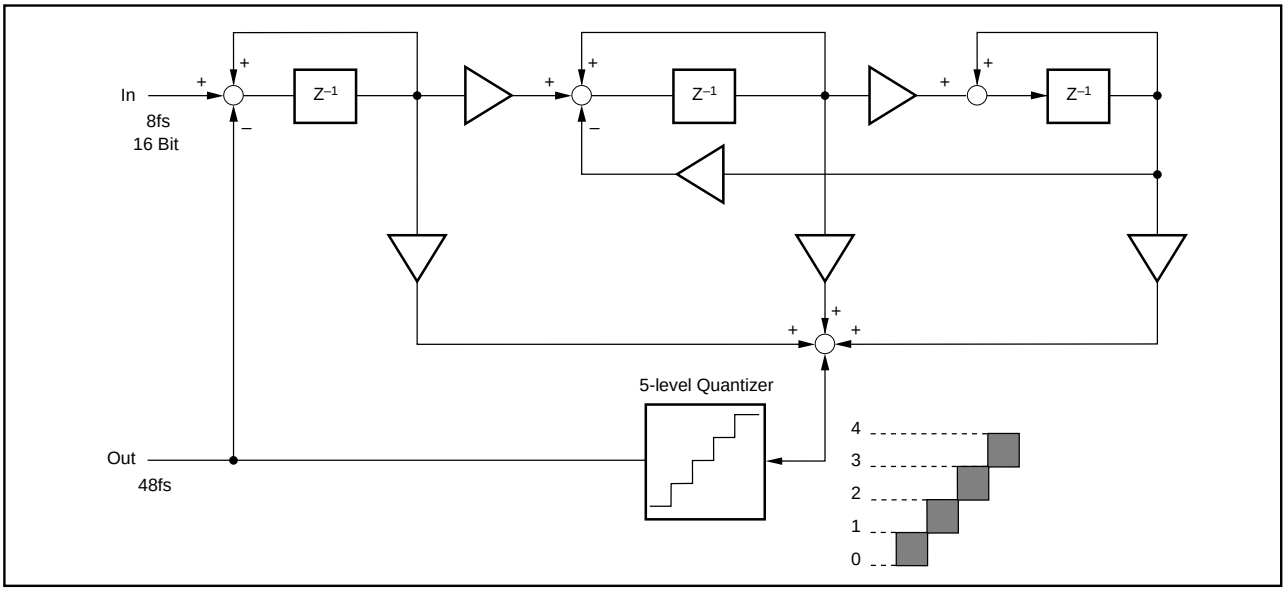


FIGURE 10. 5 Level ΔΣ Modulator Block Diagram.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is 48fs. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 11.

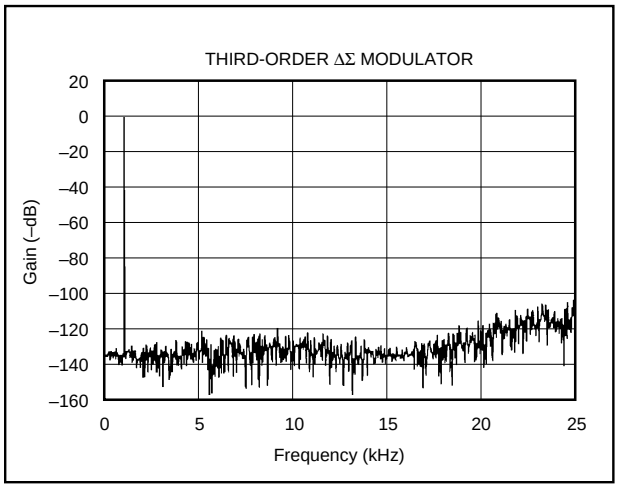


FIGURE 11. Quantization Noise Spectrum.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1712:

$$T_D = 12.625 \times 1/fs$$

For f_S = 44.1kHz, T_D = 12.625/44.1kHz = 286.28µs

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

INTERNAL RESET

When power is first applied to PCM1712, an automatic reset function occurs after 64 cycles of LRCIN.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1712 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD + N, etc. to 20kHz. Failure to use such a filter will result in higher THD + N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 12. The higher frequency rolloff of the filter is shown in Figure 13. If the user's application has the PCM1712 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 14. For some applications, a passive RC filter or 2nd-order filter may be adequate.

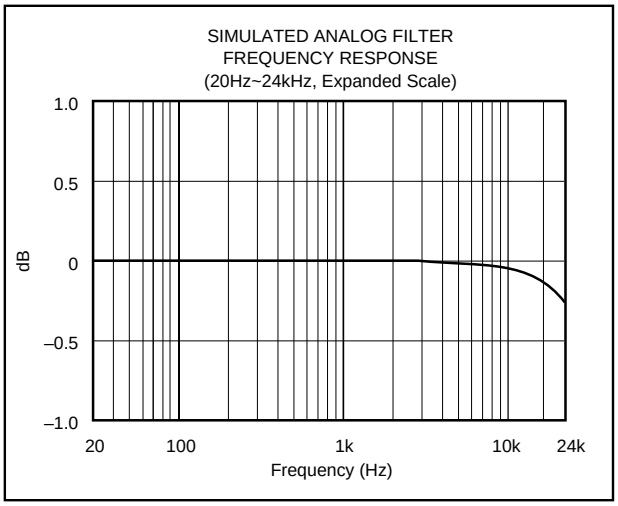


FIGURE 12. Low Pass Filter Frequency Response.

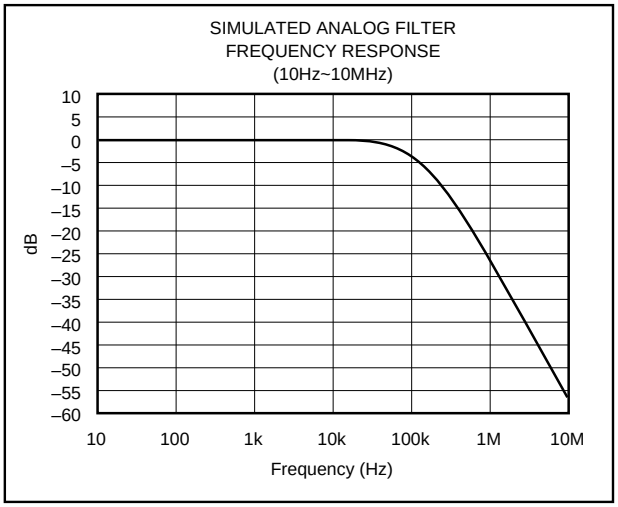


FIGURE 13. Low Pass Filter Frequency Response.

TEST CONDITIONS

Figure 15 illustrates the actual test conditions applied to PCM1712 in production. The 11th-order filter is necessary in the production environment for the removal of noise resulting from the relatively long physical distance between the unit and the test analyzer. In most actual applications, the third-order filter shown in Figure 14 is adequate. Under normal conditions, THD+N typical performance is –70dB with a 30kHz low pass filter (shown here on the THD meter), improving to –92dB when the external 20kHz second-order filter is used.

EVALUATION FIXTURES

An evaluation fixture is available for PCM1712.

DEM-PCM1712

This evaluation fixture is primarily intended for quick evaluation of the PCM1712's performance. DEM-PCM1712 can accept either an external clock or a user-installed crystal oscillator. All of the functions can be controlled by on-board switches. DEM-PCM1712 does not contain a receiver chip or an external low pass filter. DEM-PCM1712 requires a single +5V power supply.

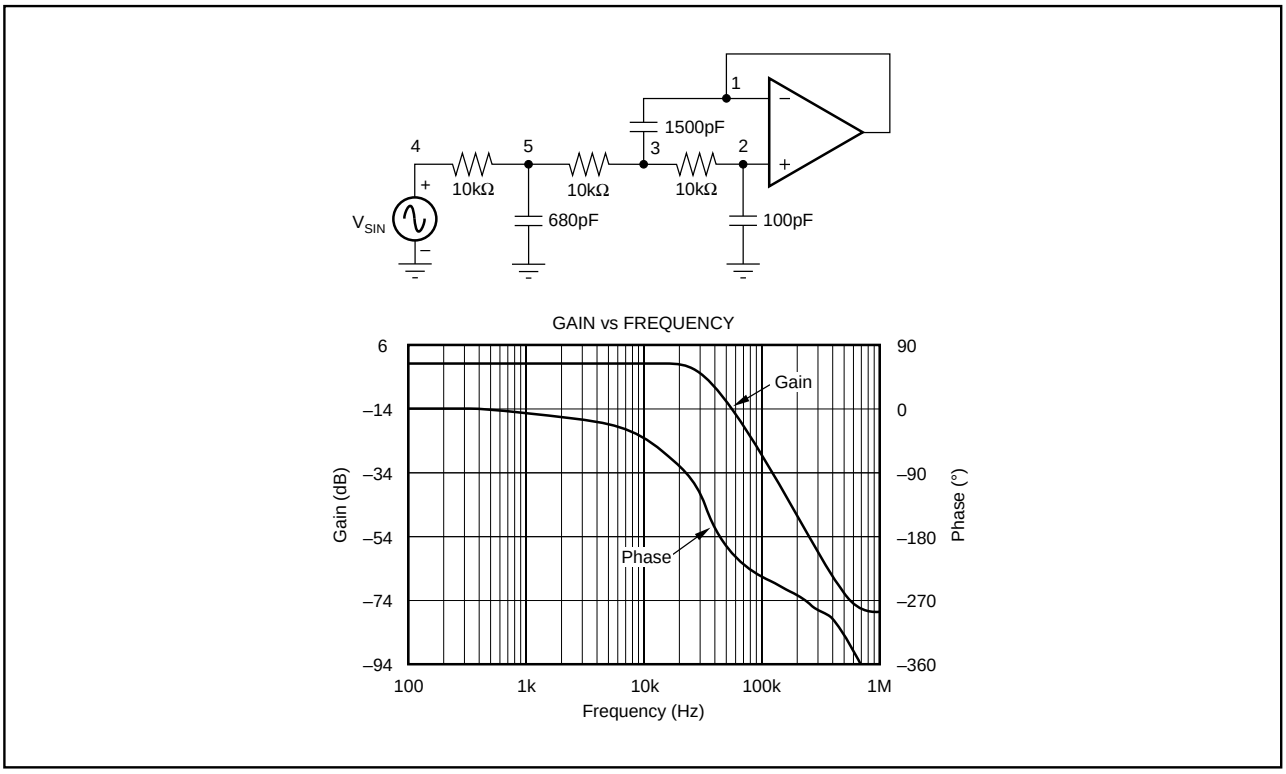


FIGURE 14. 3rd-Order LPF.

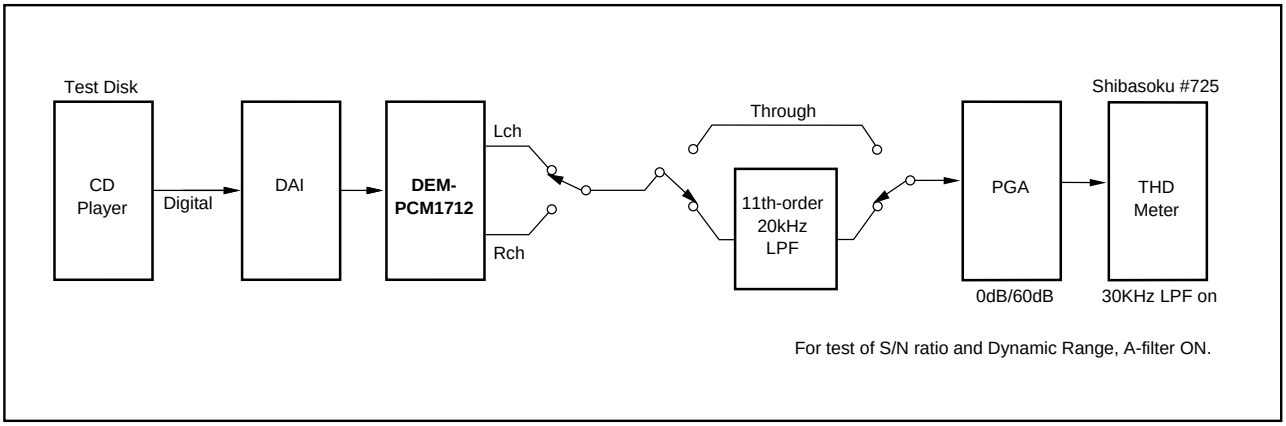


FIGURE 15. Test Block Diagram.

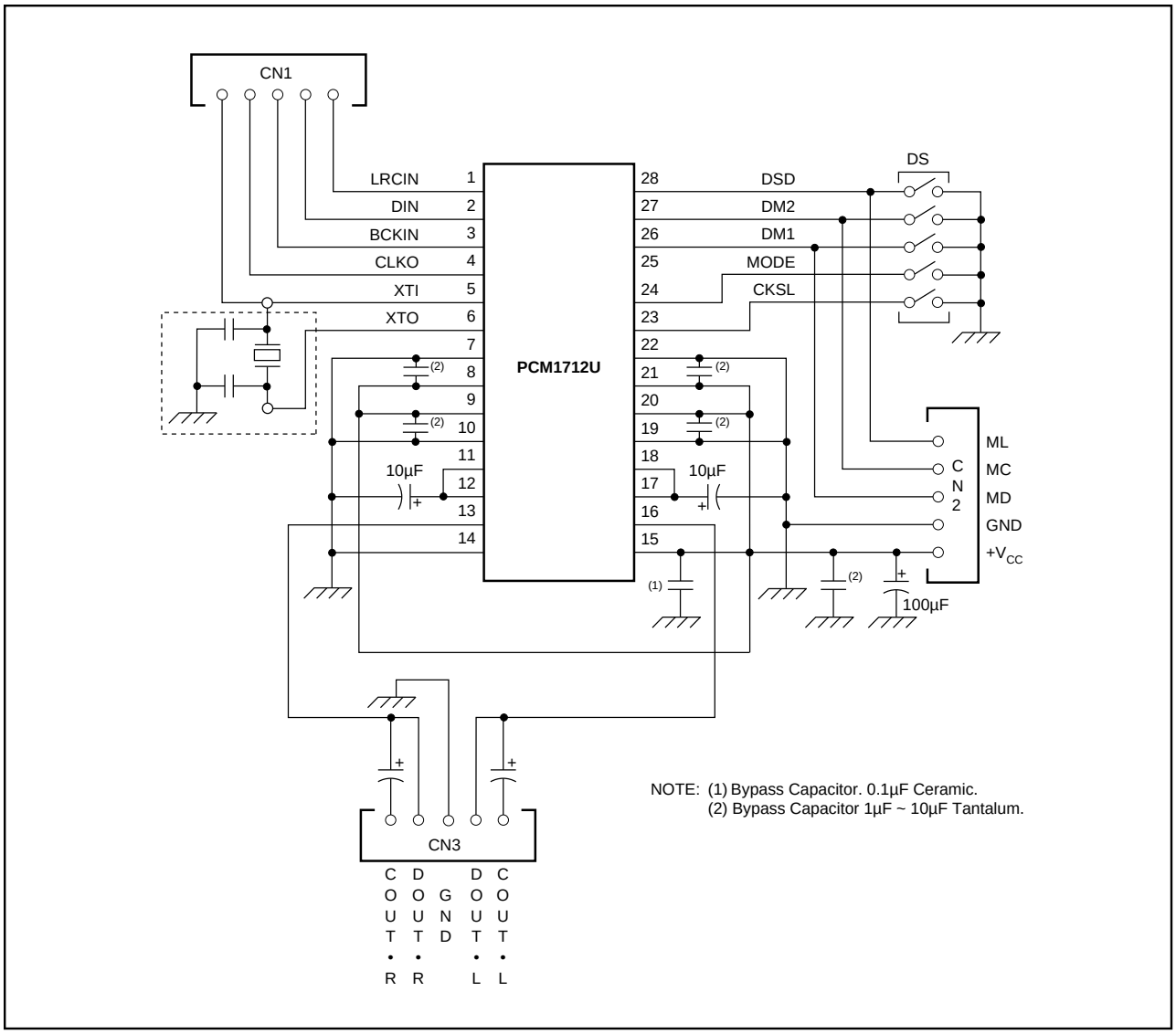


FIGURE 16. DEM-PCM1712 Schematic Circuit Diagram.