DATA SHEET

TDA8051
QPSK receiver

Product specification
Supersedes data of 1998 Jan 08
File under Integrated Circuits, IC02

1999 Aug 20

Philips Semiconductors

QPSK receiver TDA8051

FEATURES

- High operating input sensitivity
- Gain controlled amplifier
- PLL controlled carrier frequency
- Low crosstalk between I and Q channel outputs
- 3-wire transmission bus
- 5 V supply voltage.

APPLICATIONS

- BPSK/QPSK demodulation.

GENERAL DESCRIPTION

This TDA8051 is a monolithic bipolar IC intended for Quadrature Phase Shift Key (QPSK) demodulation. It includes:

- Low noise RF and gain controlled amplifier
- Two matched mixers
- Symmetrical Voltage Controlled Oscillator (VCO) with 0 to 90° signal generator whose frequency is controlled by an integrated Phase Lock Loop (PLL) circuit.
- Two matched amplifiers for output base-band active filtering and output buffers

The gain control is produced by output level detection compared with an external pre-fixed reference. The PLL consists of:

- Divide by four preamplifier
- 12-bit programmable main divider
- Crystal oscillator with 8-bit programmable reference divider
- Phase/frequency detector combined with charge pump to drive tuning amplifier
- 30 V output

QUICK REFERENCE DATA

All AC units are RMS values unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range	4.75	5.00	5.25	V
$f_{I(LNA)}$	input carrier frequency at LNA input	44	–	130	MHz
$V_{I(LNA)}$	input level at LNA input	–30	–	0	dBmV
$\Delta\Phi_{I-Q}$	phase error between I and Q channels	–	±3	–	deg
ΔG_{I-Q}	gain error between I and Q channels	–	±1	–	dB
$\alpha_{CT(I-Q)}$	crosstalk between I and Q channels	–	–30	–	dBc
IM3	3rd-order intermodulation distortion in I and Q channels (0 dBmV at LNA_IN)	–	–	–45	dBc
V_o	voltage output on pin I_OUT and Q_OUT	–	48	–	dBmV
f_{step}	step at output	50	–	250	kHz
f_{xtal}	crystal frequency	1	–	4	MHz
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8751T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

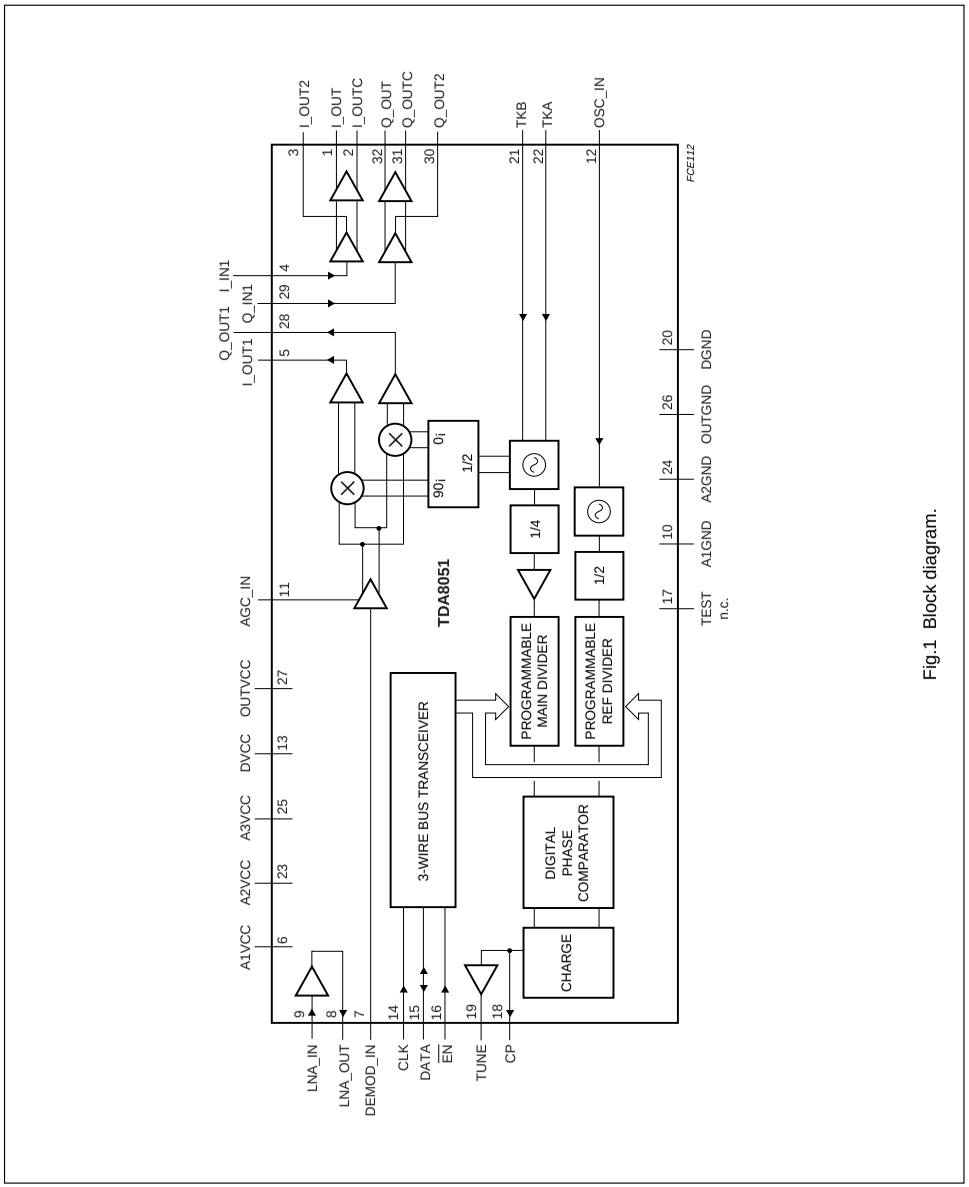


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
I_OUT	1	I data buffered balanced output
I_OUTC	2	I data buffered balanced output
I_OUT2	3	I data filtered output
I_IN1	4	input to active filter amplifier for I data
I_OUT1	5	I data raw output
A1VCC	6	analog supply voltage 1
DEMOD_IN	7	demodulator RF input
LNA_OUT	8	low noise amplifier RF output
LNA_IN	9	low noise amplifier RF input
A1GND	10	analog ground 1
AGC_IN	11	AGC control voltage input
OSC_IN	12	oscillator input
DVCC	13	digital supply voltage
CLK	14	3-wire bus serial control clock
DATA	15	3-wire bus serial control data
$\overline{EN}$	16	3-wire bus serial control enable (active LOW)
TEST	17	not connected
CP	18	charge pump output for PLL loop filter
TUNE	19	tuning voltage output
DGND	20	digital ground
TKB	21	VCO tank circuit input
TKA	22	VCO tank circuit input
A2VCC	23	analog supply voltage 2
A2GND	24	analog ground 2
A3VCC	25	analog supply voltage 3
OUTGND	26	output amplifiers ground
OUTVCC	27	output amplifiers supply voltage
Q_OUT1	28	Q data raw output
Q_IN1	29	input to active filter amplifier for Q data
Q_OUT2	30	Q data filtered output
Q_OUTC	31	Q data buffered balanced output
Q_OUT	32	Q data buffered balanced output

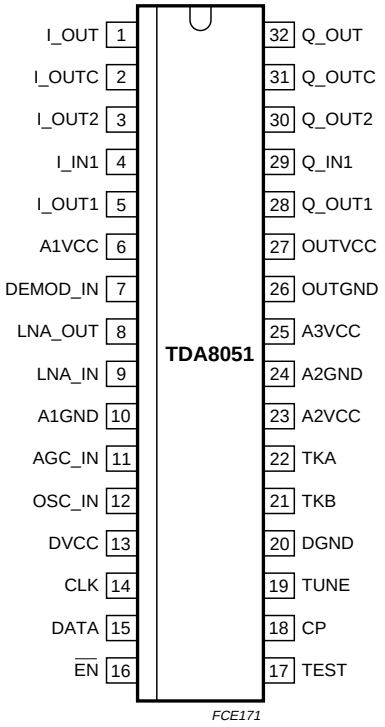


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The QPSK modulated signal is applied to the input as an asymmetrical RF signal in the bandwidth 44 to 130 MHz. The spectrum extension to this waveform must be limited by a band-pass filter superseding the IC.

The RF input is either the LNA input, if the level is –30 to 0 dBmVrms, or the DEMOD input if the level is –20 to +10 dBmVrms. The amplified RF signal is then mixed with two clocks in quadrature to provide the base-band demodulated In-phase (I) and Quad-phase (Q) signals.

The VCO operates at twice the RF carrier frequency in the bandwidth 88 - 260 MHz (one octave), therefore the 0 to 90° clocks are generated by a divider by 2.

The VCO frequency can be programmed by an integrated PLL that tunes the external LC tank circuit.

The raw I and Q generated signals contain spurious spikes, therefore each signal is passed through a third order active low-pass filter (RC cell + Sallen-Key structure), whose cut-off frequency is set by external components. The filtered I and Q data signals are then amplified to provide balanced buffer outputs.

The data sent to the PLL is loaded in bursts, framed by signal $\overline{EN}$. Programming clock edges, together with their relevant data bits, are ignored until $\overline{EN}$ becomes active (LOW). The internal latches are updated with the latest programming data when $\overline{EN}$ returns to inactive (HIGH). The last 14 bits only are retained within the programming register. No check is made on the number of clock pulses received while programming is enabled. An active clock edge causing a shift of the data bits is generated when $\overline{EN}$ goes HIGH while CLOCK is still LOW. The main divider ratio and the reference divider ratio are provided via the serial bus (see Table 1).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	6.0	V
$V_{(max)}$	maximum voltage on all pins except pin 9 (5 V)	–0.3	V_{CC}	V
t_{sc}	maximum short circuit duration on outputs	–	10	s
T_{stg}	storage temperature	–40	+150	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C
T_{amb}	operating ambient temperature	0	70	°C
$V_{CC(tune)}$	tuning voltage supply	–0.3	30	V

HANDLING

HBM ESD: The IC pins withstand 2 kV except pin 26 (1750 V).

MM ESD: The IC pins withstand 100 V except pins 2 and 31 (75 V).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	65	K/W

CHARACTERISTICS

Measured in application circuit with the following conditions: V_{CC} = 5 V; T_{amb} = 25°C. All AC units are RMS values, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA1}	analog supply voltage		4.75	5	5.25	V
I_{CCA1}	analog supply current		–	23	–	mA
V_{CCA2}	analog supply voltage		4.75	5	5.25	V
I_{CCA2}	analog supply current		–	18	–	mA
V_{CCA3}	analog supply voltage		4.75	5	5.25	V
I_{CCA3}	analog supply current		–	29	–	mA
$V_{cc(o)}$	output supply voltage		4.75	5	5.25	V
$I_{cc(o)}$	output supply current		–	17	–	mA
V_{CCD}	digital supply voltage		4.75	5	5.25	V
I_{CCD}	digital supply current		–	13	–	mA
$V_{CC(tune)}$	tuning supply voltage		–	–	30	V
Low noise amplifier: R_s = 75 Ω/R_i = 75 Ω unless otherwise specified						
$V_{I(DC)}$	DC input level	internally set	–	0.85	–	V
V_i	input level		–30	–	0	dBmV
f_i	input carrier frequency		44	–	130	MHz
R_i	input resistance		–	75	–	Ω
C_i	input capacitance		–	2.5	–	pF
R_{LLNA}	input return loss		–	–15	–	dB
NF_{LNA}	noise figure		–	7	11	dB
$V_{leak(LO)}$	LO leakage on pin at LNA_IN	$f_{N \times LO}$ = 140 – 860 MHz; pin LNA_OUT connected to DEMOD_IN	–	–	–15	dBmV
		$f_{LO/2}$ = 70 – 130 MHz; pin LNA_OUT connected to DEMOD_IN	–	–35	–30	dBmV
G_{LNA}	LNA gain	f = 100 MHz; $V_{I(LNA)}$ = 0 dBmV	8	10	–	dB
V_o	output level	–	–20	–	+10	dBmV
ΔV_o	output flatness	in 1 MHz bandwidth; $V_{I(LNA)}$ = 0 dBmV	–	0.25	0.5	dB
		44 to 70 MHz; $V_{I(LNA)}$ = 0 dBmV	–	0.50	–	dB
		70 to 130 MHz; $V_{I(LNA)}$ = 0 dBmV	–	1.3	1.5	dB
IM3	3rd-order intermodulation	2 carriers at +10 dBmV each at pin LNA_IN at 103 to 105 MHz	–	–	–60	dBc

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(DC)}$	DC output level		–	1.3	–	V
R_o	output resistance		–	75	–	Ω
Quadrature demodulator: R_s = 75 Ω/R_i = 20 kΩ unless otherwise specified						
$V_{I(DC)}$	DC input level	internally set	–	1	–	V
V_i	input level		–20	–	+10	dBmV
f_i	input carrier frequency		44	–	130	MHz
R_i	input resistance		–	75	–	Ω
C_i	input capacitance		–	2.5	–	pF
RL_I	input Return Loss		–	–12	–	dB
$V_{o(I-Q)}$	output level on pin I_OUT1 or Q_OUT1		–	22	–	dBmV
$B_{o(I-Q)}$	output 3 dB bandwidth	LO = 200 MHz; RF = 100 to 130 MHz	–	35	38	MHz
C/N	carrier to noise ratio at 500 kHz on pin at I_OUT1 or Q_OUT1	V_I = –20 dBmV; $V_{o(I\ and\ Q)}$ = 22 dBmV	–	88	–	dBc/Hz
		V_I = 10 dBmV; $V_{o(I\ and\ Q)}$ = 22 dBmV	–	93	–	dBc/Hz
$V_{leak(LO)}$	LO leakage on pin DEMOD_IN	f_{LO} = 140 to 260 MHz; $f_{LO/2}$ = 70 to 130 MHz	–	–	–15	dBmV
$V_{AGC(r)}$	AGC range	f_{LO} = 200 MHz; f_{RF} = 100.25 MHz at –20 to +10 dBmV; f_{BF} = 250 kHz at 22 dBmV	30	–	–	dB
$V_{AGC(s)}$	AGC slope maximum	f_{LO} = 200 MHz; f_{RF} = 100.25 MHz at –20 to +10 dBmV; f_{BF} = 250 kHz at 22 dBmV	–	30	–	dB/V
V_{AGC}	gain control voltage at AGC_IN		10% V_{CCA}	–	90% V_{CCA}	V
G_{max}	max. conversion gain	f_{LO} = 260 MHz; f_{RF} = 130.25 MHz at –20 dBmV; V_{AGC} = 4.5 V	42	–	–	dB
G_{min}	min. conversion gain	f_{LO} = 140 MHz; f_{RF} = 70.25 MHz at 10 dBmV V_{AGC} = 0.5 V	–	–	12	dB
$\Delta\Phi_{I-Q}$	phase error between I and Q channels	f_{LO} = 140 to 260 MHz; f_{RF} = 70.25 to 130.25 MHz; f_{BF} = 250 kHz at 22 dBmV over specified input range	–	±3	–	deg
ΔG_{I-Q}	gain error between I and Q channels	f_{LO} = 140 to 260 MHz; f_{RF} = 70.25 to 130.25 MHz; f_{BF} = 250 kHz at 22 dBmV over specified input range	–	±1	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta\Phi_{I-Q}$	phase error between I and Q channels	f_{LO} = 88 to 140 MHz; f_{RF} = 44.25 to 70.25 MHz; f_{BF} = 250 kHz at 22 dBmV over specified input range	–	±3	–	deg
ΔG_{I-Q}	gain error between I and Q channels	f_{LO} = 88 to 140 MHz; f_{RF} = 44.25 to 70.25 MHz; f_{BF} = 250 kHz at 22 dBmV over specified input range	–	±1	–	dB
IM3	3rd-order intermodulation in I and Q channels	see Fig.3	–	–	–45	dBc
IM2	2nd-order intermodulation in I and Q channels	see Fig.3	–	–	–40	dBc
AMREJ	AM rejection at I and Q channels	guaranteed by design; see Fig.4	–	–	–38	dBc
$\Delta V_{o(I/Q)}$	output flatness at I and Q outputs	in 1 MHz bandwidth	–	0.25	–	dB
		f = 40 to 70 MHz	–	3	–	dB
		f = 70 to 130 MHz	–	3	–	dB
$V_{o(DC)}$	DC output level		–	2.5	–	V
R_o	output resistance		–	400	–	Ω
Output section: R_s = 400 Ω/R_i = 4 kΩ/R on pin I_OUT2 or Q_OUT2 = 20 kΩ unless otherwise specified						
$V_{I(DC)}$	DC input voltage		–	3.6	–	V
V_i	input level		–	22	–	dBmV
R_i	input resistance		–	17.5	–	kΩ
C_i	input capacitance		–	0.4	–	pF
G_O	gain from I-Q_IN1 to I-Q_OUT2	f_{BF} = 1 MHz at 22 dBmV	–	3.8	–	dB
$\Delta V_{o(I-Q\_out2)}$	output flatness on pins I_OUT2 and Q_OUT2	f_{BF} = 0 to 1.5 MHz	–	0.25	–	dB
		f_{BF} = 0 to 6 MHz at 22 dBmV input	–	1	–	dB
$V_{o(flt)}$	DC output level at filter output		–	2.6	–	V
R_o	output resistance	f < 20 MHz	–	250	–	Ω
H_2	2nd harmonic	f_{BF} = 1 MHz at 48 dBmV output	–	–40	–35	dBc
H_3	3rd harmonic	f_{BF} = 1 MHz at 48 dBmV output	–	–45	–40	dBc
IM3	3rd-order intermodulation at pins I_OUT and Q_OUT	see Fig.5	–	–50	–45	dBc
$\alpha_{CT(I-Q)}$	crosstalk between I and Q channels	f = 5 MHz; see Fig.6	–	–40	–30	dBc
N_o	output noise power at 500 kHz from carrier	see Fig.7	–	–56	–	dBmv/Hz
G_{I-Q}	gain from I-Q_IN1 to I-Q_OUT	f_{BF} = 1 MHz at 22 dBmV input	–	27	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{1(I-Q)}$	DC output level on pin I-Q_OUT		–	3.1	–	V
$R_{o(dif)}$	output differential resistance		–	460	–	Ω
Overall: R_s = 75 Ω/R_i = 4 kΩ unless otherwise specified						
V_o	voltage output on pins I_OUT and Q_OUT	see Fig.8	–	48	–	dBmV
LO_{lev}	LO level on pins I_OUT and Q_OUT	see Fig.8	–	–	–45	dBc
S_o	spurious emission on pins I_OUT and Q_OUT	f = 0 to 5 MHz; see Fig.8	–	–40	–	dBc
ΔG_{I-Q}	gain error on pins I_OUT and Q_OUT	see Fig.8	–	±1	–	dB
AMR	AM rejection in I and Q channels	guaranteed by design; see Fig.9	–	–	–40	dBc
IM3	3rd-order intermodulation	guaranteed by design; see Fig.10	–	–	–45	dBc
Voltage Controlled Oscillator (VCO)						
$f_{vco(min)}$	min. oscillation frequency	note 1	–	88	–	MHz
$f_{vco(max)}$	max. oscillation frequency	note 1	–	260	–	MHz
$\alpha N_{(osc)}$	oscillator phase noise	at 10 kHz	–	–75	–	dBc/Hz
		at 100 kHz	–	–95	–	dBc/Hz
Phase Locked Loop (PLL)						
Step	frequency step size	at pin VCO output	100	–	500	kHz
RD	fixed reference divider ratio		–	2	–	–
RDR	programmable reference divider ratio		2	–	80	–
ND	programmable fix main divider ratio		–	4	–	–
NDR	main divider ratio		128	–	2600	–
$I_{(CP)}$	charge pump current		–	300	–	µA
Crystal oscillator						
f_{xtal}	crystal frequency	r_{xtal} = 25 to 200 Ω	1	–	4	MHz
Z_i	crystal oscillator input impedance (absolute value)	f_{xtal} = 4 MHz	600	1200	–	Ω
$V_{I(DC)}$	DC input level		–	2.9	–	V
V_i	input level		–	30	–	mVrms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
3-wire bus						
V_{IL}	input Low level	guaranteed by design	–	–	0.8	V
V_{IH}	input High level	guaranteed by design	2.4	–	–	V
f_{clk}	clock frequency	guaranteed by design	–	330	–	kHz
t_{su}	input data to CLK set-up time	guaranteed by design	–	2	–	µs
t_h	input data to CLK hold time	guaranteed by design	–	1	–	µs
$t_{d(strt)}$	delay to rising clock edge	guaranteed by design	–	3	–	µs
$t_{d(stp)}$	delay from last clock edge	guaranteed by design	–	3	–	µs

Notes

1. The frequency range of the receiver is 44 to 130 MHz. The local oscillator (LO) operates at twice the output frequency (88 to 260 MHz). Frequency control by varicap diodes allows a variation over one octave.
2. Crystal oscillator. The crystal oscillator uses a 4, 2 or 1 MHz crystal in series with a capacitor. The crystal is parallel resonant with load capacitance of 18 to 20 pF. Connection to V_{CC} is preferred but can also be to GND.

Note to characteristics

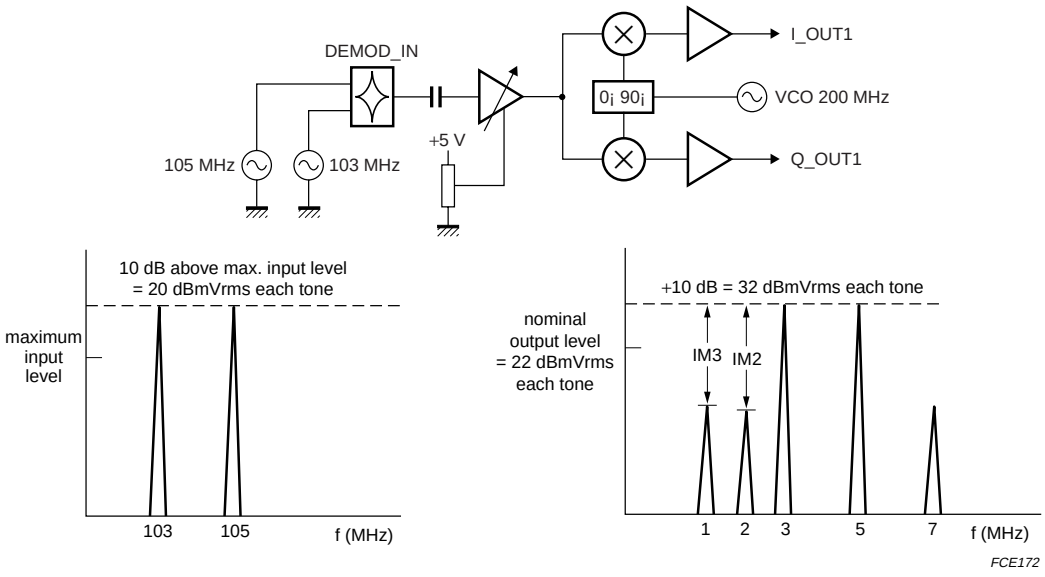


Fig.3 IM2 and IM3 measurement of the demodulator.

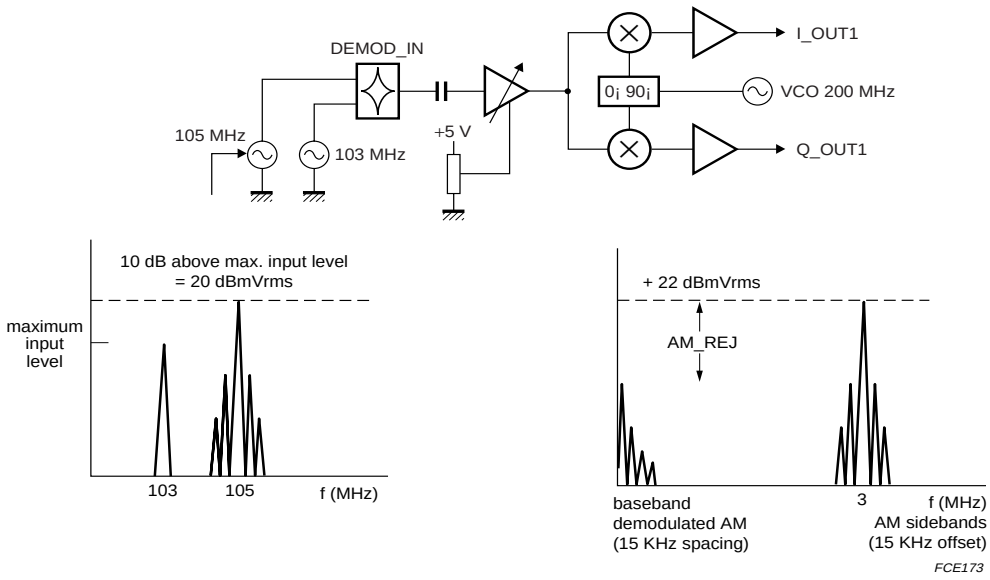


Fig.4 AM rejection test.

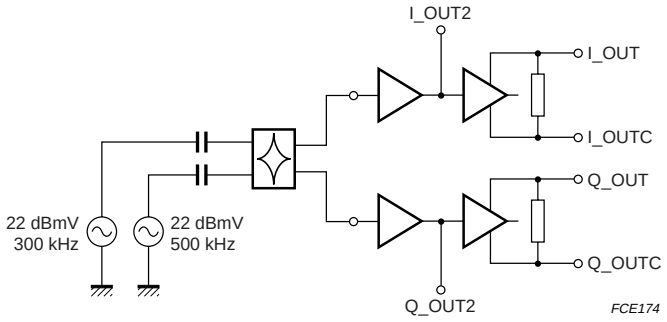
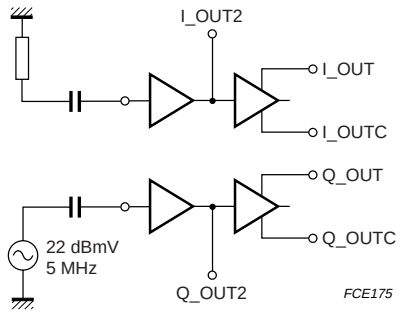


Fig.5 IM3 measurement of the output section.



(1) Measure I and Q, α is the difference between the two carriers.

Fig.6 Crosstalk measurement.

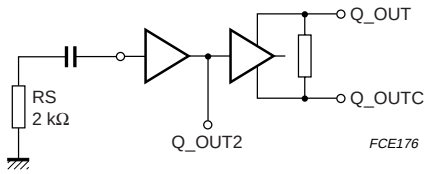
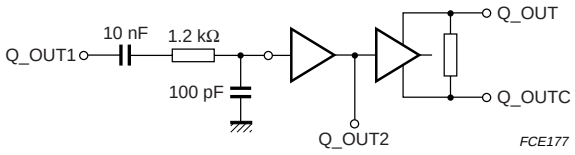


Fig.7 Noise measurement.



LNA input: –15 dBmV; AGC set in order to have a 250 kHz output sine wave at 48 dBmV; f_{ref} = 70 to 130 MHz; f_{lo} = 140 to 260 MHz.

Fig.8 LO level, spurious, I/Q gain error and V_o measurements.

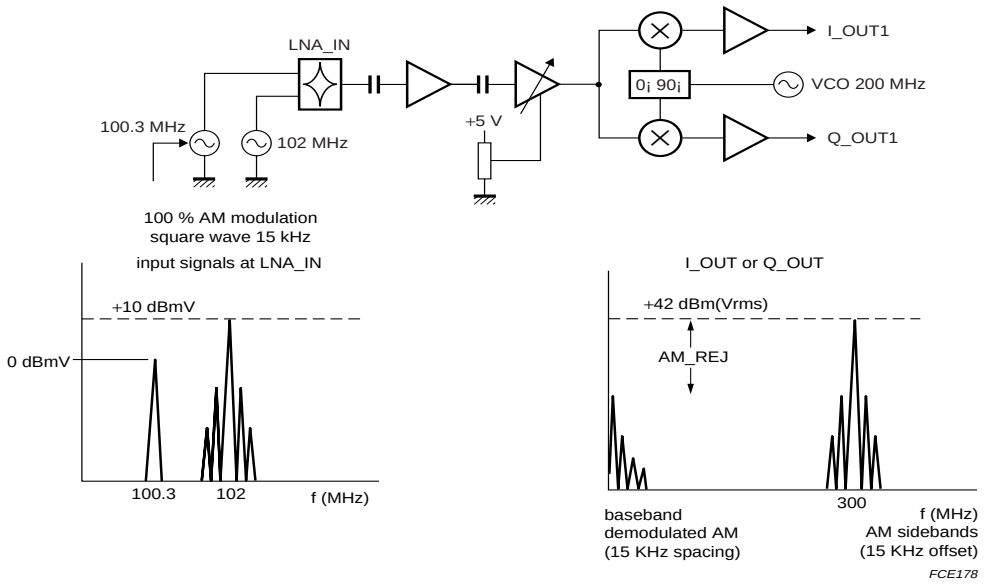


Fig.9 Overall AM rejection measurement.

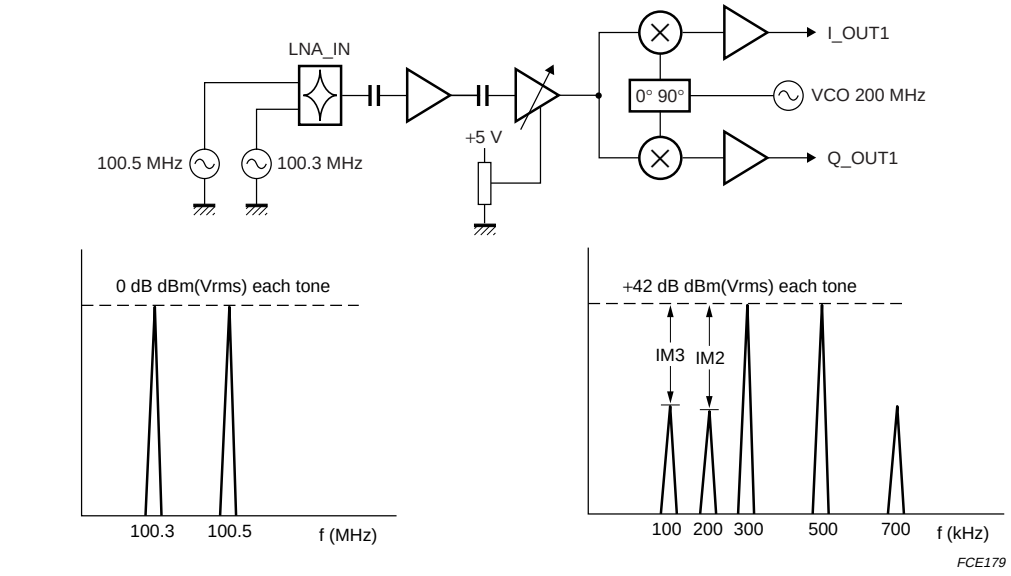


Fig.10 Overall IM3 measurement.

TIMING CHARACTERISTICS

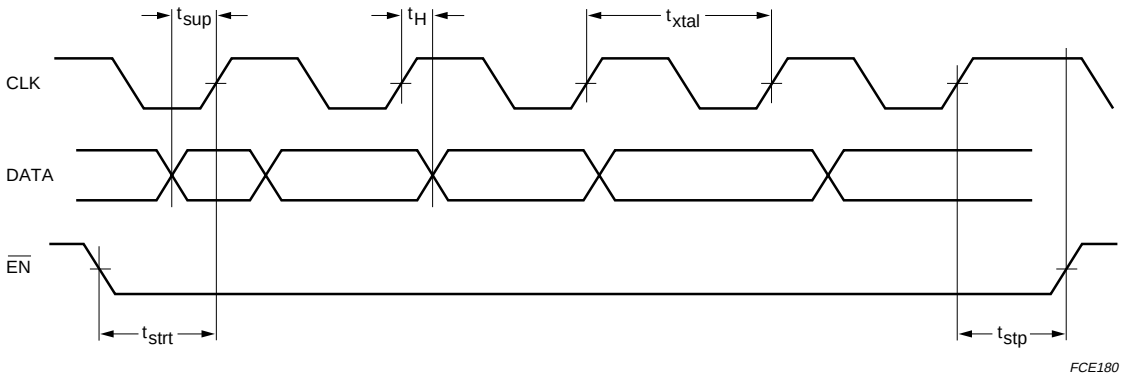


Fig.11 Logic interface signals.

DATA FORMAT

Table 1

FIRST													**LAST**
Data													
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	AD1	AD0
Reference ratio													
X	X	X	X	R7	R6	R5	R4	R3	R2	R1	R0	0	1
Principal ratio													
P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	1	1

APPLICATION INFORMATION

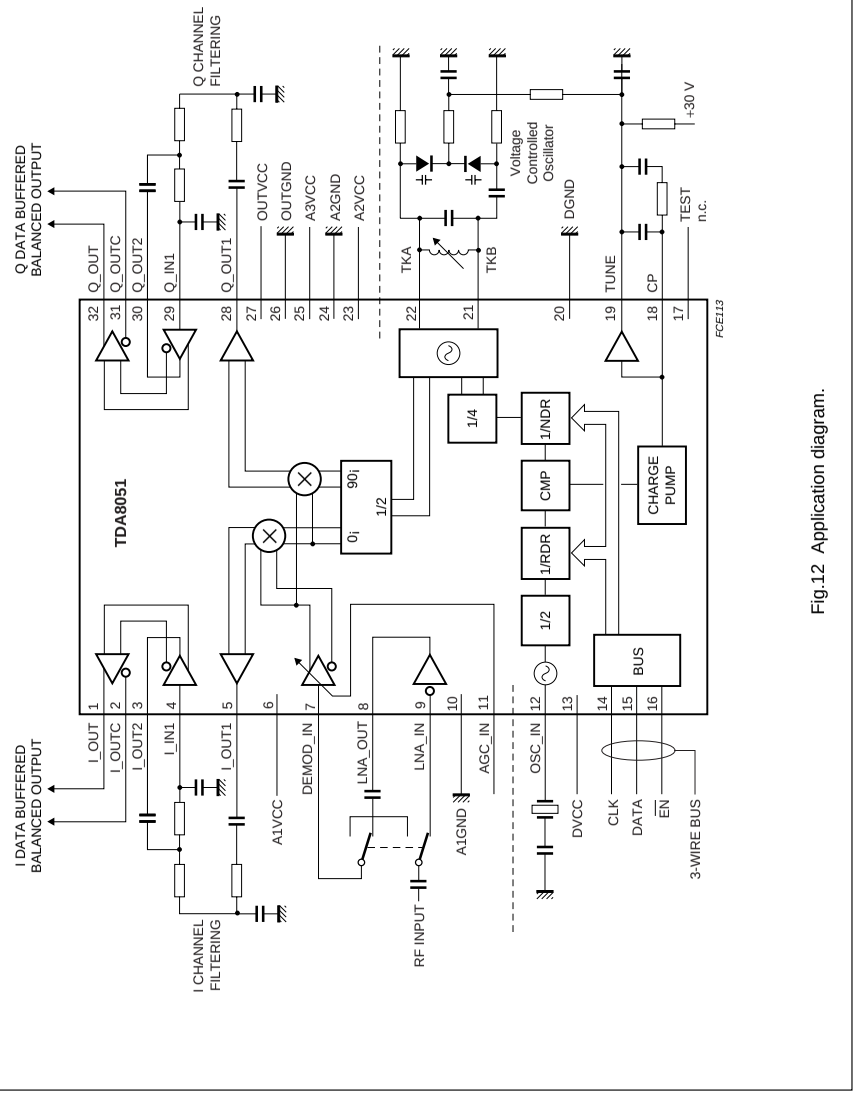
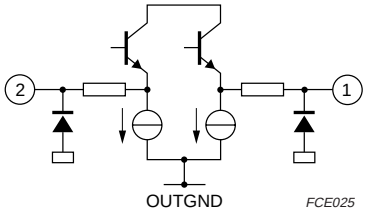
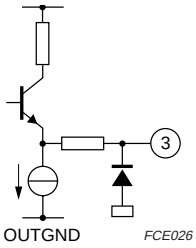
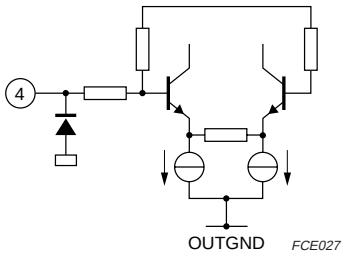
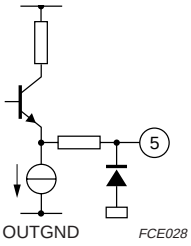
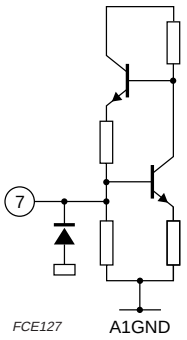
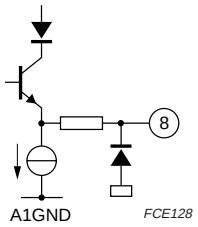
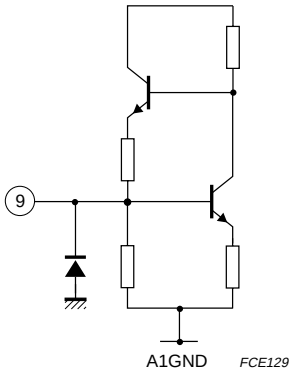
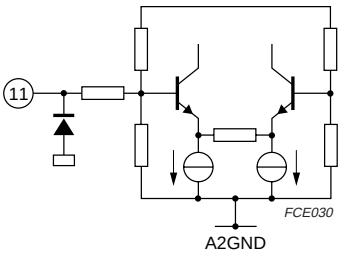
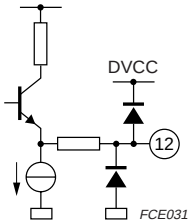
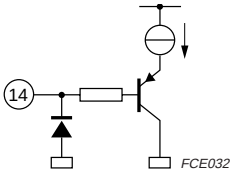
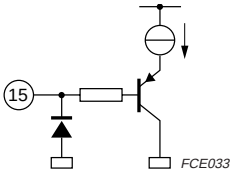
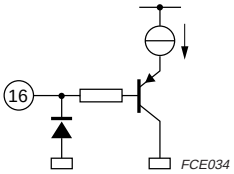
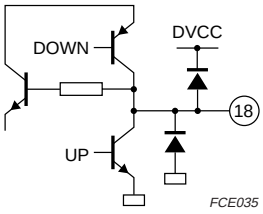


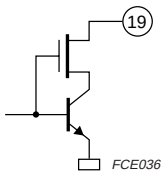
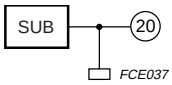
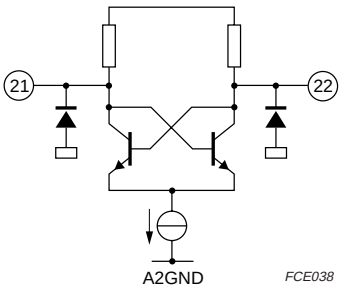
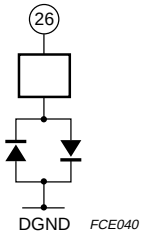
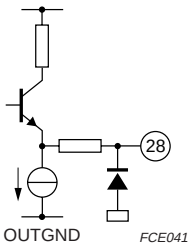
Fig.12 Application diagram.

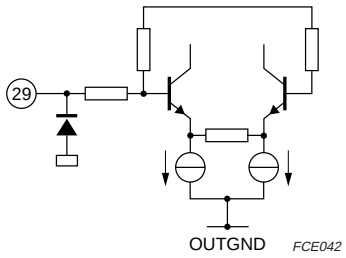
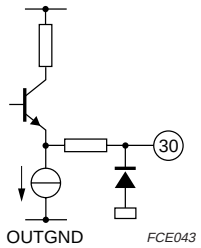
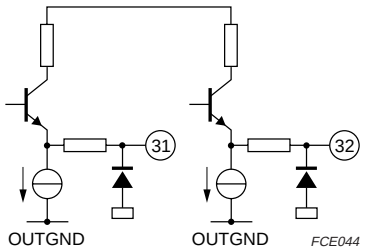
INTERNAL PIN CONFIGURATIONS

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
I_OUT I_OUTC	1 2		3.1 V 3.1 V
I_OUT2	3		2.6 V
I_IN1	4		3.6 V
I_OUT1			2.5 V
A1VCC	6	Analog supply voltage 1	5 V

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
DEMOD_IN	7		1 V
LNA_OUT	8		1.3 V
LNA_IN	9		0.9 V
A1GND	10	analog ground 1	0. V
AGC_IN	11		–

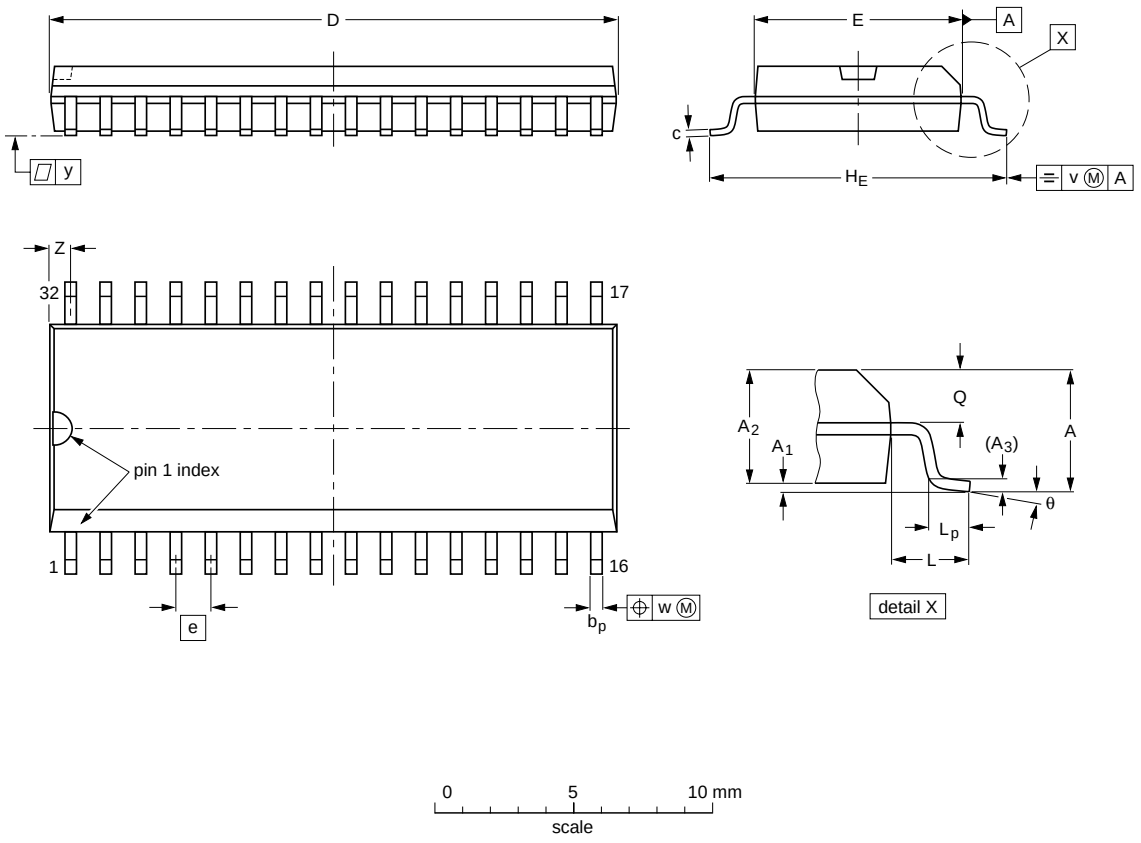
SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
OSC_IN	12		3.0 V
DVCC	13	digital supply voltage	5 V
CLK	14		n.a.
DATA	15		n.a.
$\overline{EN}$	16		n.a.
TEST	17	not connected	n.a.
CP	18		1.9 V

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
TUNE	19		V_{VT}
DGND	20		0 V
TKB TKA	21 22		2.4 V 2.4 V
A2VCC	23	analog DC supply voltage 2	5 V
A2GND	24	analog ground 2	0 V
A3VCC	25	analog supply voltage 3	5 V
OUTGND	26		0 V
OUTVCC	27	output amplifiers supply voltage	5 V
Q_OUT1	28		2.5 V

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
Q_IN1	29		3.6 V
Q_OUT2	30		2.6 V
Q_OUTC Q_OUT	31 32		3.1 V 3.1 V

PACKAGE OUTLINE

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~95-01-25~~ 97-05-22

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
HLQFP, HSQFP, HSOP, SMS	not suitable(2)	suitable
PLCC(3), SO	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SQFP	not suitable	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands 545004/25/02/pp24 Date of release: 1999 Aug 20 Document order number: 9397 750 04691

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