19-0108; Rev 2; 10/96

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

308ksps ADC with DSP Interface and 78dB SINAD

MAX121

General Description

The MAX121 is a complete, BiCMOS, serial-output, sampling 14-bit analog-to-digital converter (ADC) that combines an on-chip track/hold and a low-drift, low-noise, buried-zener voltage reference with fast conversion speed and low power consumption. The throughput rate is as high as 308k samples per second (ksps). The full-scale analog input range is ±5V.

The MAX121 utilizes the successive-approximation architecture with a high-speed DAC to achieve both fast conversion speeds and low-power operation. Operating with +5V and -12V or -15V power supplies, power consumption is only 210mW.

The MAX121 can be directly interfaced to the serial port of most popular digital-signal processors, and comes in space-saving 16-pin DIP and SO and smaller 20-pin SSOP packages. The MAX121 operates with TTL- and CMOS-compatible clocks in the frequency range from 0.1MHz to 5.5MHz. All logic inputs and outputs are TTL- and CMOS-compatible. This data sheet includes application notes for easy interface to TMS320, µPD77230, and ADSP2101 digital-signal processors, as well as µPs using the Motorola SPI and QSPI interface standards.

Applications

Digital Signal Processing

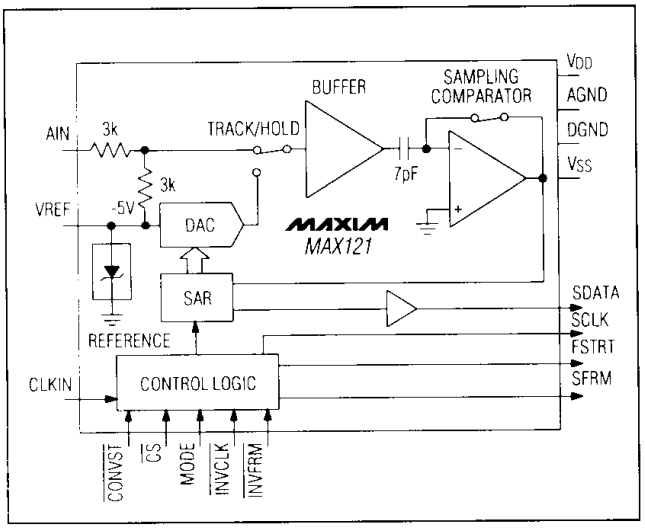
Audio and Telecom Processing

Speech Recognition and Synthesis

DSP Servo Control

Spectrum Analysis

Functional Diagram



Features

- ♦ 14-Bit Resolution
- ♦ 2.9µs Conversion Time/308ksps Throughput
- ♦ 400ns Acquisition Time
- ♦ Low Noise and Distortion:
  78dB SINAD
  -85dB THD
- ♦ ±5V Bipolar Input Range, Overvoltage Tolerant to ±15V
- ♦ 210mW Power Dissipation
- ♦ Continuous-Conversion Mode Available
- ♦ 30ppm/°C, -5V Internal Reference
- ♦ Interfaces to DSP Processors
- ♦ 16-Pin DIP and SO Packages, 20-Pin SSOP Package

Ordering Information

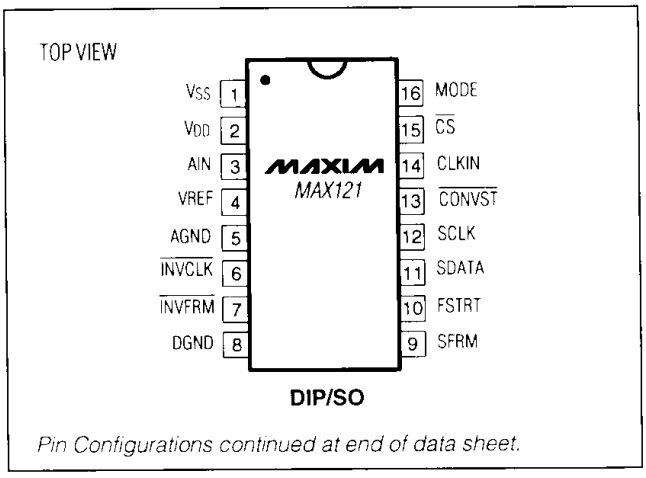
PART	TEMP. RANGE	PIN-PACKAGE
MAX121CPE	0°C to +70°C	16 Plastic DIP
MAX121CWE	0°C to +70°C	16 Wide SO
MAX121CAP	0°C to +70°C	20 SSOP**
MAX121C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

* *Contact factory for dice specifications.*

** *20-pin SSOP is 50% smaller than 16-pin SOIC.*

Pin Configurations



Pin Configurations continued at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +6V
V_{SS} to DGND ..... +0.3V to -17V
AIN to AGND ..... ±15V
AGND to DGND ..... ±0.3V
Digital Inputs to DGND ..... -0.3V, (V_{DD} + 0.3V)
(CS, CONVST, MODE, CLKIN, INVCLK, INVFRM)
Digital Outputs to DGND ..... +0.3V, (V_{DD} + 0.3V)
(SFRM, FSTRT, SCLK, SDATA)

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) .. 800mW
Operating Temperature Ranges:
MAX121C__ ..... 0°C to +70°C
MAX121E__ ..... -40°C to +85°C
MAX121MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.75V to 5.25V, V_{SS} = -10.8V to -15.75V, MAX121C/E f_{CLK} = 5.5MHz, MAX121M f_{CLK} = 5MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (MAX121C/E: f_S = 308kHz, AIN = 10Vp-p, 50kHz) (MAX121M: f_S 278kHz, AIN = 10Vp-p, 50kHz)							
Signal-to-Noise Ratio	SINAD	Including distortion	MAX121C	75	78		dB
			MAX121E/M	73	77		
Total Harmonic Distortion	THD	First five harmonics	MAX121C/E		-85	-77	dB
			MAX121M		-83	-76	
Spurious-Free Dynamic Range	SFDR		MAX121C/E	77	86		dB
			MAX121M	76	84		
ACCURACY							
Resolution	RES			14			Bits
Differential Nonlinearity (Note 1)	DNL	12 bits no missing codes over temp. range			±1.5		LSB
Integral Nonlinearity	INL				±2		LSB
Bipolar Zero Error		Code 00..00 to 00..01 transition, near AIN = 0V				±10	mV
		Temperature drift			±1		ppm/°C
Full-Scale Error (Notes 1, 2)		Including reference; adjusted for bipolar zero error; T_A = +25°C				±0.2	%
Full-Scale Temperature Drift		Excluding reference			±1		ppm/°C
Power-Supply Rejection		V_{DD} only, 5V ±5%			±1/2	±2	LSB
		V_{SS} only, -12V ±10%			±1	±2	
		V_{SS} only, -15V ±5%			±1	±2	
ANALOG INPUT							
Input Range				-5		+5	V
Input Current		AIN = 5V (R_{IN} approximately 6kΩ to REF)				2.5	mA
Input Capacitance (Note 3)						10	pF
Full-Power Bandwidth					1.5		MHz

ELECTRICAL CHARACTERISTICS (continued)

(VDD = 4.75V to 5.25V, VSS = -10.8V to -15.75V, MAX121C/E fCLK = 5.5MHz, MAX121M fCLK = 5MHz, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE							
Output Voltage		No external load, AIN = 5V, TA = +25°C		-5.02		-4.98	V
External Load Regulation		0mA < ISINK < 5mA, AIN = 0V				5	mV
Temperature Drift (Note 4)		MAX121C/E				±30	ppm/°C
		MAX121M				±35	
CONVERSION TIME							
Synchronous	tCONV	16 tCLK	MAX121C/E			2.91	µs
			MAX121M			3.20	
Clock Frequency	fCLK		MAX121C/E	0.1		5.5	MHz
			MAX121M	0.1		5.0	
DIGITAL INPUTS (CLKIN, $\overline{CONVST}$, $\overline{CS}$)							
Input High Voltage	VIH			2.4			V
Input Low Voltage	VIL					0.8	V
Input Capacitance (Note 3)						10	pF
Input Current		VDD = 0V or VDD				±5	µA
DIGITAL OUTPUTS (SCLK, SDATA, FSTRT, SFRM)							
Output Low Voltage	VOL	ISINK = 1.6mA				0.4	V
Output High Voltage	VOH	ISOURCE = 1mA		VDD-0.5			V
Leakage Current	ILKG	VOUT = 0V or VDD				±5	µA
Output Capacitance (Note 3)						10	pF
POWER REQUIREMENTS							
Positive Supply Voltage	VDD	By supply-rejection test		4.75		5.25	V
Negative Supply Voltage	VSS	By supply-rejection test		-10.8		-15.75	V
Positive Supply Current	IDD	VDD = 5.25V, VSS = -15.75V, AIN = 0V, $\overline{CS}$ = $\overline{CONVST}$ = MODE = 5V			9	15	mA
Negative Supply Current	ISS	VDD = 5.25V, VSS = -15.75V, AIN = 0V, $\overline{CS}$ = $\overline{CONVST}$ = MODE = 5V			14	20	mA
Power Dissipation		VDD = 5V, VSS = -12V, AIN = 0V, $\overline{CS}$ = $\overline{CONVST}$ = MODE = 5V			213	315	mW

Note 1: These tests are performed at VDD = +5V, VSS = -15V. Operation over supply is guaranteed by supply-rejection tests.
Note 2: Ideal full-scale transition is at +5V - 3/2LSB = +4.9991V, adjusted for offset error.
Note 3: Guaranteed, not tested.
Note 4: Temperature drift is defined as the change in output voltage from +25°C to TMIN or TMAX. It is calculated as TC = (ΔVREF/VREF) / ΔT.

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TIMING CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = -12V or -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX121C/E		MAX121M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CONVST Pulse Width (Note 6)	t_{CW}		20			30		35		ns
Data-Access Time	t_{DA}	C_L = 50pF		25	50		65		80	ns
Data-Hold Time	t_{DH}			25	50		65		80	ns
CLKIN to SCLK	t_{CD}	C_L = 50pF		40	65		85		105	ns
SCLK to SDATA Skew	t_{SC}	C_L = 50pF			±65		±80		±100	ns
SCLK to SFRM or FSTRT Skew	t_{SC}	C_L = 50pF			±25		±35		±40	ns
Acquisition Time (Note 6)	t_{AQ}		400			400		400		ns
Aperture Delay	t_{AP}			10						ns
Aperture Jitter				30						ps
Clock Setup/Hold Time	t_{CK}		10		50	10	50	10	50	ns

Note 5: Control inputs specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V. Output delays are measured to +0.8V if going low, or +2.4V if going high. For a data-hold time, a change of 0.5V is measured. See Figures 4 and 5 for load circuits.

Note 6: Guaranteed, but not tested.

Pin Description

PIN		NAME	FUNCTION
DIP/SO	SSOP		
1	1	V_{SS}	Negative Power Supply: -12V or -15V
2	2	V_{DD}	Positive Power Supply: +5V
3	3	AIN	Sampling Analog Input: ±5V bipolar input range
4	4	VREF	-5V Reference Output. Bypass to AGND with 22µF II 0.1µF.
5	7	AGND	Analog Ground
6	8	INVCLK	Invert Serial Clock. Connect to DGND to invert the SCLK output (relative to CLKIN).
7	9	INVFRM	Invert Serial Frame. This input sets the polarity of the SFRM output as follows: If INVFRM = DGND, SFRM is high during a conversion. If INVFRM = V_{DD}, SFRM is low during a conversion.
8	10	DGND	Digital Ground
9	11	SFRM	Serial Frame Output. Normally high (INVFRM = V_{DD}), falls at the beginning of the conversion and rises at the end (after 16 t_{CLK}) signaling the end of a 16-bit frame.
10	12	FSTRT	Frame Start Output. High pulse that lasts one clock cycle, falling edge indicates that a valid MSB is available.
11	13	SDATA	Serial Data Output. MSB first, twos-complement binary output code.
12	14	SCLK	Serial Clock Output. Same polarity as CLKIN if INVCLK = V_{DD}, inverted CLKIN if INVCLK = DGND. Note that SCLK runs whenever CLKIN is active.
13	17	CONVST	Active-Low Convert Start Input. Conversions are initiated on falling edges.
14	18	CLKIN	Clock Input. Supply a TTL-/CMOS-compatible clock from 0.1MHz to 5.5MHz, 40%-60% duty cycle.
15	19	CS	Active-Low Chip-Select Input. CS = DGND enables the three-state outputs. Also, if CONVST is low, initiates a conversion on the falling edge of CS.
16	20	MODE	Hardwire to set operational mode: V_{DD}: single conversions, DGND: continuous conversions
	5, 6, 15, 16	N.C.	No Connect – not internally connected.

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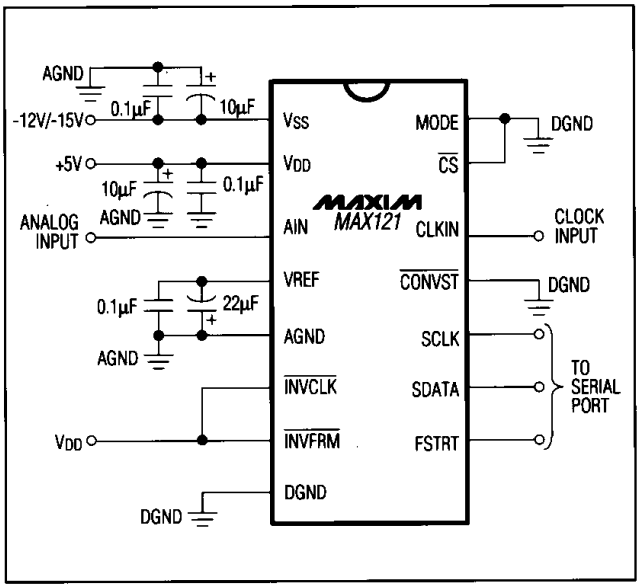

Figure 1. MAX121 In the Simplest Operational Mode (Continuous-Conversion Mode)

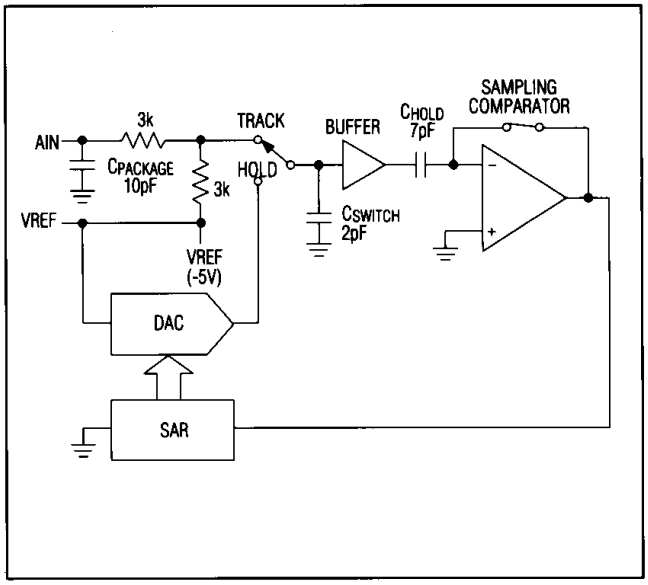

Figure 2. Equivalent Input Circuit

Detailed Description

ADC Operation

The MAX121 uses successive approximation and input track/hold (T/H) circuitry to convert an analog signal to a 14-bit serial digital output code. The control logic interfaces easily to most microprocessors (µPs) and digital-signal processors (DSPs), requiring only a few passive components for most applications. The T/H does not require an external capacitor. Figure 1 shows the MAX121 in its simplest operational configuration.

Analog Input Track/Hold

The Equivalent Input Circuit (Figure 2), illustrates the sampling architecture of the ADC's analog comparator. An internal buffer charges the hold capacitor to minimize the required acquisition time between conversions. The analog input appears as a 6kΩ resistor in parallel with a 10pF capacitor.

Between conversions, the buffer input is connected to AIN through the input resistance. When a conversion starts, the buffer input is disconnected from AIN, thus sampling the input. At the end of the conversion, the buffer input is reconnected to AIN, and the hold capacitor tracks the input voltage.

The T/H is in its tracking mode whenever a conversion is not in progress. Hold mode starts approximately 10ns after a conversion is initiated (aperture delay). The variation in this delay from one conversion to the next (aperture jitter) is typically 30ps. Figures 7-9 detail the track/hold mode and interface timing for the three different interface modes.

Internal Reference

The MAX121 -5.00V buried-zener reference biases the internal DAC. The reference output is available at the VREF pin and must be bypassed to the AGND pin with a 0.1µF ceramic capacitor in parallel with a 22µF or greater electrolytic capacitor. The electrolytic capacitor's equivalent series resistance (ESR) must be 100mΩ or less to properly compensate the reference output buffer. Sanyo's organic semiconductor capacitors work well; telephone and FAX numbers are provided below.

Sanyo Video Components (USA)
Phone: (619) 661-6835
FAX: (619) 661-1055
Sanyo Electric Company, LTD. (Japan)
Phone: 0720-70-1005
FAX: 0720-70-1174
Sanyo Fisher Vertriebs GmbH (Germany)
Phone: 06102-27041, ext. 44
FAX: 06102-27045

Proper bypassing minimizes reference noise and maintains a low impedance at high frequencies. The internal-reference output buffer can sink up to 5mA from an external load.

An external reference voltage can be used to overdrive the MAX121's internal reference, if the external reference lies within the range from -5.05V to -5.10V. The external reference must be capable of sinking a minimum of 5mA. The external VREF bypass capacitors are still required.

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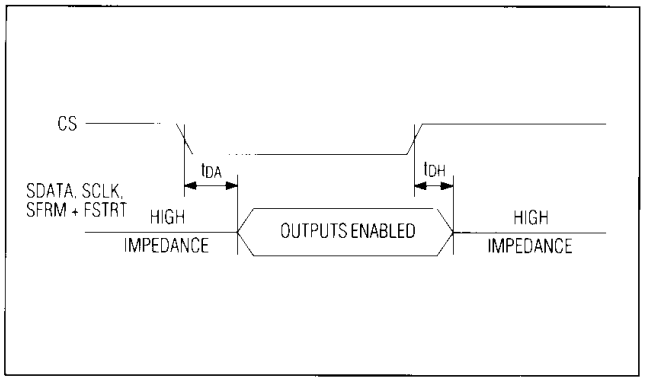

Figure 3. Data-Access + Data-Hold Timing

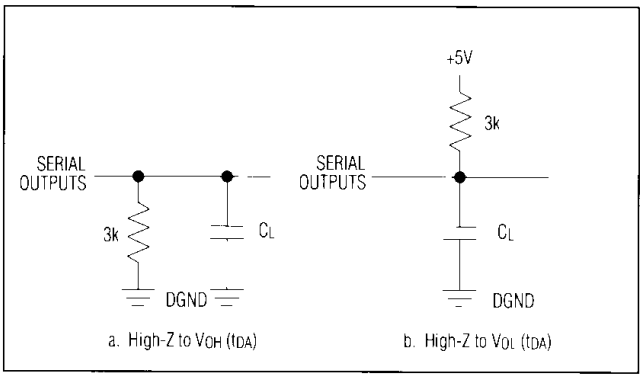

Figure 4. Load Circuits for Data-Access Time

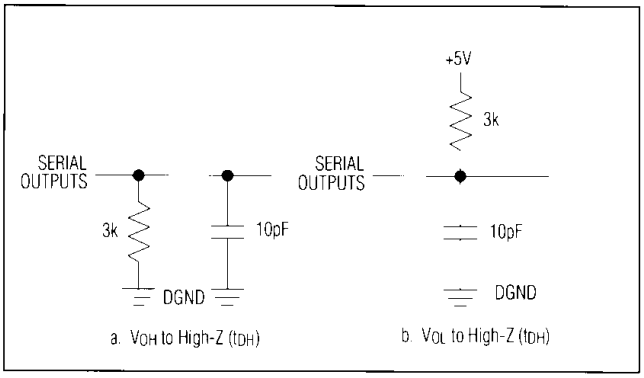

Figure 5. Load Circuits for Data-Hold Time

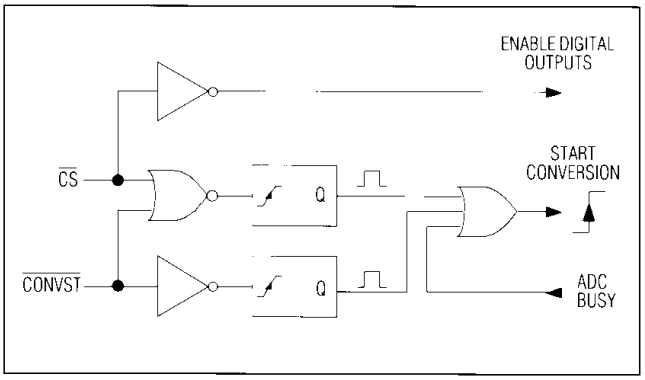

Figure 6. Conversion Control Logic

External Clock

The MAX121 requires a TTL-/CMOS-compatible clock for proper operation. The MAX121 accepts clocks in the frequency range from 0.1MHz to 5.5MHz when operating in mode 1 or mode 2 (see *Operating Modes* section). To satisfy the 400ns acquisition-time requirement with 2 clock cycles, the maximum clock frequency is limited to 5MHz when operating in mode 3 (continuous-conversion mode). The minimum clock frequency in all modes is limited to 0.1MHz due to the droop rate of the internal T/H.

Output Data Format

The conversion result is output as a 16-bit serial data stream, starting with the 14 data bits (MSB first) followed by 2 trailing zeros. The format of the output data is twos-complement binary. Data is clocked out of the SDATA pin on the rising edge of CLKIN.

The output data can be framed using either the FSTRT or the SFRM output. FSTRT (normally low) goes high for 1 clock cycle preceding the MSB. A falling edge on FSTRT indicates that the MSB is available on the SDATA output.

The SFRM output (normally high when $\overline{INVFRM}$ = V_{DD}) goes low coincident with the MSB appearing at the SDATA pin. SFRM returns high 16 clock cycles later. The polarity of SFRM can be inverted by tying the $\overline{INVFRM}$ input to DGND. A minimum of 18 clock cycles per conversion is required to obtain a valid SFRM output.

See Figure 3 for the data-access and data-hold timing diagram if several devices share the serial bus. The equivalent load circuits for data-access and data-hold timing are shown in Figures 4 and 5.

Digital Interface

The MAX121 serial interface is compatible with SPI and QSPI serial interfaces. In addition, two framing signals (FSTRT and SFRM) are provided to allow the MAX121 to easily interface to most digital-signal processors (DSP) with no external glue logic. The $\overline{INVCLK}$ input inverts the phase of SCLK relative to CLKIN, and the $\overline{INVFRM}$ input inverts the phase of the SFRM output. These control signals allow the MAX121 to directly interface to devices with many different serial-interface standards. Specific information for interfacing the MAX121 with SPI, QSPI and several DSP devices is included in the *Applications Information* section.

Timing and Control

The MAX121 has 3 possible modes of operation, as outlined in the timing diagrams of Figures 7-9 and discussed in the *Operating Modes* section.

In Mode 1, the $\overline{CONVST}$ input is used to control the start of the conversion. Mode 1 is intended for DSP and other applications where the analog input must be sampled at a precise instant in time.

In Mode 2, the $\overline{CS}$ input controls the start of the conversion. This mode is useful when several devices are multiplexed on the same serial data bus, since the MAX121 outputs are placed in a high-impedance state when $\overline{CS}$ is pulled high.

Mode 3 is the continuous-conversion mode. This mode is intended for data logging and similiar applications where the MAX121 is directly linked to memory through a first-in/first-out (FIFO) buffer or a direct memory access (DMA) port.

In all three operating modes, the start of conversion is controlled by either the $\overline{CS}$ or the $\overline{CONVST}$ input. Both of these inputs must be low for a conversion to take place. Figure 6 shows the logic equivalent for the conversion circuitry. Once the conversion is in progress, it cannot be restarted.

Operating Modes

Mode 1: $\overline{CONVST}$ Controls Conversion Starts (MODE = V_{DD}, $\overline{CS}$ = DGND)

Figure 7 shows the timing diagram for mode 1. In this mode, conversion start operations are controlled by the $\overline{CONVST}$ input.

A falling edge on the $\overline{CONVST}$ input places the T/H into the hold mode and starts a conversion in the successive-approximation register (SAR). The FSTRT (normally low) output goes high on the next rising clock edge and remains high for one clock cycle. On the next rising clock edge, FSTRT goes low and the SFRM output goes low ($\overline{INVFRM}$ = V_{DD}), indicating that the MSB is ready to be latched. SFRM remains high for 16 clock cycles (14 data bits plus 2 trailing zeros).

The T/H amplifier returns to the track mode when the 14th bit (D0) is clocked out of the SDATA pin. A new conversion can be initiated by the $\overline{CONVST}$ input after the 400ns minimum acquisition time has been satisfied.

$\overline{CS}$ must be low to start a conversion. In applications where the MAX121 interfaces with a dedicated serial port, $\overline{CS}$ can be hardwired to DGND. To interface the MAX121 to a multiplexed serial bus, $\overline{CS}$ can be externally driven low to enable conversions, or driven high to place the serial outputs into a high-impedance state.

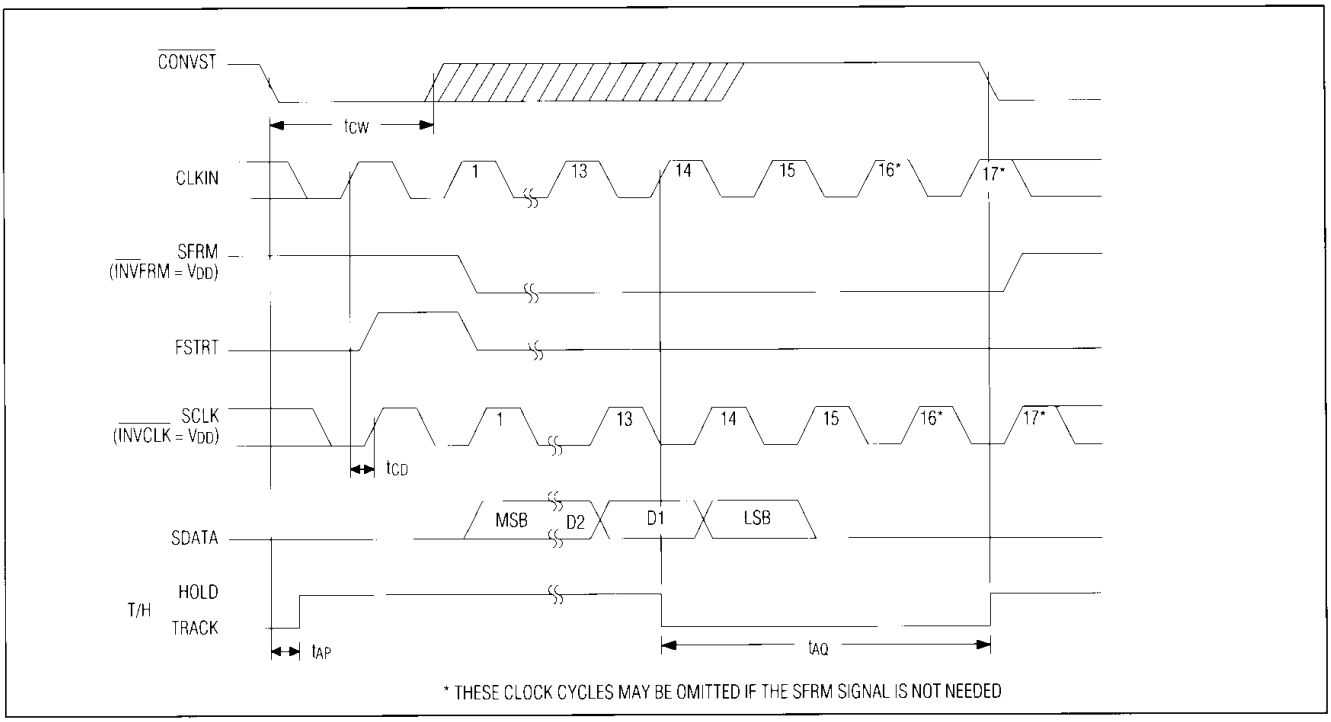

Figure 7. CONVST Controls Conversion Starts (Mode 1)

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Mode 2: $\overline{CS}$ Controls Conversion Starts (MODE = V_{DD}, $\overline{CONVST}$ = DGND)

Figure 8 shows the timing diagram for mode 2. In mode 2, $\overline{CS}$ controls the conversion start and enables the serial output pins. Mode 2 is useful in applications where the MAX121 shares the output data bus with other devices. When $\overline{CS}$ is driven high, the MAX121 is disabled and its serial outputs (SCLK, SDATA, SFRM and FSTRT) are placed into a high-impedance state.

A falling edge on the $\overline{CS}$ input places the T/H into the hold mode and starts a conversion in the SAR. The FSTRT and SFRM outputs can be used to frame the output data as described in the mode 1 section. $\overline{CS}$ must remain low for the duration of the conversion.

The T/H amplifier returns to the track mode when the 14th bit (D0) is clocked out of the SDATA pin. A new conversion can be initiated by the $\overline{CS}$ input after the 400ns acquisition time has been satisfied.

Mode 3: Continuous-Conversion Mode ($\overline{CONVST}$ = $\overline{CS}$ = MODE = DGND)

For applications that do not require precise control of sampling in time, such as data logging, the MAX121 can operate in continuous-conversion mode, directly linked to memory through DMA ports or a FIFO buffer.

In this mode, conversions are performed continuously at the rate of one conversion for every 16 clock cycles, which includes 2 clock cycles for the T/H acquisition time. To satisfy the 400ns minimum acquisition-time requirement within 2 clock cycles, the MAX121's maximum clock frequency is limited to 5MHz when operating in mode 3.

The FSTRT output is used to frame data, as described in the mode 1 section and the mode 3 timing diagram (Figure 9). The SFRM output is meaningless in mode 3, since it will not change state.

The MODE input should be hardwired to DGND, since this input must be low when the MAX121 powers up for proper operation of mode 3. To disable conversions, drive $\overline{CONVST}$ high. To put the serial outputs into a high-impedance state, drive $\overline{CS}$ high.

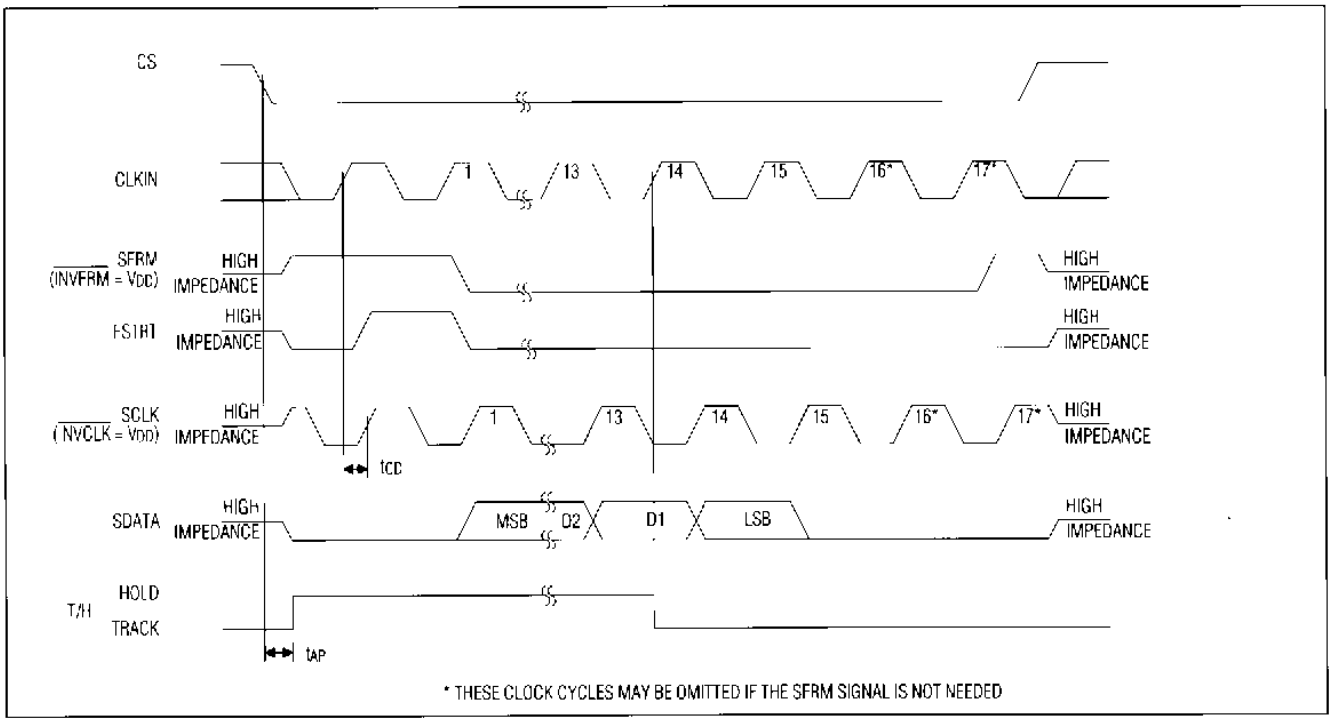

Figure 8. $\overline{CS}$ Controls Conversion Starts (Mode 2)

Applications Information

Initialization After Power-Up

Upon power-up, the first conversion of the MAX121 will be valid if the following conditions are met:

1) Allow 16 clock cycles for the internal T/H to enter the track mode, plus a minimum of 400ns in the track mode for the data-acquisition time.

2) Make sure the reference voltage has settled. Allow 0.5ms for each 1µF of reference bypass capacitance (11ms for a 22µF capacitor).

Clock and Control Synchronization

If the clock and conversion start inputs ($\overline{CONVST}$ or $\overline{CS}$ – see *Operating Modes* section) are not synchronized, the conversion time can vary from 15 to 16 clock cycles. The SAR always changes state on the rising edge of the CLKIN input. To ensure a fixed conversion time, refer to Figure 10 and the following guidelines:

For a conversion time of 15 clock cycles, the conversion start input(s) should go low at least 50ns before the next rising edge of CLKIN. For a conversion time of 16 clock cycles, the conversion start input(s) should go low within 10ns of the next rising edge of CLKIN. If the conversion start input(s) go low from 10ns to 50ns before the next rising edge of CLKIN, the number of clock cycles required is undefined and can be either 15 or 16. For best analog performance, the conversion start inputs must be synchronized with CLKIN.

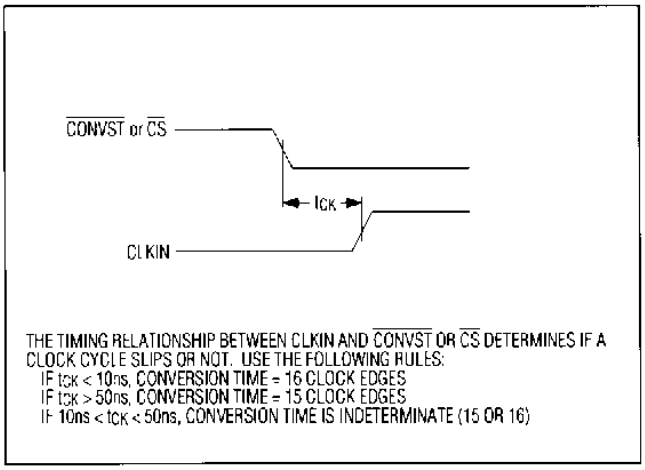

Figure 10. Clock and Control Synchronization

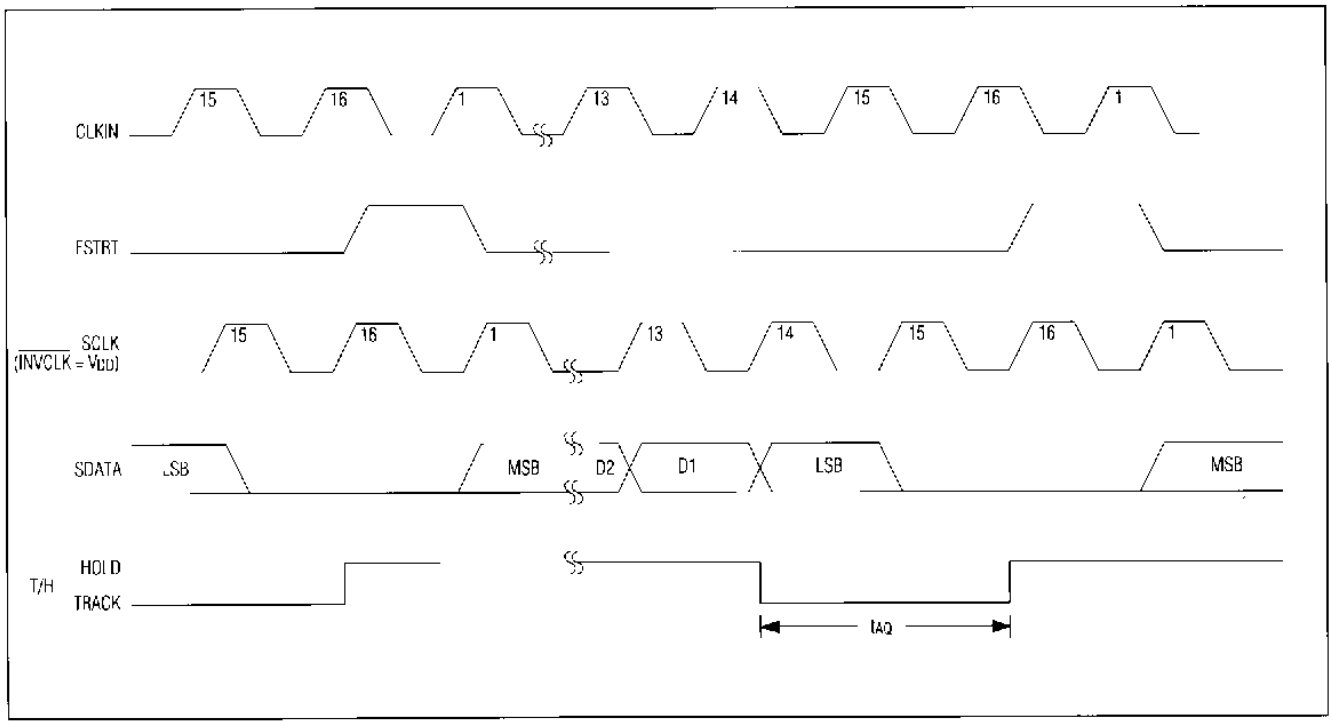

Figure 9. Continuous-Conversion Mode (Mode 3)

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Maximum Clock Rate for Serial Interface

The maximum serial clock rate depends upon the minimum setup time required by the receiving processor's serial data input and the ADC's maximum clock-to-data delay. The MAX121 allows two fundamentally different methods of clocking data into the processor. In the first clocking method, CLKIN is both the input clock to the MAX121 and the serial clock for the processor. With the second method, CLKIN is the input clock for the MAX121 while SCLK is the serial clock for shifting data into the processor. (See Figure 11.)

The first method would generally be used with simple serial-interface standards (such as SPI) where the processor does not support asynchronous data transfers. The maximum clock-to-data delay would be $t_{CD} + t_{SC}$. For this case, calculate the maximum serial clock rate with the following formula:

$$f_{CLKIN} = (1/2) \times 1/(t_{SU} + t_{CD} + t_{SC})$$

where t_{SU} is the minimum data setup time required at the processor serial data input, t_{CD} is the maximum CLKIN-to-SCLK delay of the MAX121, and t_{SC} is the maximum SCLK-to-SDATA delay for the MAX121.

The second type of interface is intended for applications where the processor supports asynchronous data transfers. The SCLK output of the MAX121 drives the serial clock of the processor, eliminating the t_{CD} term from the above equation and allowing the use of faster clocks. For this case, calculate the maximum serial clock rate with the following formula:

$$f_{CLKIN} = (1/2) \times 1/(t_{SU} + t_{SC})$$

where the variables are as defined above.

Motorola SPI Serial Interface (CPOL = 0, CPHA = 1)

Figure 13 shows the MAX121 and processor interface connections required to support the SPI standard. Figure 12 shows the SPI interface timing diagram. For SPI interfaces, the processor $\overline{SS}$ input should be pulled high, to configure the processor as the master. An I/O port from the processor drives the MAX121 $\overline{CONVST}$ (mode 1) or $\overline{CS}$ (mode 2) low to control the conversion starts. The SCK output of the processor will drive the CLKIN of the MAX121. The MISO I/O of the processor is driven by the SDATA output of the MAX121.

The SPI standard requires that all data transfers occur in blocks of 8 bits, but the MAX121 outputs data in 16-bit blocks. Therefore, two 1-byte read operations are required to receive the full 14 data bits from the MAX121.

A conversion is initiated by driving the processor I/O port low. Next, a write operation must be performed by the processor to activate the serial clock and read the first 8 bits of data from the MAX121.

The MAX121 output data transitions on the rising edge of the clock. The processor reads data on the falling edge of the clock (CPHA = 1). This provides one half clock cycle to satisfy the minimum setup and hold time requirement of the processor data input. The maximum clock rate for SPI interfaces is 2MHz.

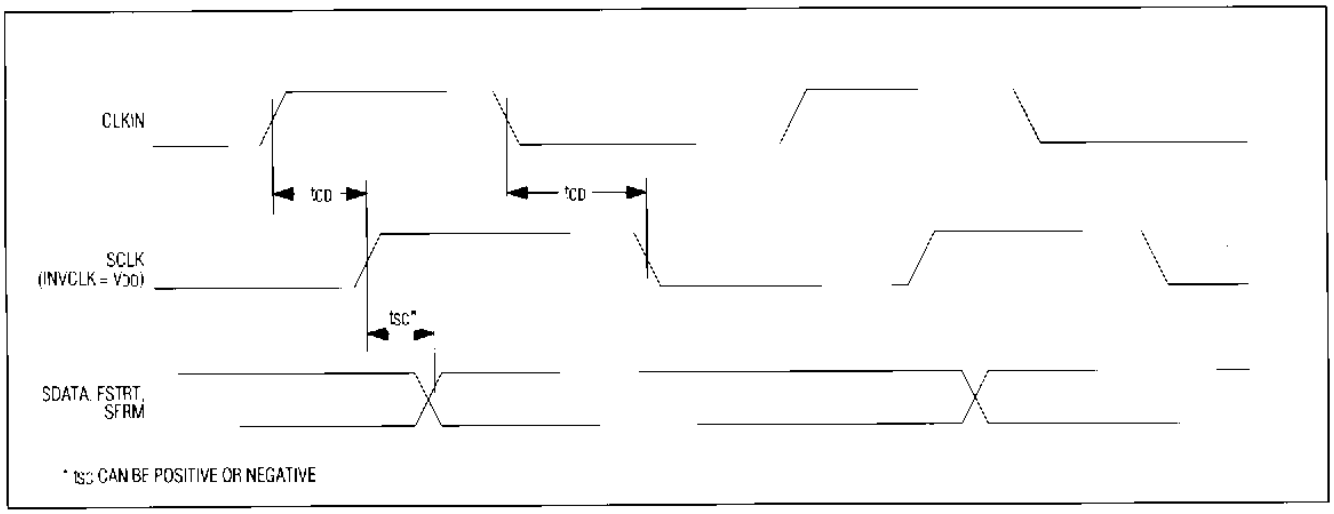

Figure 11. Timing Diagram for Serial Data

The first byte of data read by the processor will consist of a leading zero followed by the 7 MSBs of data. A second write operation should then be initiated to read the second byte of data, which contains the 7 LSBs of conversion data followed by a trailing zero. To minimize errors due to droop of the MAX121 internal T/H, limit the maximum time delay between the conversion start and the end of the second read operation to no more than 160µs.

Motorola QSPI Serial Interface (CPOL = 0, CPHA = 1)

Figure 14 shows the connections required to implement a QSPI interface with the MAX121. The timing diagram for this interface is shown in Figure 15. The QSPI standard is similiar to SPI, with the primary differences as follows:

1) QSPI allows arbitrary length data transfers from 8 to 16 bits, so only one read operation is required to receive the 14 bits of output data from the MAX121.
2) QSPI allows clock rates up to 4MHz, compared to 2MHz with SPI.

ADSP2101 Serial Interface

Figure 16 shows the connections required to interface the MAX121 to Analog Devices' ADSP2101 DSP. Figure 17 is a plot of the timing diagram. The ADSP2101 has a high-speed serial interface with a minimum serial data setup time of 10ns (t_{SCS}) and a minimum data-hold time of 10ns (t_{SCH}). This interface permits operation of the MAX121 at its maximum clock rate of 5.5MHz.

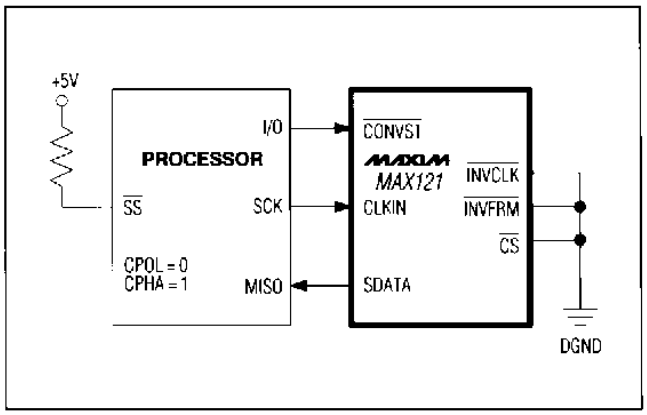

Figure 13. SPI Interface Circuit

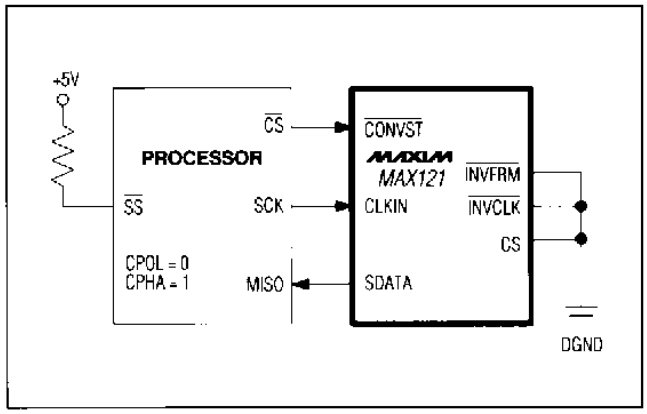

Figure 14. QSPI Interface Circuit

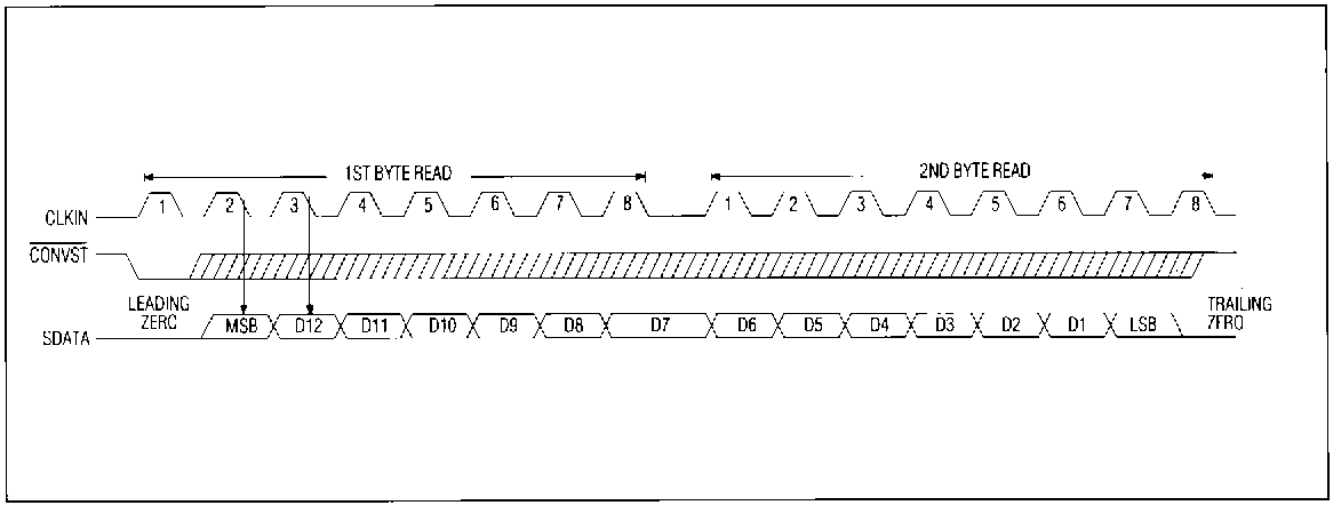

Figure 12. SPI Interface Timing Diagram

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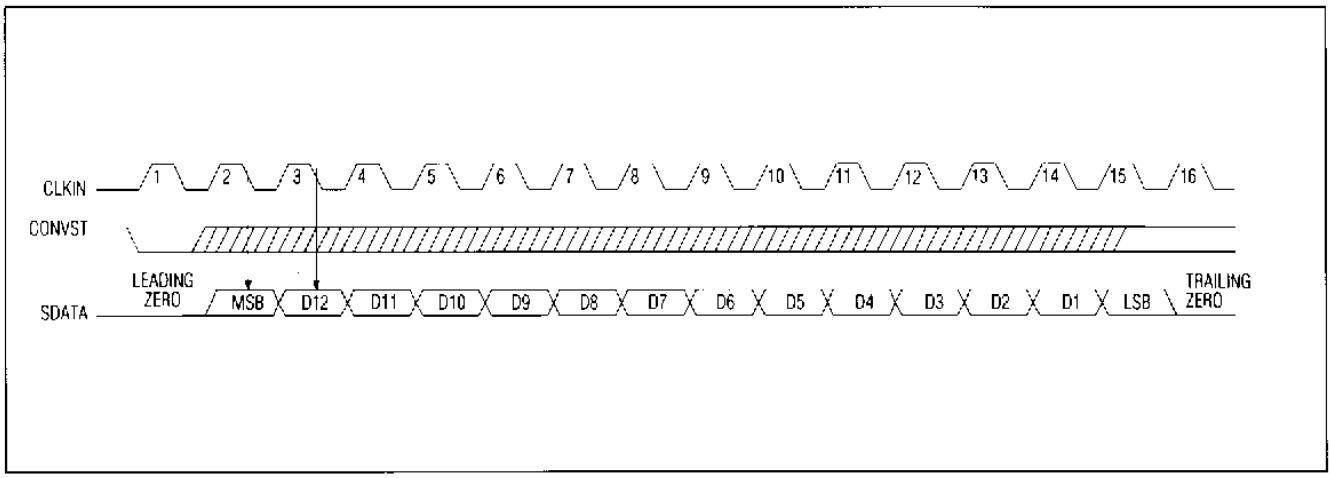


Figure 15. QSPI Interface Timing Diagram

An output port of the ADSP2101 drives the MAX121 CONVST input low to initiate a conversion. The SFRM output of the MAX121 drives the RFS (Receive Frame Synchronization) input to the DSP low to indicate that the MSB has been shifted out of the MAX121 SDATA pin. On the next falling edge on SCLK, the MSB is shifted into the ADSP2101 serial input. Note that the MAX121 $\overline{INVFRM}$ input is grounded to provide the proper phase for the SFRM output.

The SCLK terminal of the ADSP2101 is configured as an input and is driven by the MAX121 SCLK output to clock data into the DSP. The SFRM output remains low for 16 clock cycles, allowing the 14 data bits to be shifted into the ADSP2101, followed by 2 trailing zeros.

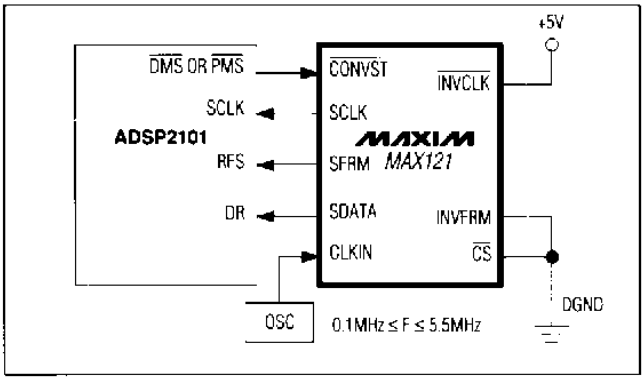


Figure 16. ADSP2101 to MAX121 Interface

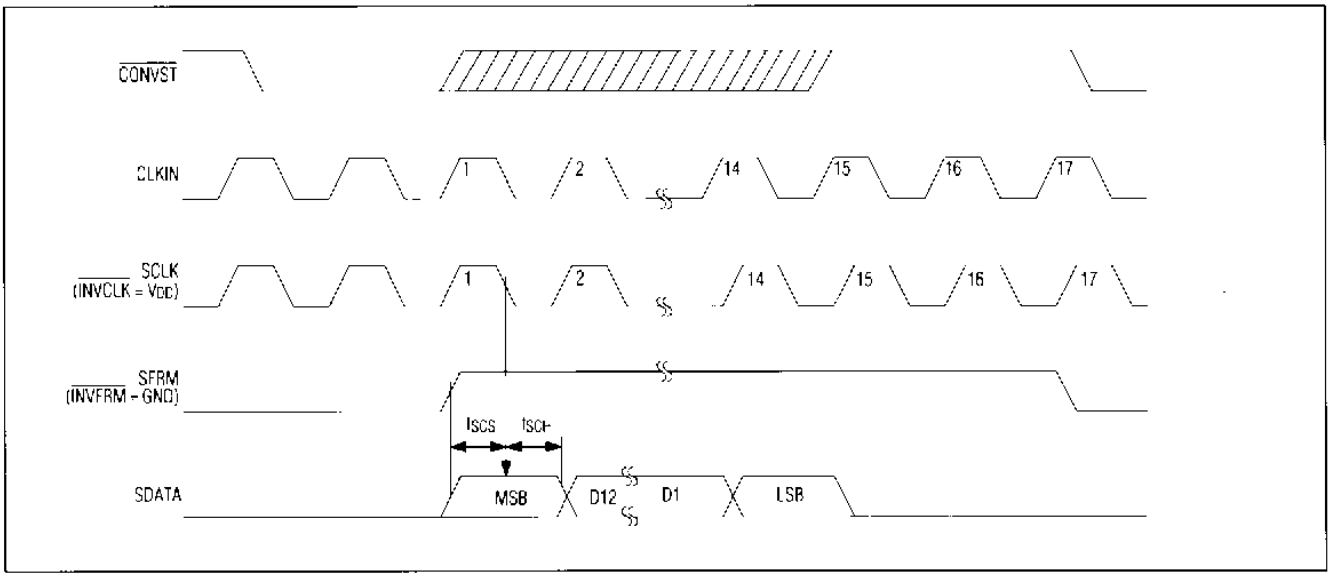


Figure 17. ADSP2101 Interface Timing Diagram

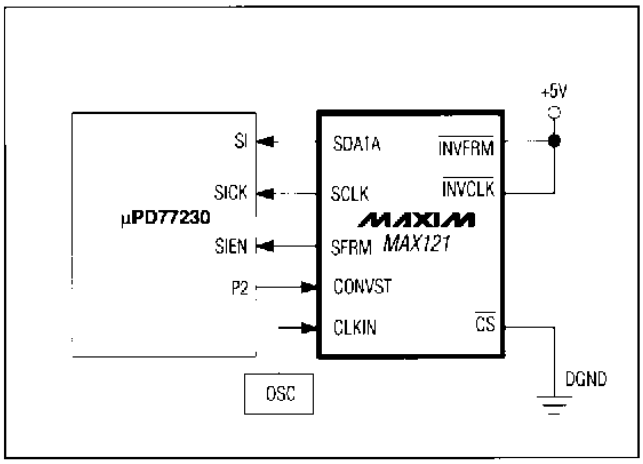


Figure 18. NEC µPD77230 Interface Circuit

NEC µPD77230 Serial Interface

Figure 18 shows the connections required to interface the MAX121 to NEC's µPD77230 DSP without external glue logic. The timing diagram is shown in Figure 19. See the *Maximum Clock Rate for Serial Interface* section to determine the maximum usable clock rate for this interface, substituting t_{SISS} for t_{SU} in the equations. The t_{HSSI} term in the timing diagram is the minimum data-hold time for the µPD77230's serial data input.

An I/O port of the µPD77230 drives the MAX121 $\overline{CONVST}$ pin low to initiate a conversion. The MAX121 SFRM output drives the SIEN (Serial Input Enable) terminal of the DSP low to frame the data. On the next falling edge of SCLK, the MSB is shifted into the SI (Serial Input) pin of the µPD77230. SDATA drives the SI terminal of the DSP. The MSB is followed by the other 13 data bits and two trailing zeros, after which the SFRM output returns high to disable the DSP serial input until the next conversion is initiated.

TMS320 High-Speed Serial Interface

The flexibility of the MAX121 permits the implementation of a variety of interfaces with the Texas Instruments TMS320 DSP. The *TMS320 Simple Serial Interface* section of this data sheet discusses the simplest type of MAX121-to-TMS320 interface, which works with serial clock rates up to 3.2MHz.

This section describes an interface that allows the maximum throughput to be obtained from the MAX121/TMS320 system, by operating the MAX121 at its maximum clock. Figure 20 shows the interconnections required to implement this interface. Figure 21 is the timing diagram for this interface.

The MAX121 CLKIN is driven by an external clock oscillator. The XF0 I/O port of the TMS320 drives the MAX121 CONVST input low to initiate a conversion. CLKR (Receive Clock) of the TMS320 is configured as an input and driven by the MAX121 SCLK output. Data on the MAX121 SDATA output changes state on the rising edge of the clock, while data is latched into the DR input of the TMS320 on the falling edge. This provides one half clock cycle to meet the setup and hold time requirements of the TMS320 DR input. The maximum skew between the MAX121 SCLK and SDATA is ±65ns at +25°C, so one half clock cycle is more than sufficient to guarantee that the setup and hold time requirement is satisfied.

The FSTRT output of the MAX121 drives the FSR input of the TMS320 to frame the data. A falling edge on the FSTRT output indicates that the MSB is ready to be latched. On the next falling clock edge, the MSB is latched into the TMS320. For this interface, the TMS320 is configured to receive a 16-bit word (RLEN = 01 in the TMS320 serial-port global control register) so the 14 bits of data are clocked into the DSP, followed by two trailing zeros.

TMS320 Simple Serial Interface

Figure 22 shows an application circuit using the simplest interface between the MAX121 and the TMS320. The timing diagram for this circuit is shown in Figure 23.

In this circuit, the CLKR port of the TMS320 is configured as a clock output and drives the CLKIN of the MAX121. The MAX121 output changes state on the rising edge of the CLKIN, while the data is latched into the DR port of the TMS320 on the falling edge. The XF1 I/O port of the TMS320 drives the MAX121 $\overline{CONVST}$ input low to initiate a conversion. The FSTRT output of the MAX121 drives the FSR input of the TMS320 to frame the data. A falling edge on the FSTRT output indicates that the MSB is ready to be latched. On the next falling clock edge, the MSB is latched into the TMS320. For this interface, the TMS320 is configured to receive a 16-bit word (RLEN = 01 in the TMS320 serial-port global control register) so the 14 bits of data are clocked into the DSP, followed by two trailing zeros. At T_A = +25°C, the clock frequency is limited to approximately 3.2MHz with this interface, due to the CLKIN-to-SDATA maximum delay of 130ns and the 25ns setup and hold time requirement for the TMS320.

308ksps ADC with DSP Interface and 78dB SINAD

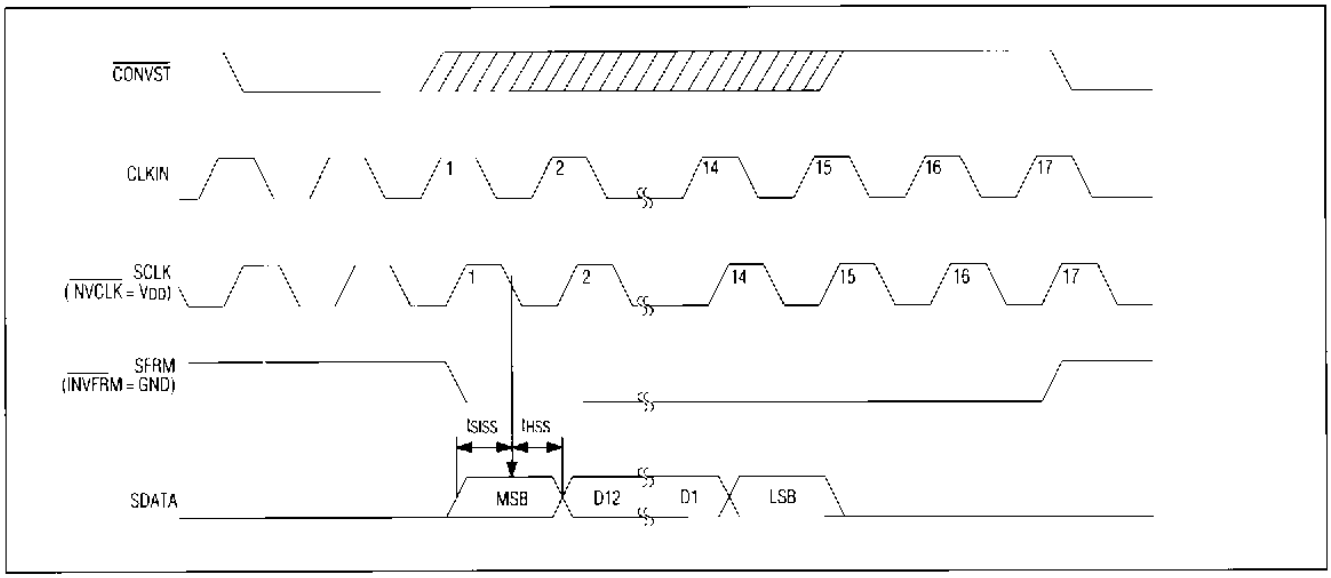


Figure 19. NEC µPD77230 Interface Timing Diagram

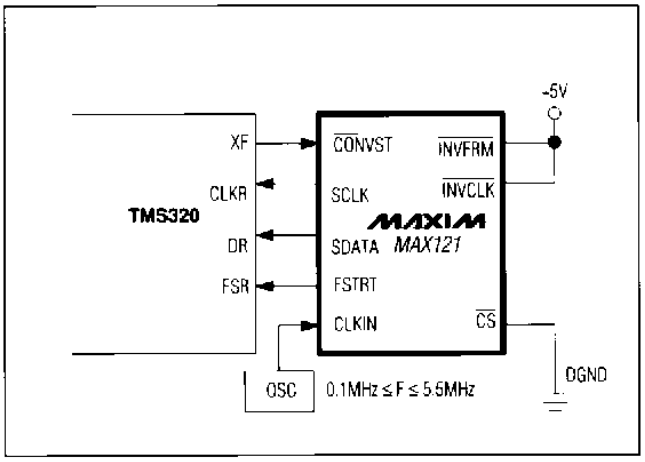


Figure 20. TMS320 High-Speed Serial-Interface Circuit

Figure 24 is a listing of a short program written in the TMS320 assembly language that initiates conversions in the TMS320 and ships the output data back to the host PC. The C language program listed in Figure 25 displays the results of every 30,000th conversion on the PC screen, along with the min and max values for all conversions performed during one operating sequence.

Digital Bus/Clock Noise

If the clock is active when the T/H is sampling the input signal, errors can be caused by coupling from the CLKIN pin to the analog input. If this is a problem, the clock should be disabled for one clock cycle while the T/H is placed into hold mode. In mode 1, the clock should be disabled (CLKIN = DGND) for one cycle while $\overline{CONVST}$ is pulsed low. In mode 2, the clock should be disabled (CLKIN = DGND) for one clock cycle while $\overline{CS}$ is driven low. The clock should be re-activated on the first cycle after the conversion is started ($\overline{CONVST}$ or $\overline{CS}$ pulsed low).

Layout, Grounding and Bypassing

For best system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be tied together at the low-impedance power-supply source, as shown in Figure 26.

The board layout should ensure that digital and analog signal lines are kept separate, as much as possible. Take care not to run analog and digital (especially clock) lines parallel to one another.

The high-speed comparator in the ADC is sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. Bypass these supplies to the analog-ground plane with 0.1µF and 10µF bypass capacitors. Keep capacitor leads at a minimum length for best supply-noise rejection. If the +5V power supply is very noisy, a 5Ω resistor can be connected, as shown in Figure 26, to filter this noise. Figure 27 shows the negative power supply (V_{SS}) rejection vs. frequency. Figure 28 shows the positive power-supply (V_{DD}) rejection vs. frequency, with and without the optional 5Ω resistor.

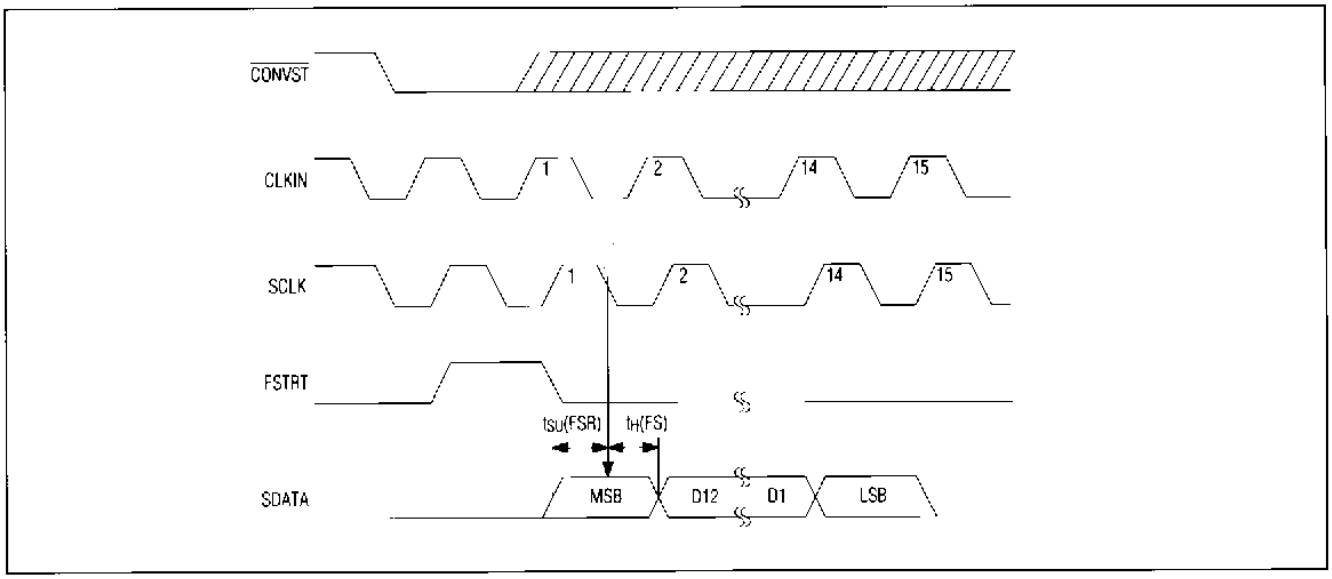


Figure 21 TMS320 High-Speed Serial-Interface Timing Diagram

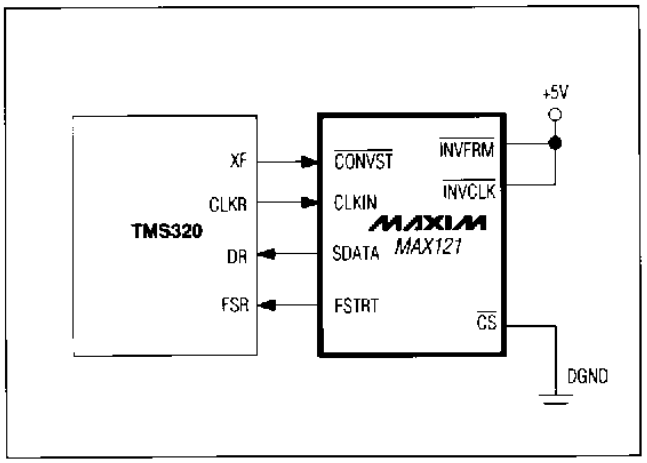


Figure 22. TMS320 Simple Serial-Interface Circuit

Dynamic Performance

High-speed sampling capability and 308kHz throughput make the MAX121 ideal for wideband signal processing. To support these and other related applications, FFT (Fast Fourier Transform) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sinewave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content. Conversion errors are then seen as spectral elements outside of the fundamental input frequency.

A/D converters have traditionally been evaluated by specifications such as Zero and Full-Scale Error, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

The signal-to-noise plus distortion ratio (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other ADC output signals. The output band is limited to frequencies above DC and below one-half the ADC sample (conversion) rate.

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution: SINAD = (6.02N + 1.76)dB, where N is the number of bits of resolution. A perfect 14-bit ADC can, therefore, do no better than 86dB. An FFT plot of the output shows the output level in various spectral bands. Figure 29 shows the result of sampling a pure 50kHz sinusoid at a 300kHz rate with the MAX121.

By transposing the equation that converts resolution to SINAD, we can, from the measured SINAD, determine the effective resolution (effective number of bits) that the ADC provides: N = (SINAD - 1.76)/6.02. Figure 30 shows the effective number of bits as a function of the input frequency for the MAX121.

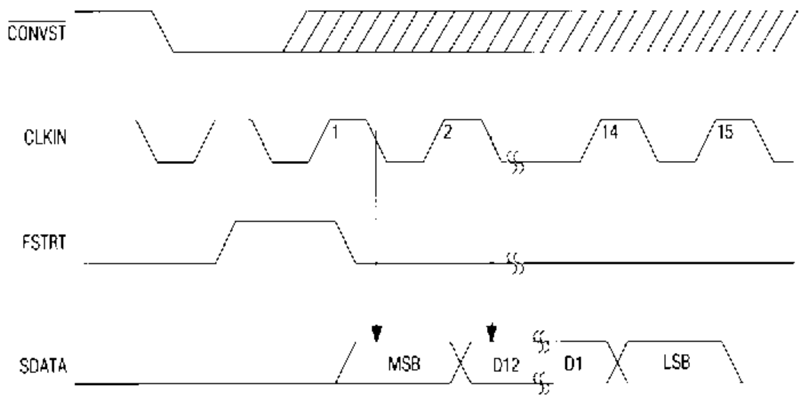


Figure 23. TMS320 Simple Serial-Interface Timing Diagram

```
;#;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
;
;
;;
;;    Project:  Maxim 121 to TI TMS320C30 Application Note
;;
;;    File:     maximti.asm
;;
;;    Purpose:  This file contains the code that is loaded onto the
;;              TMS320C30 Evaluation Module (EVM).  It's purpose is to
;;              collect digitized samples from the Maxim 121 ADC at a
;;              regular rate and ship those values to the PC.
;;
;;    Tabstops: 8
;;
;;
;;
;;    $Log:$
;;
;;    Edit History:
;;
;;      Date            By      Description
;;      ----            --      -----------
;;      09/24/92        KHB     Initial Creation
;;
;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;#;;
```

Figure 24. TMS320 Assembly Language Program to Control Conversions Using the TMS320 Simple Serial-Interface

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;Publics;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

        .global maxim
        .global wait_sample
        .global wait_loop
        .global next_sample

        .global IOF_MASK_AMASK
        .global IOF_SET_XF1
        .global IOR_RESET_XF1
        .global CTRL
        .global SERGLOB1
        .global SERPRTX1
        .global SERPRTR1
        .global SERTIM1
        .global SERTIM1VAL
        .global HOST_DATA



;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;Data;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

        .data

IOF_AMASK       .word   000000EH        ; Preserve XF0 settings
IOF_SET_XF1     .word   0000060H        ; Set XF1 as output high
IOF_RESET_XF1   .word   0000020H        ; Set XF1 as output low

CTRL            .word   0808000H        ; Pointer to peripheral-bus memory map

SERGLOB1        .word   8120280H        ; Setup serial 1 global control (80)
                                        ;  Use internal receive clock
                                        ;  FSR active during entire transfer
                                        ;  16-bit rcv data length
                                        ;  FSR active low
                                        ;  Take rcvr out of reset
SERPRTX1        .word   0000000H        ; Setup serial 1 xmt port control (82)
SERPRTR1        .word   0000111H        ; Setup serial 1 rcv port control (83)
                                        ;  CLKR1 = serial port pin
                                        ;  DR1   = serial port pin
                                        ;  FSR1  = serial port pin
SERTIM1         .word   00003C0H        ; Setup serial 1 timer control (84)
                                        ;  Start rcv timer, 50% duty cycle,
                                        ;  internal clk src = 1/2 CLKOUT is
                                        ;   used to increment rcvr timer.
SERTIM1VAL      .word   00020000H       ; Timer period values RX and TX
                                        ;  Rcvr timer is high order 16-bits
                                        ;  (CLKOUT/2)/2 =
                                        ;   1.875Mhz CLKR1->MAX121 CLKIN

HOST_DATA       .word   00804000H       ; Memory address of host data port
```

Figure 24. TMS320 Assembly Language Program to Control Conversions Using the TMS320 Simple Serial-Interface (continued)

308ksps ADC with DSP Interface and 78dB SINAD

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;Functions;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

        .text

maxim
;
; Initialization Code
;
        LDI     0,ST            ; Initialize status register
        LDIU    128,DP          ; Initialize data page register
        LDI     0985CH,SP       ; Initialize stack pointer

        LDI     IOF,R1          ; Read in I/O Flags register to R1
        AND     @IOF_AMASK,R1   ; Remove current XF1 bits, preserve XF0 settings
        OR      @IOF_SET_XF1,R1 ; Set XF1 (CONVST*) Inactive (high)
        LDI     R1,IOF          ; Make it so!

        LDI     @CTRL,AR0       ; Load AR0 w/ptr to control reg base
        LDI     @HOST_DATA,AR1  ; Load AR1 w/host interface address

        LDI     @SERTIM1VAL,R0
        STI     R0,*+AR0(86)    ; Setup serial ch1 timer period value
        LDI     @SERGLOB1,R0
        STI     R0,*+AR0(80)    ; Setup serial ch1 global register
        LDI     @SERPRTX1,R0
        STI     R0,*+AR0(82)    ; Setup serial ch1 xmt control register
        LDI     @SERPRTR1,R0
        STI     R0,*+AR0(83)    ; Setup serial ch1 rcv control register
        LDI     @SERTIM1,R0
        STI     R0,*+AR0(84)    ; Setup serial ch1 timer register



next_sample:
;
; Start Conversion -->     ____|‾‾|_____        (CONVST*)
;
        LDI     IOF,R1          ; Read in I/O Flags register to R1
        AND     @IOF_AMASK,R1   ; Remove current XF1 bits, preserve XF0 settings
        OR      @IOF_SET_XF1,R1 ; Set XF1 (CONVST*) Inactive (high)
        LDI     R1,IOF          ; Make it so!

        AND     @IOF_AMASK,R1           ; Remove current XF1 bits, preserve XF0
        OR      @IOF_RESET_XF1,R1       ; Set XF1 (CONVST*) Active (low)
        LDI     R1,IOF                  ; Make it so!
```

Figure 24. TMS320 Assembly Language Program to Control Conversions Using the TMS320 Simple Serial-Interface (continued)

```
wait_sample:
;
; Wait for completion of conversion
;       MAX121 SFRM Active Signals TMS320 FSR1 that data transfer
;       is ready to start.
;
        LDI     *+AR0(80),R2    ; Read in Serial Ch 1 global register
        AND     01H,R2          ; Check for RRDY Active (1)
                                ; RRDY goes active when 16-bits have been rcvd
        BZ      wait_sample     ; Keep waiting if not ready

        LDI     *+AR0(92),R3    ; Ready, read value from Data Receive register
        STI     R3,*+AR1(0)     ; Send out value to host

;
; Arbitrary wait time until start of next convert.
;
        LDI     100,R0
wait_loop:
        SUBI    1,R0
        BNZ     wait_loop       ; Keep waiting until R0 decremented to zero

        BR      @next_sample    ; Go start next convert

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                .end
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
```

Figure 24. TMS320 Assembly Language Program to Control Conversions Using the TMS320 Simple Serial-Interface (continued)

308ksps ADC with DSP Interface and 78dB SINAD

```
/*#*************************************************************************
**
**
**
**
**    Project:  Maxim 121 to TI TMS320C30 Application Note
**
**    File:     readdata.c
**
**    Purpose:  This file contains a PC based program used to read data
**              from the TMS320C30 Evaluation Module (EVM) and display
**              the data on the PC screen.
**              This file may be compiled with either the Microsoft C
**              Compiler or Borland C++ Compiler.
**
**    Tabstops: 4
**
**
**
**    $Log:$
**
**    Edit History:
**
**      Date        By      Description
**      ----        --      -----------
**      09/24/92    KHB     Initial Creation
**
**
*************************************************************************#*/

#include <stdio.h>      /* for printf() */
#include <conio.h>      /* for kbhit(), getch(), and inpw() */

#define VERSION_STAMP   1

void
main(void)
{
    int x;
    int value;
    int quit = 0;
    int min = 32767;
    int max = -32768;

    printf("\n");
    printf("TMS320 EVM Data Display Program - Version %d\n", VERSION_STAMP);

    printf("m = reset Max/Min values, ESC to quit\n\n");
```

Figure 25. C Language Program to Log Data From MAX121 Conversions

```
    while(!quit)
    {
        if(kbhit())
        {
            switch(getch())
            {
                case 'm':           /* Clear Max/Min Storage Variables */
                    max = -32768;
                    min = 32767;
                    break;
                case 'q':           /* Quit Program */
                case 0x1B:
                    quit = 1;
                    break;
            }
        }
        for(x=0; x<30000; x++)
        {
            /* Gather samples as fast as possible and update Max/Min */
            /* Only output every 30,000th sample.  The 30,000 has no */
            /*  specific origin other than the display updated at a  */
            /*  comfortable rate.                                    */
            value = inpw(0x0240+0x0808);    /* EVM Data Port */
            value >>= 2;                /* Shift from 16-bit back to 14-bit */

            /* Update Max/Min */
            if(value > max)
                max = value;
            else if(value < min)
                min = value;
        }
        /* Output the latest sample in decimal and hex along with Max/Min */
        printf("  %06d  %04Xh  min:%06d  max:%06d  \r", value, value, min, max);
    }

    /* Exit */
    printf("\n\n");
    return;
}
```

Figure 25. C Language Program to Log Data From MAX121 Conversions (continued)

308ksps ADC with DSP Interface and 78dB SINAD

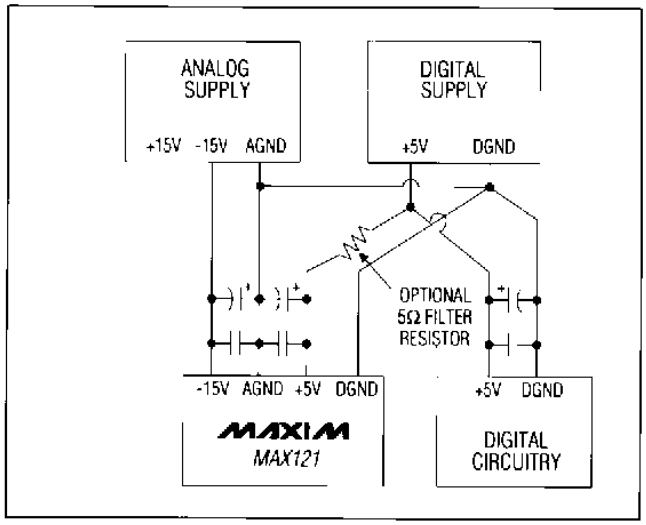


Figure 26. Power-Supply Grounding

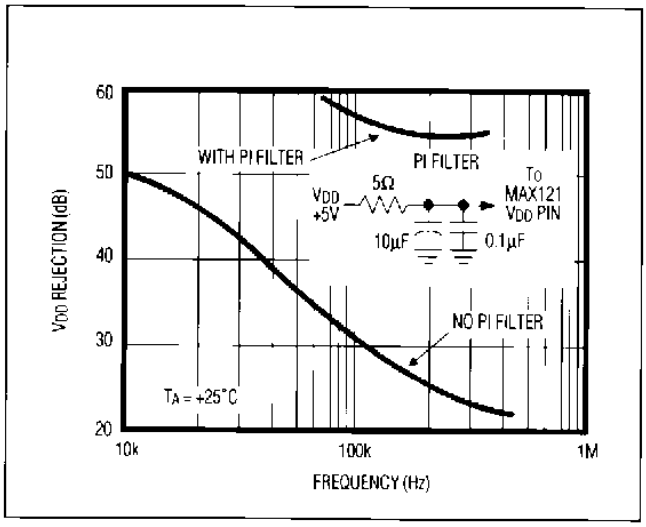


Figure 28. V_{DD} Power-Supply Rejection vs. Frequency

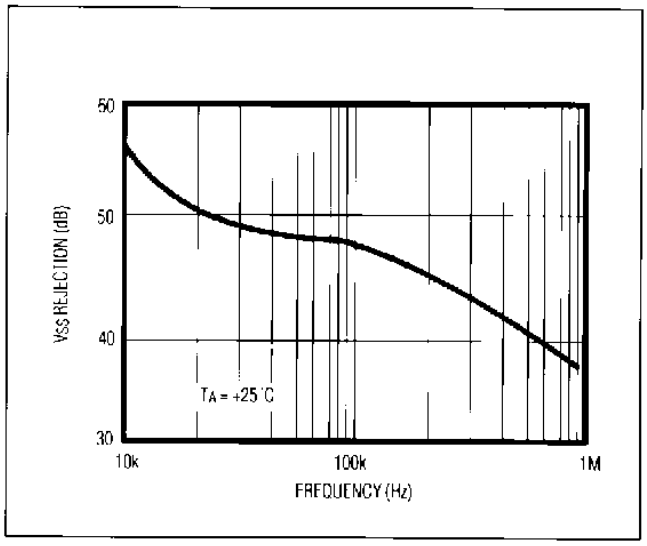


Figure 27. V_{SS} Power-Supply Rejection vs. Frequency

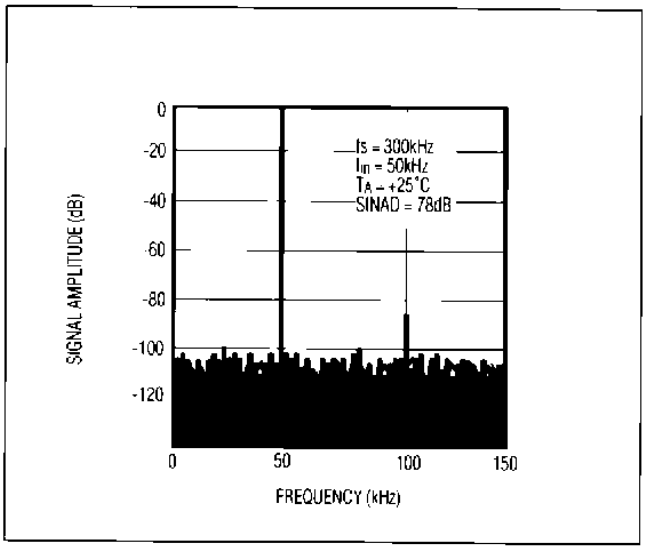


Figure 29. MAX121 FFT Plot

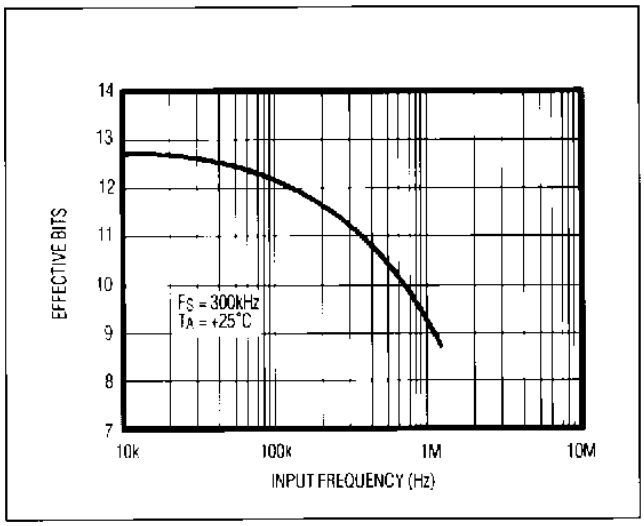


Figure 30. Effective Bits vs. Input Frequency

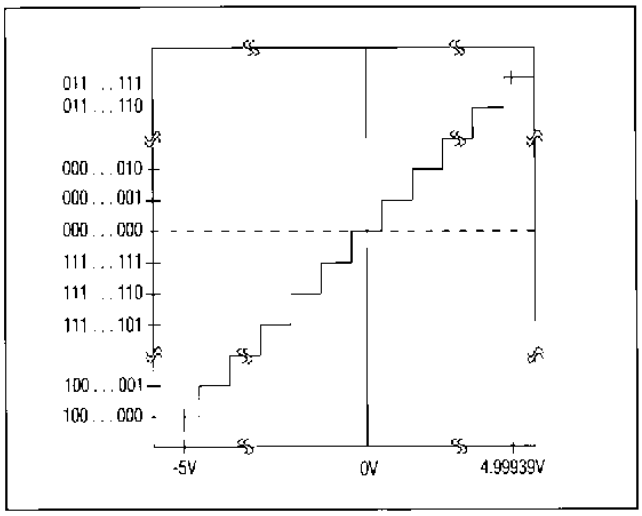


Figure 31. Bipolar Transfer Function

Total Harmonic Distortion

If a pure sine wave is sampled by an ADC at greater than the Nyquist frequency, the nonlinearities in the ADC's transfer function create harmonics of the input frequency present in the sampled output data.

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all the harmonics (in the frequency band above DC and below one-half the sample rate, but not including the DC component) to the RMS amplitude of the fundamental frequency. This is expressed as follows:

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_N^2}}{V_1}$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics. The THD specification in the *Electrical Characteristics* includes the 2nd through 5th harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Transfer Function

The plot in Figure 31 graphs the bipolar input/output transfer function for the MAX121. Code transitions occur halfway between successive integer LSB values. Output coding is two's-complement binary, with 1 LSB = 610µV (10V/16384).

308ksps ADC with DSP Interface and 78dB SINAD

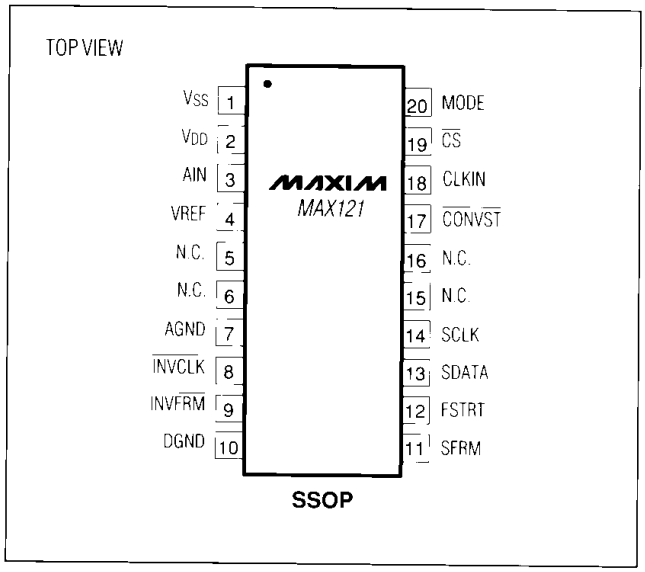
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX121EPE	-40°C to +85°C	16 Plastic DIP
MAX121EWE	-40°C to +85°C	16 Wide SO
MAX121EAP	-40°C to +85°C	20 SSOP**
MAX121MJE	-55°C to +125°C	16 CERDIP***

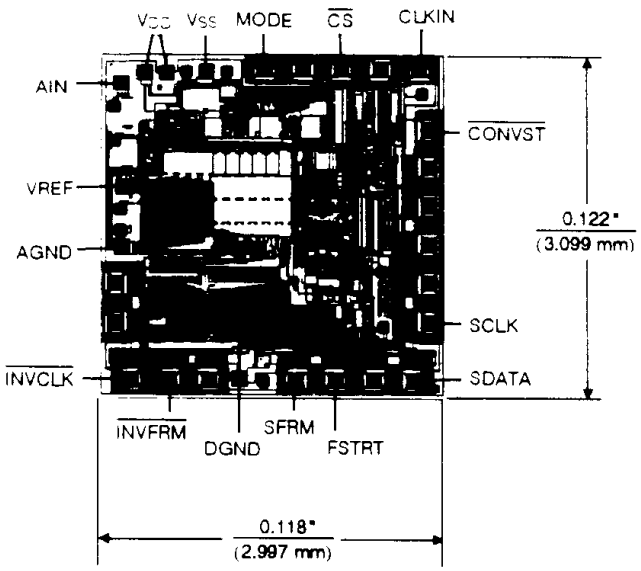
PART	TEMP. RANGE	BOARD TYPE
MAX121EVKIT-DIP	0°C to +70°C	Through-Hole

*** 20-pin SSOP is 50% smaller than 16-pin SOIC.*
**** Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations (continued)



Chip Topography



SUBSTRATE CONNECTED TO V_{DD};
TRANSISTOR COUNT: 1;920.