DS80C310
High-Speed Micro

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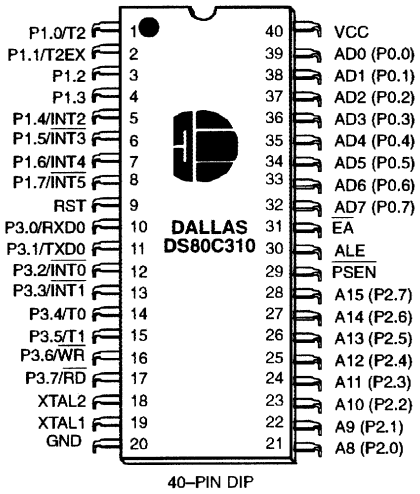
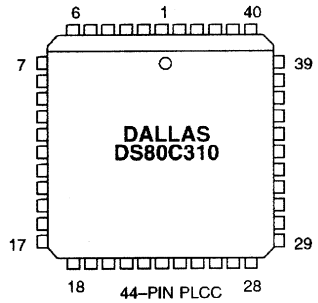
FEATURES

- 80C32-compatible
  - 8051 pin- and instruction set-compatible
  - Full duplex serial port
  - Three 16-bit timer/counters
  - 256 bytes scratchpad RAM
  - Multiplexed address/data bus
  - Addresses 64 kB ROM and 64 kB RAM
- High-Speed Architecture
  - 4 clocks/machine cycle (8051 = 12)
  - Runs DC to 33 MHz clock rates
  - Single-cycle instruction in 121 ns
  - Dual data pointer
  - Optional variable length MOVX to access fast/slow RAM /peripherals
- 10 total interrupt sources with 6 external
- Internal power-on reset circuit
- Upwardly compatible with the DS80C320
- Available in 40-pin PDIP, 44-pin PLCC, and 44-pin TQFP

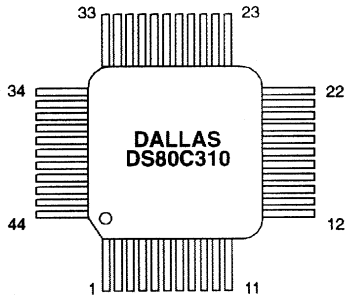
PACKAGE OUTLINE



40–PIN DIP



44–PIN PLCC



44–PIN TQFP

DESCRIPTION

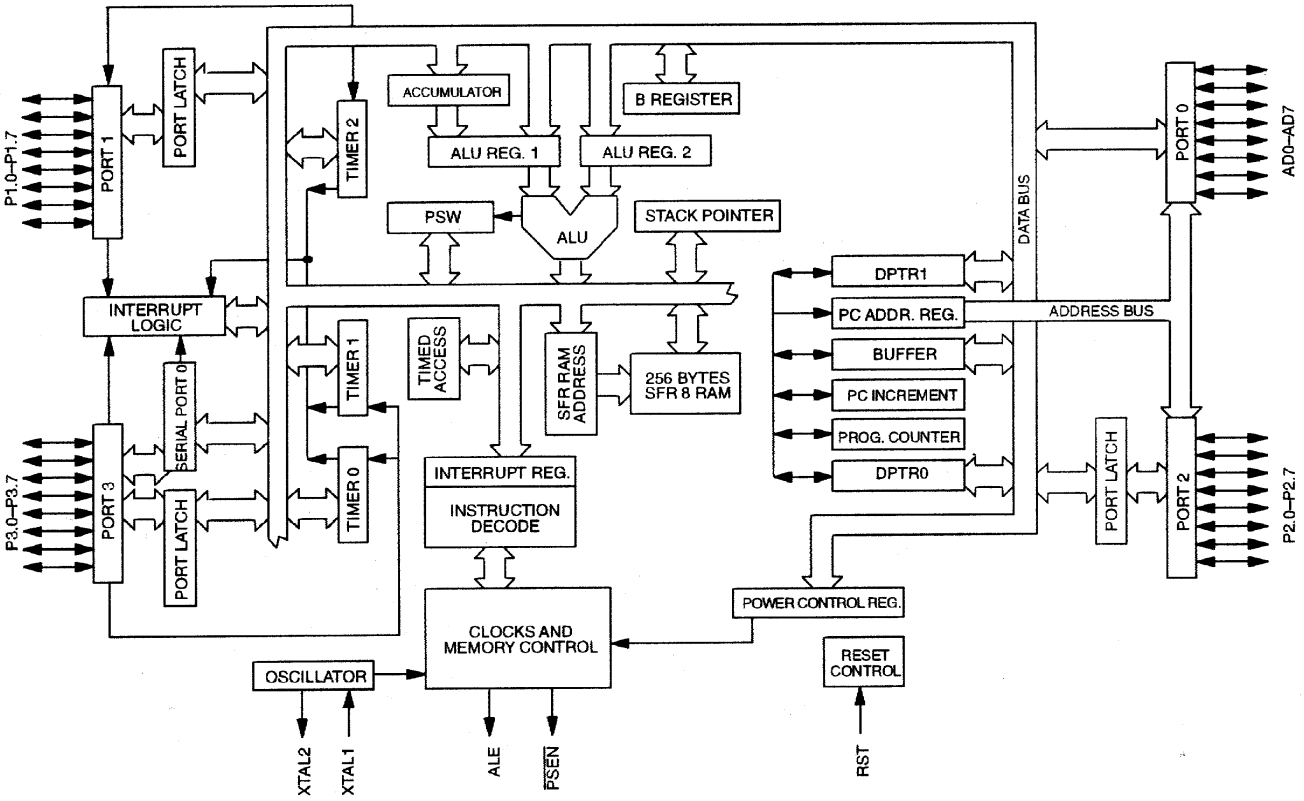
The DS80C310 is a fast 80C31/80C32-compatible microcontroller. It features a redesigned processor core without wasted clock and memory cycles. As a result, it executes every 8051 instruction between 1.5 and 3 times faster than the original architecture for the same crystal speed. Typical applications will see a speed improvement of 2.5 times using the same code and the same crystal. The DS80C310 offers a maximum crystal speed of 33 MHz, resulting in apparent execution speeds of 82.5 MHz (approximately 2.5X).

The DS80C310 is pin-compatible with the standard 80C32 and includes standard resources such as three timer/counters, 256 bytes of RAM, and a serial port. It also provides dual data pointers (DPTRs) to speed block data memory moves. It also can adjust the speed of MOVX data memory access between two and nine machine cycles for flexibility in selecting external memory and peripherals. The DS80C310 offers upward compatibility with the DS80C320.

ORDERING INFORMATION:

PART NUMBER	PACKAGE	MAX. CLOCK SPEED	TEMPERATURE RANGE
DS80C310-MCG	40-pin plastic DIP	25 MHz	0°C to 70°C
DS80C310-QCG	44-pin PLCC	25 MHz	0°C to 70°C
DS80C310-ECG	44-pin TQFP	25 MHz	0°C to 70°C
DS80C310-MCL	40-pin plastic DIP	33 MHz	0°C to 70°C
DS80C310-QCL	44-pin PLCC	33 MHz	0°C to 70°C
DS80C310-ECL	44-pin TQFP	33 MHz	0°C to 70°C

DS80C310 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

DIP	PLCC	TQFP	SIGNAL NAME	DESCRIPTION
40	44	38	V_{CC}	**V_{CC}** -+5V.
20	22,23 1	16,17, 39	GND	**GND**- Digital circuit ground.
9	10	4	RST	**RST - Input**. The RST input pin contains a Schmitt voltage input to recognize external active high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external Reset sources.
18 19	20 21	14 15	XTAL2 XTAL1	**XTAL1, XTAL2** - The crystal oscillator pins XTAL1 and XTAL2 provide support for parallel resonant, AT cut crystals. XTAL1 acts also as an input in the event that an external clock source is used in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
29	32	26	$\overline{\text{PSEN}}$	**$\overline{\text{PSEN}}$ - Output**. The Program Store Enable output. This signal is commonly connected to external ROM memory as a chip enable. $\overline{\text{PSEN}}$ is active low. $\overline{\text{PSEN}}$ is driven high when data memory (RAM) is being accessed through the bus and during a reset condition.
30	33	27	ALE	**ALE - Output**. The Address Latch Enable output functions as clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch.ALE is forced high when the DS80C310 is in a Reset condition.
39 38 37 36 35 34 33 32	43 42 41 40 39 38 37 36	37 36 35 34 33 32 31 30	AD0 (P0.0) AD1 (P0.1) AD2 (P0.2) AD3 (P0.3) AD4 (P0.4) AD5 (P0.5) AD6 (P0.6) AD7 (P0.7)	**AD0-7 (Port 0) - I/O**. Port 0 is the multiplexed address/data bus. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bidirectional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. Port 0 has no true port latch and can not be written directly by software. The reset condition of Port 0 is high.
1-8	2-9	40-44 1-3	P1.0-P1.7	**Port 1 - I/O**. Port 1 functions as both an 8-bit bidirectional I/O port and an alternate functional interface for Timer 2 I/O and new External Interrupts. The reset condition of Port 1 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS80C310 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes the output high (and input) state. The alternate modes of Port 1 are outlined as follows:

DIP	PLCC	TQFP	SIGNAL NAME	DESCRIPTION
				Port Alternate Function
1	2	40		P1.0 T2 External I/O for Timer/Counter 2
2	3	41		P1.1 T2EX Timer/Counter 2 Capture/Reload Trigger
3	4	42		P1.2 none (DS80C320 has a serial port RXD)
4	5	43		P1.3 none (DS80C320 has a serial port TXD)
5	6	44		P1.4 INT2 External Interrupt 2 (Positive Edge Detect)
6	7	1		P1.5 $\overline{\text{INT3}}$ External Interrupt 3 (Negative Edge Detect)
7	8	2		P1.6 INT4 External Interrupt 4 (Positive Edge Detect)
8	9	3		P1.7 $\overline{\text{INT5}}$ External Interrupt 5 (Negative Edge Detect)
21	24	18	A8 (P2.0)	**A8-15 (Port 2) -Output**. Port 2 serves as the MSB for external addressing. P2.7 is A15 and P2.0 is A8. The DS80C310 will automatically place the MSB of an address on P2 for external ROM and RAM access. Although Port 2 can be accessed like an ordinary I/O port, the value stored on the Port 2 latch will never be seen on the pins (due to memory access). Therefore writing to Port 2 in software is only useful for the instructions MOVX A, @ Ri or MOVX @ Ri, A. These instructions use the Port 2 internal latch to supply the external address MSB; the Port 2 latch value will be supplied as the address information.
22	25	19	A9 (P2.1)	
23	26	20	A10(P2.2)	
24	27	21	A11(P2.3)	
25	28	22	A12(P2.4)	
26	29	23	A13 P2.5)	
27	30	24	A14(P2.6)	
28	31	25	A15(P2.7)	
10-17	11, 13-19	5,7-13	P3.0-3.7	**Port 3 - I/O.** Port 3 functions as both an 8-bit bidirectional I/O port and an alternate functional interface for external Interrupts, Serial Port 0, Timer 0 and 1 Inputs, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. The reset condition of Port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS80C310 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes both the output high and input state. The alternate modes of Port 3 are outlined below.
				Port Alternate Mode
10	11	5		P3.0 RXD0 Serial Port 0 Input
11	13	7		P3.1 TXD0 Serial Port 0 Output
12	14	8		P3.2 $\overline{\text{INT0}}$ External Interrupt 0
13	15	9		P3.3 $\overline{\text{INT1}}$ External Interrupt 1
14	16	10		P3.4 T0 Timer 0 External Input
15	17	11		P3.5 T1 Timer 1 External Input
16	18	12		P3.6 $\overline{\text{WR}}$ External Data Memory Write Strobe
17	19	13		P3.7 $\overline{\text{RD}}$ External Data Memory Read Strobe
31	35	29	$\overline{\text{EA}}$	**$\overline{\text{EA}}$ - Input.** This pin must be connected to ground for proper operation.
-	12 34	6 28	NC	**NC - Reserved**. These pins should not be connected. They are reserved for use with future devices in this family.

COMPATIBILITY

The DS80C310 is a fully static CMOS 8051-compatible microcontroller designed for high performance. In most cases the DS80C310 can drop into an existing socket for the 80C31 or 80C32 to improve the operation significantly. In general, software written for existing 8051-based systems works without modification on the DS80C310. The exception is critical timing since the High-Speed Micro performs its instructions much faster than the original for any given crystal selection. The DS80C310 runs the standard 8051 family instruction set and is pin compatible with DIP, PLCC or TQFP packages. The DS80C310 is a streamlined version of the DS80C320. It maintains upward compatibility but has fewer peripherals.

The DS80C310 provides three 16-bit timer/counters, a full-duplex serial port, and 256 bytes of direct RAM. I/O ports have the same operation as a standard 8051 product. Timers will default to a 12-clock per cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new 4 clocks per cycle if desired.

The DS80C310 provides several new hardware functions that are controlled by Special Function registers. A summary of the Special Function Registers is provided in Table 2.

PERFORMANCE OVERVIEW

The DS80C310 features a high-speed 8051 compatible core. Higher speed comes not just from increasing the clock frequency, but from a newer, more efficient design.

This updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS80C310, the same machine cycle takes four clocks. Thus the fastest instruction, 1 machine cycle, executes three times faster for the same crystal frequency. Note that these are identical instructions. The majority of instructions on the DS80C310 will see the full 3 to 1 speed improvement. Some instructions will get between 1.5 and 2.4 to 1 improvement. All instructions are faster than the original 8051.

The numerical average of all opcodes gives approximately a 2.5 to 1 speed improvement. Improvement of individual programs will depend on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3 to 1 improved opcodes makes dramatic speed improvements likely for any code. These architecture improvements and 0.8 µm CMOS produce a peak instruction cycle in 121 ns (8.25 MIPs). The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions in the DS80C310 perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real time events, the timing of software loops can be calculated using a table in the High-Speed Microcontroller User's Guide. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture the "MOVX A, @ DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of

time. In the DS80C310, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the “MOV direct, direct” uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS80C310 usually uses one instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the High-Speed Microcontroller User’s Guide for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS80C310. The High-Speed Microcontroller User's Guide describes all SFRs. Functions that are not part of the standard 80C32 are in bold.

SPECIAL FUNCTION REGISTERS Table 2

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
SP									
DPL									
DPH									
DPL1									
DPH1									
DPS	0	0	0	0	0	0	0	SEL	
PCON	SMOD	SM0D0	-	-	GF1	GF0	STOP	IDLE	
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	
TL0									
TL1									
TH0									
TH1									
CKCON	**-**	**-**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	
EXIF	**IE5**	**IE4**	**IE3**	**IE2**	-	-	-	-	
SCON	SMO/FE	SM1	SM2	REN	TB8	RB8	TI	RI	
SBUF									
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	
IE	EA	-	ET2	ES0	ET1	EX1	ET0	EX0	
SADDR0									
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	
IP	-	-	PT2	PSO	PT1	PX1	PT0	PX0	
SADEN0									
STATUS	0	HIP	LIP	1	1	1	1	1	
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	
T2MOD	-	-	-	-	-	-	T2OE	DCEN	
RCAP2L									
RCAP2H									
TL2									
TH2									
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	
WDCON	-	**POR**	-	-	-	-	-	-	
ACC									
EIE	-	-	-	-	**EX5**	**EX4**	**EX3**	**EX2**	
B									
EIP	-	-	-	-	**PX5**	**PX4**	**PX3**	**PX2**	

MEMORY ACCESS

The DS80C310 contains no on-chip ROM, and 256 bytes of scratchpad RAM. Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. Timing diagrams are provided in the Electrical Specifications. Program memory (ROM) is accessed at a fixed rate determined by the crystal frequency and the actual instructions. As mentioned above, an instruction cycle requires four clocks. Data memory (RAM) is accessed according to a variable speed MOVX instruction as described below.

STRETCH MEMORY CYCLE

The DS80C310 allows the application software to adjust the speed of data memory access. The micro is capable of performing the MOVX in as few as two instruction cycles. However, this value can be stretched as needed so that both fast memory and slow memory or peripherals can be accessed with no glue logic. Even in highspeed systems, it may not be necessary or desirable to perform data memory access at full speed. In addition, there are a variety of memory mapped peripherals such as LCD displays or UARTs that are not fast.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. This allows the user to select a stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to a one resulting in a three-cycle MOVX. Therefore, RAM access will not be performed at full speed. This is a convenience to existing designs that may not have fast RAM in place. When maximum speed is desired, the software should select a Stretch value of 0. When using very slow RAM or peripherals, a larger stretch value can be selected. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. This results in a wider read/write strobe allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is shown in the Electrical Specifications. Note that full speed access is not the reset default case. Table 3 shows the resulting strobe widths for each Stretch value. The memory stretch is implemented using the Clock Control Special Function Register at SFR location 8Eh. The stretch value is selected using bits CKCON.2-0. In the table, these bits are referred to as M2 through M0. The first stretch (default) allows the use of common 120 ns or 150 ns RAMs without dramatically lengthening the memory access.

DATA MEMORY CYCLE STRETCH VALUES Table 3

CKCON.2-0				RD OR WR STROBE	STROBE WIDTH TIME	
M2	M1	M0	MEMORY CYCLES	WIDTH IN CLOCKS	@ 25 MHz	@ 33 MHz
0	0	0	2	2	80 ns	60ns
0	0	1	3(default)	4	160 ns	121ns
0	1	0	4	8	320 ns	242ns
0	1	1	5	12	480 ns	364ns
1	0	0	6	16	640 ns	485ns
1	0	1	7	20	800 ns	606ns
1	1	0	8	24	960 ns	727ns
1	1	1	9	28	1120 ns	848ns

DUAL DATA POINTER

Data memory block moves can be accelerated using the DS80C310 Dual Data Pointer (DPTR). The standard 8032 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS80C310, the standard data pointer is called DPTR and is located at SFR addresses 82h and 83h. These are the standard locations. No modification of standard code is needed to use DPTR. The new DPTR is located at SFR 84h and 85h and is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer and is located at the lsb of the SFR location 86h. No other bits in register 86h have any effect and are set to 0. The user switches between data pointers by toggling the lsb of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore only one instruction is required to switch from a source to a destination address. Using the Dual Data Pointer saves code from needing to save source and destination addresses when doing a block move. Once loaded, the software simply switches between DPTR0 and 1. The relevant register locations are as follows.

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (lsb)

STOP MODE ENHANCEMENTS

Setting bit 1 of the Power Control register (PCON; 87h) invokes the Stop mode. Stop mode is the lowest power state since it turns off all internal clocking. The I_{CC} of a standard Stop mode is approximately 1 µA (but is specified in the Electrical Specifications). The CPU will exit Stop mode from an external interrupt or a reset condition. Internally generated interrupts are not useful since they require clocking activity.

The DS80C310 allows a resume from Stop using an INT2-5, which are edge-triggered interrupts. The start-up timing is managed by an internal crystal counter. A delay of 65,536 clocks occurs to give the crystal enough time to start and stabilize.

PERIPHERAL OVERVIEW

The DS80C310 provides the same peripheral functions as the standard 80C32. It is compatible with the DS80C320 but does not offer all of the peripherals.

TIMER RATE CONTROL

There is one important difference between the DS80C310 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers as well as for machine cycles. The DS80C310 architecture normally uses 4 clocks per machine cycle. However, in the area of timers and serial ports, the DS80C310 will default to 12 clocks per cycle on reset. This allows existing code with real-time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4-clock rate. The Clock Control register (CKCON; 8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the DS80C310 uses 4 clocks per cycle to generate timer speeds. When the bit is a 0, the DS80C310 uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Note that unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER ON RESET

The DS80C310 will hold itself in reset during a power-up until 65,536 clock cycles have elapsed. The power-on reset used by the DS80C310 differs somewhat from other members of the High-Speed Microcontroller family. The crystal oscillator may start anywhere between 1.0V and 4.5V but is not specified. This eliminates the need for an RC reset circuit. For voltage-specific precision brownout detection, an external component will be needed. When the device goes through a power-on reset, the POR flag will be set in the WDCON (D8h) register at bit 6.

INTERRUPTS

The DS80C310 provides 10 interrupt sources with two priority levels. Software can assign high or low priority to all sources. All interrupts that are new to the 8051 have a lower natural priority than the originals.

INTERRUPT SOURCES AND PRIORITIES Table 4

NAME	DESCRIPTION	VECTOR	NATURAL PRIORITY
$\overline{\text{INT0}}$	External Interrupt 0	03h	1
TF0	Timer 0	0Bh	2
$\overline{\text{INT1}}$	External Interrupt 1	13h	3
TF1	Timer 1	1Bh	4
SCON	T1 or R1 from the serial port	23h	5
TF2	Timer 2	2Bh	6
INT2	External Interrupt 2	43h	7
$\overline{\text{INT3}}$	External Interrupt 3	4Bh	8
INT4	External Interrupt 4	53h	9
$\overline{\text{INT5}}$	External Interrupt 5	5Bh	10

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.0	5.0	5.5	V	1
Supply Current Active Mode @ 33 MHz	I_{CC}		30		mA	2
Supply Current Idle Mode @ 33 MHz	I_{IDLE}		15		mA	3
Supply Current Stop Mode	I_{STOP}		1		µA	4
Input Low Level	V_{IL}	-0.3		+0.8	V	1
Input High Level (Except XTAL1 and RST)	V_{IH}	2.0		V_{CC}+0.3	V	1
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC}+0.3	V	1
Output Low Voltage Ports 1,3 @ I_{OL} = 1.6 mA	V_{OL1}		0.15	0.45	V	1
Output Low Voltage Port 0,2, ALE, $\overline{PSEN}$ @ I_{OL} =3.2 mA	V_{OL2}		0.15	0.45	V	1, 5
Output High Voltage Port 1, 3, ALE, $\overline{PSEN}$ @ I_{OH} =-50 µA	V_{OH1}	2.4			V	1, 6
Output High Voltage @ I_{OH} =-1.5mA Ports 1,3	V_{OH2}	2.4			V	1, 7
Output High Voltage Port 0, 2, ALE, $\overline{PSEN}$ @ I_{OH} =-8 mA	V_{OH3}	2.4			V	1, 5
Input Low Current Ports 1, 3 @ 0.45V	I_{IL}			-55	µA	10
Transition Current from 1 to 0 Ports 1,3 @ 2V	I_{TL}			-650	µA	8
Input Leakage Port 0, Bus Mode	I_L	-300		300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	KΩ	

NOTES FOR DC ELECTRICAL CHARACTERISTICS:

All parameters apply to both commercial and industrial temperature operation unless otherwise noted.

1. All voltages are referenced to ground.

2. Active current is measured with a 33 MHz clock source driving XTAL1, V_{CC} =RST=5.5V, all other pins disconnected.

3. Idle mode current is measured with a 33 MHz clock source driving XTAL1, V_{CC} =5.5V, RST at ground, all other pins disconnected.

4. Stop mode current measured with XTAL1 and RST grounded, V_{CC} =5.5V, all other pins disconnected.

5. When addressing external memory.

6. RST=V_{CC}. This condition mimics operation of pins in I/O mode.

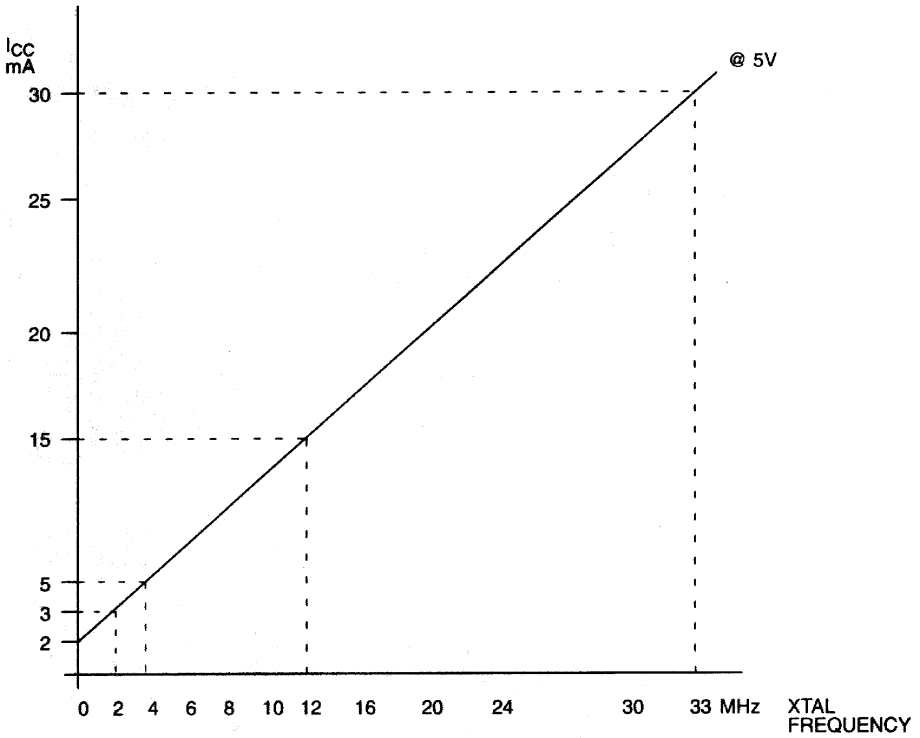
7. During a 0 to 1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.

8. Ports 1 and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.

9. 0.45<V_{IN} <V_{CC}. Not a high-impedance input. This port is a weak address holding latch because Port 0 is dedicated as an address bus on the DS80C310. Peak current occurs near the input transition point of the latch, approximately 2V.

10. Current required from external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to hold the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.

TYPICAL I_{CC} VERSUS FREQUENCY Figure 2



AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	25 MHz		VARIABLE CLOCK		NOTES
		MIN	MAX	MIN	MAX	
Oscillator Freq. (Ext. Osc.) (Ext. Crystal)	$1/t_{CLCL}$	0 1	33 33	0 1	33 33	MHz
ALe Pulse Width	t_{LHLL}	40		$1.5t_{CLCL}$-5		ns
Port 0 Address Valid to ALE Low	t_{AVLL}	10		$0.5t_{CLCL}$-5		ns
Address Hold after ALE Low	t_{LLAX1}	10		$0.5t_{CLCL}$-5		ns
ALE Low to Valid Instruction In	t_{LLIV}		56		$2.5t_{CLCL}$-20	ns
ALE Low to $\overline{\text{PSEN}}$ Low	t_{LLPL}	10		$0.5t_{CLCL}$-5		ns
$\overline{\text{PSEN}}$ Pulse Width	t_{PLPH}	55		$2t_{CLCL}$-5		ns
$\overline{\text{PSEN}}$ Low to Valid Instr. In	t_{PLIV}		41		$2t_{CLCL}$-20	ns
Input Instruction Hold after $\overline{\text{PSEN}}$	t_{PXIX}	0		0		ns
Input Instruction Float after $\overline{\text{PSEN}}$	t_{PXIZ}		26		t_{CLCL}-5	ns
Port 0 Address to Valid Instr. In	t_{AVIV}		71		$3t_{CLCL}$-20	ns
Port 2 Address to Valid Instr. In	t_{AVIV2}		81		$3.5t_{CLCL}$-25	ns
$\overline{\text{PSEN}}$ Low to Address Float	t_{PLAZ}		0		0	ns

NOTES FOR AC ELECTRICAL CHARACTERISTICS

All parameters apply to both commercial and industrial temperature range operation unless otherwise noted. All signals characterized with load capacitance of 80 pF except Port 0, ALE, $\overline{\text{PSEN}}$, and WR with 100 pF. Interfacing to memory devices with float times (turn off times) over 25 ns may cause contention. This will not damage the parts, but will cause an increase in operating current. Specifications assume a 50% duty cycle for the oscillator. Port 2 and ALE timing will change in relation to duty cycle variation.

MOVX CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK MIN	VARIABLE CLOCK MAX	UNITS	STRETCH
Data Access ALE Pulse Width	t_{LHLL2}	$1.5t_{CLCL}$-5 $2t_{CLCL}$-5		ns	t_{MCS}=0 t_{MCS}>0
Address Hold after ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL}$-5 t_{CLCL}-5		ns	t_{MCS}=0 t_{MCS}>0
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-5 t_{MCS}-10		ns	t_{MCS}=0 t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-5 t_{MCS}-10		ns	t_{MCS}=0 t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-20 t_{MCS}-20	ns	t_{MCS}=0 t_{MCS}>0
Data Hold after Read	t_{RHDX}	0		ns	
Data Float after Read	t_{RHDZ}		t_{CLCL}-5 $2t_{CLCL}$-5	ns	t_{MCS}=0 t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-20 t_{CLCL}+t_{MCS}-40	ns	t_{MCS}=0 t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-20 $1.5t_{CLCL+}$ t_{MCS} - 20	ns	t_{MCS}=0 t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-20 $2t_{CLCL+}$ t_{MCS}-20	ns	t_{MCS}=0 t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-5 t_{CLCL}-5	$0.5t_{CLCL}$+5 t_{CLCL}+5	ns	t_{MCS}=0 t_{MCS}>0
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-5 $2t_{CLCL}$-5		ns	t_{MCS}=0 t_{MCS}>0
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-10 $2.5t_{CLCL}$-10		ns	t_{MCS}=0 t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-5		ns	
Data Hold after Write	t_{WHQX}	t_{CLCL}-5 $2t_{CLCL}$-5		ns	t_{MCS}=0 t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		$-0.5t_{CLCL}$-5	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	0 t_{CLCL}-5	10 t_{CLCL}+5	ns	t_{MCS}=0 t_{MCS}>0

NOTE: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock High Time	t_{CHCX}	10			ns	
Clock Low Time	t_{CLCX}	10			ns	
Clock Rise Time	t_{CLCL}			5	ns	
Clock Fall Time	t_{CHCL}			5	ns	

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

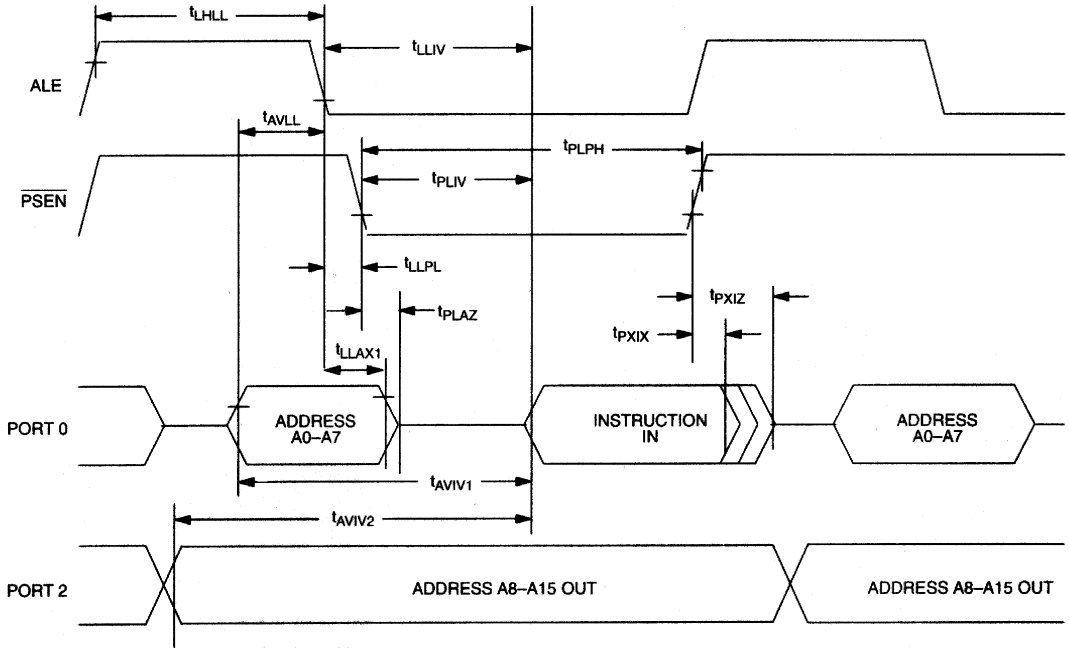
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Serial Port Clock Cycle Time SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XLXL}		$12t_{CLCL}$ $4t_{CLCL}$		ns ns	
Output Data Setup to Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{QVXH}		$10t_{CLCL}$ $3t_{CLCL}$		ns ns	
Output Data Hold from Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHQX}		$2t_{CLCL}$ t_{CLCL}		ns ns	
Input Data Hold after Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDX}		t_{CLCL} t_{CLCL}		ns ns	
Clock Rising Edge to Input Data Valid SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDV}		$11t_{CLCL}$ $3t_{CLCL}$		ns ns	

EXPLANATION OF AC SYMBOLS

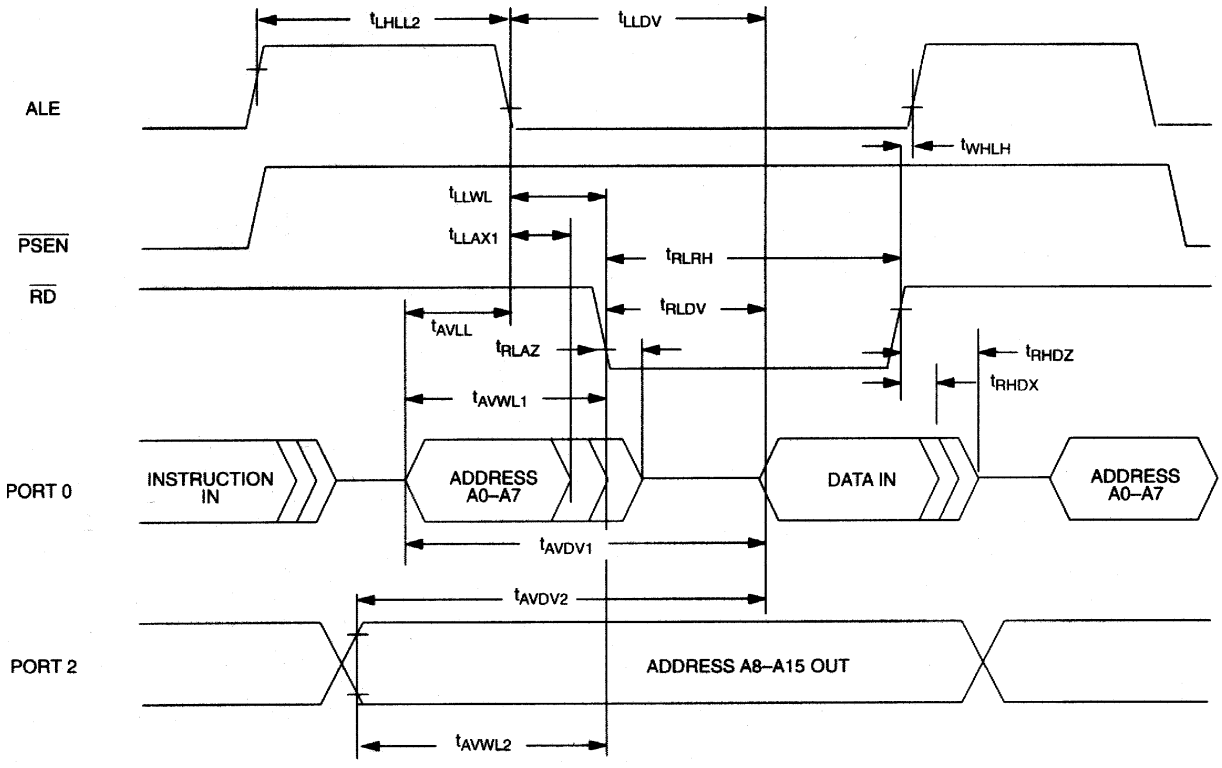
In an effort to remain compatible with the original 8051 family, this device specifies the same parameters as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t Time
A Address
C Clock
D Input data
H Logic level high
L Logic level low
I Instruction
P $\overline{\text{PSEN}}$
Q Output data
R $\overline{\text{RD}}$ signal
V Valid
W $\overline{\text{WR}}$ signal
X No longer a valid logic level
Z Tristate

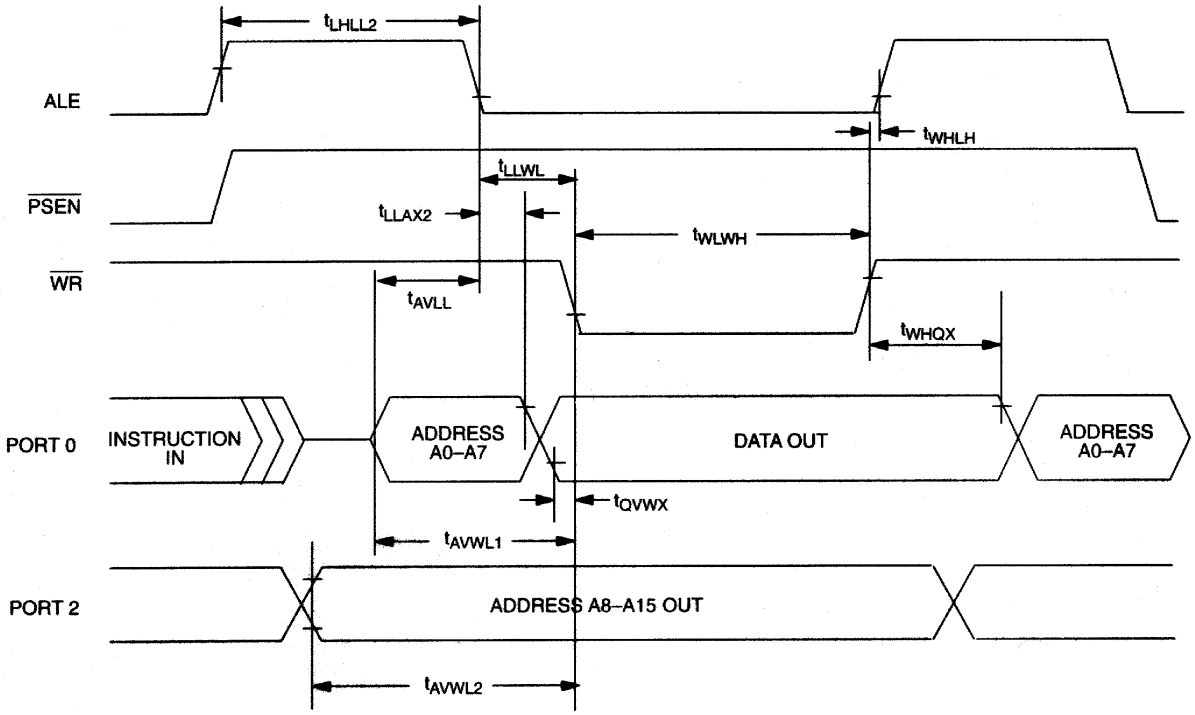
EXTERNAL PROGRAM MEMORY READ CYCLE



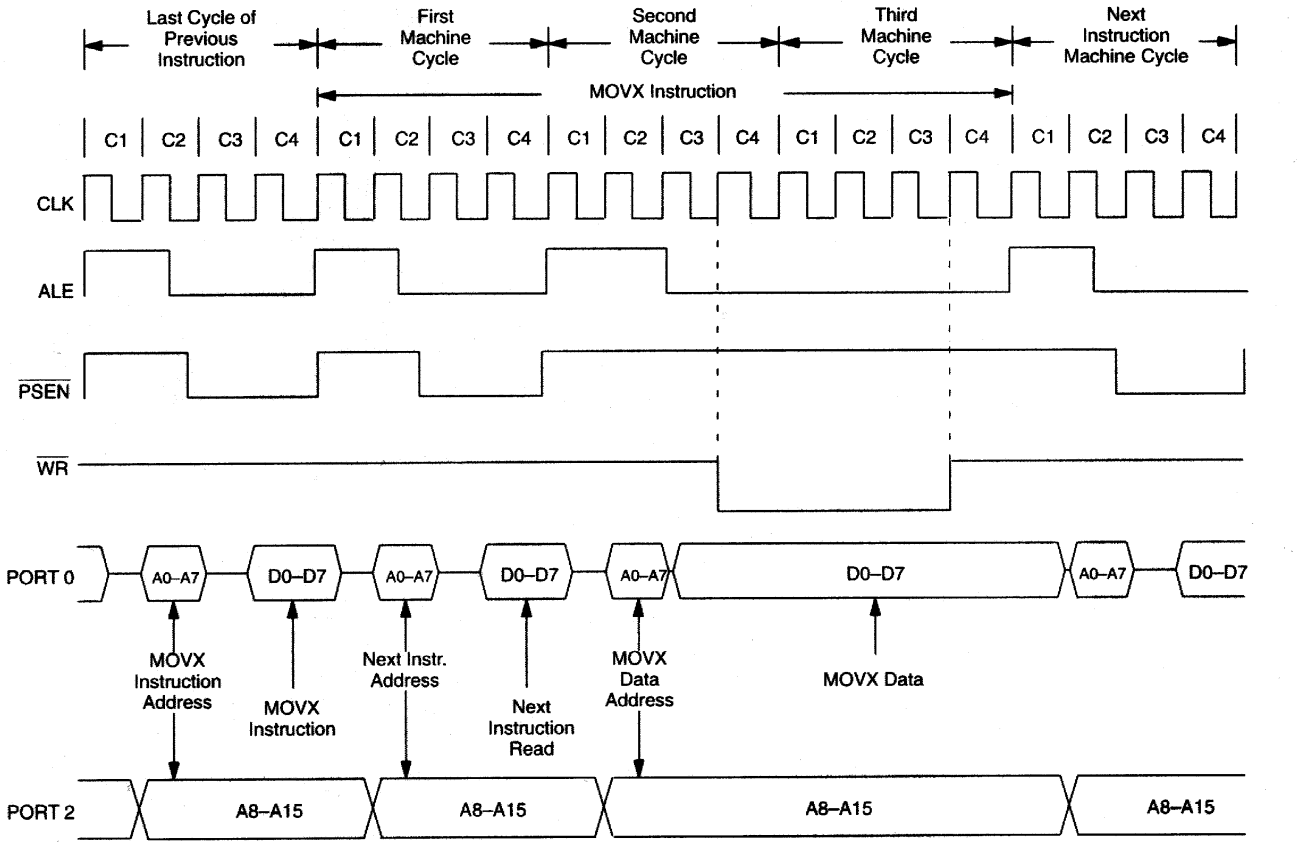
EXTERNAL DATA MEMORY READ CYCLE



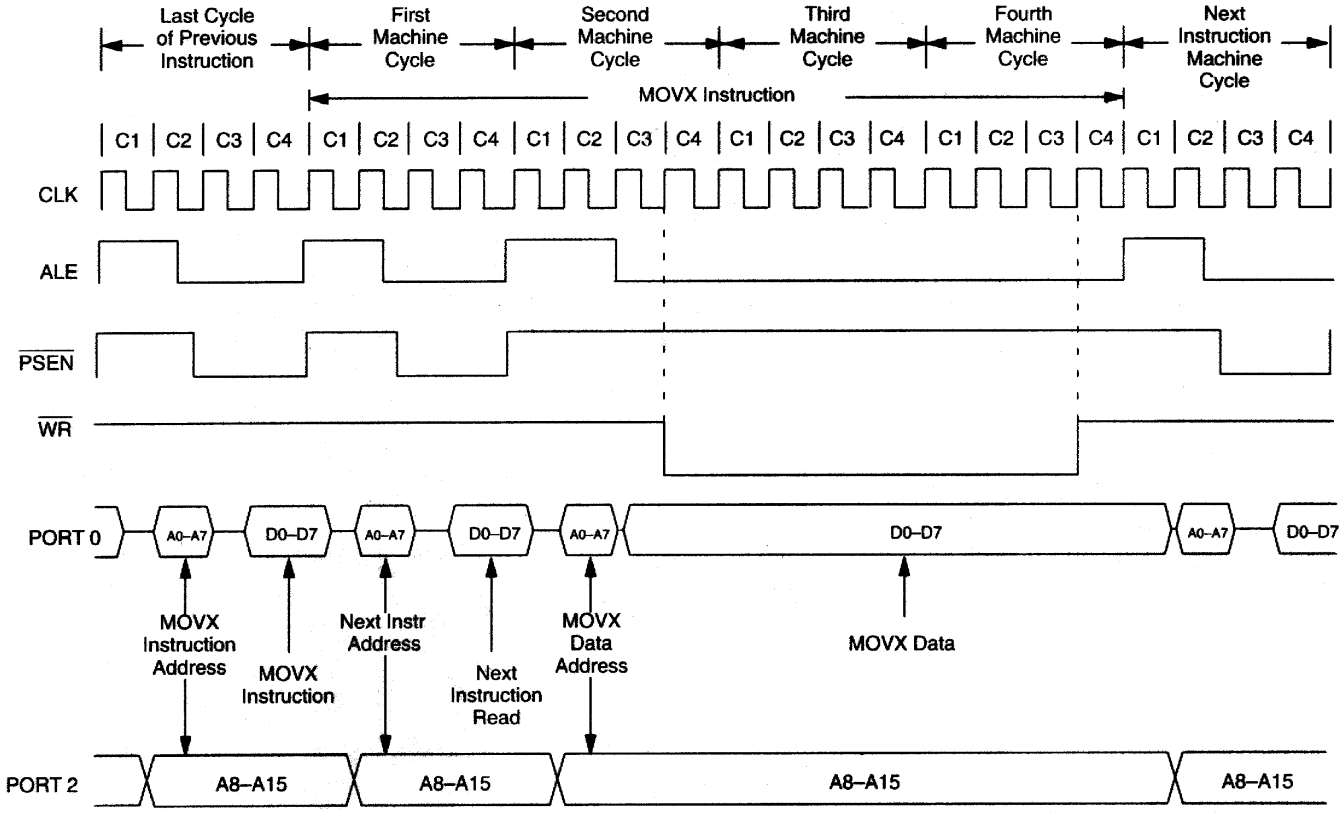
DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH=1

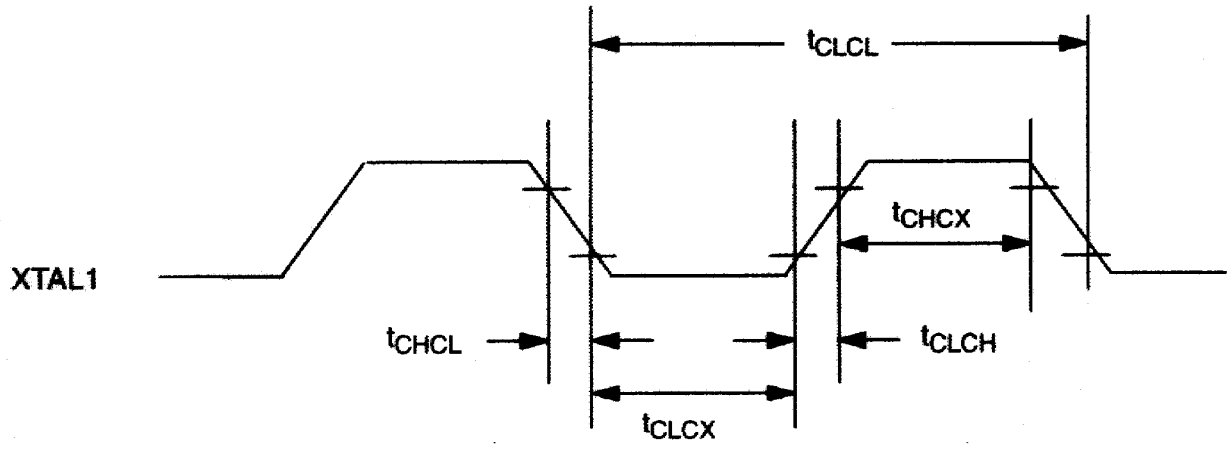


DATA MEMORY WRITE WITH STRETCH=2



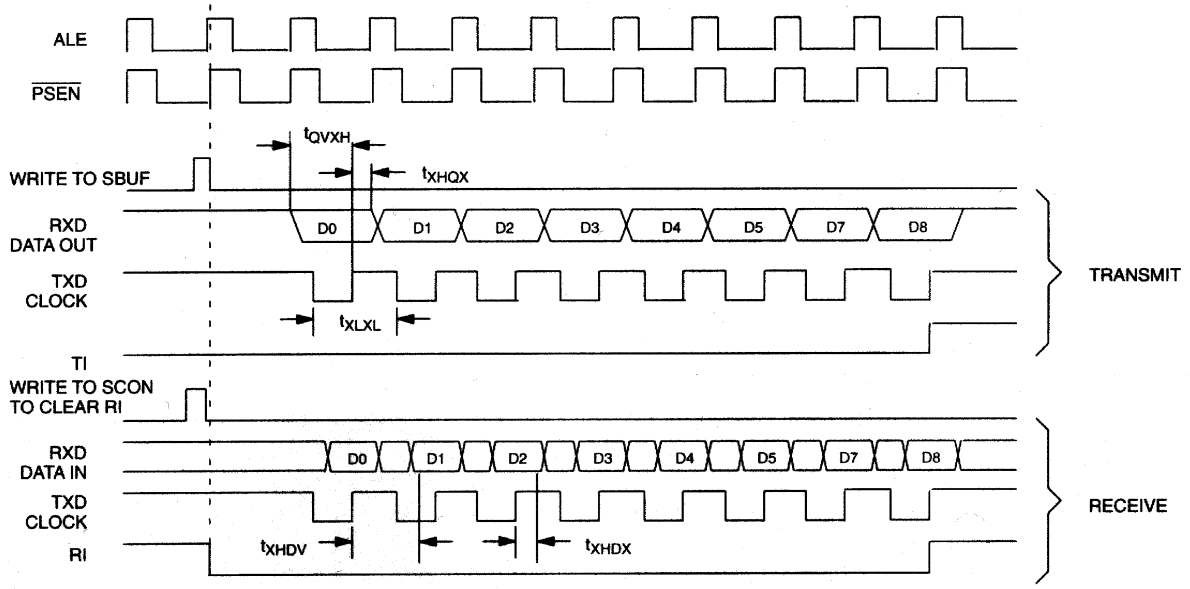
FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

EXTERNAL CLOCK DRIVE

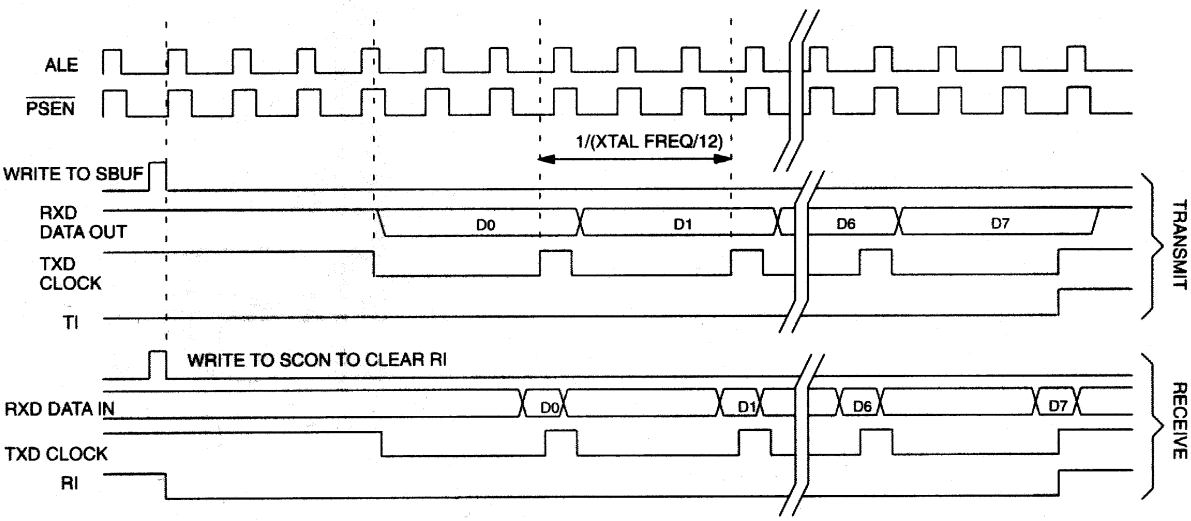


SERIAL PORT MODE 0 TIMING

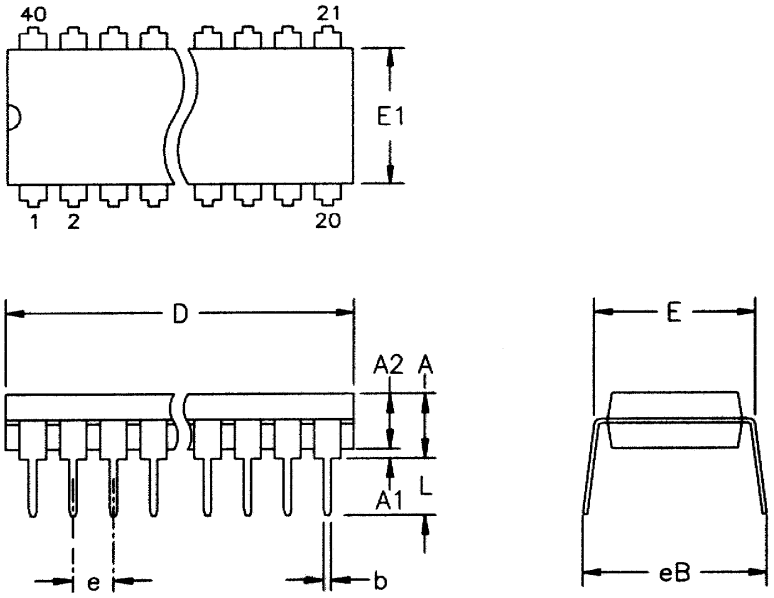
SERIAL PORT 0 (SYNCHRONOUS MODE)
HIGH-SPEED OPERATION SM2=1=>TXD CLOCK=XTAL/4



SERIAL PORT 0 (SYNCHRONOUS MODE)
SM2=0=>TXD CLOCK=XTAL/12



40-PIN PDIP (600-MIL)

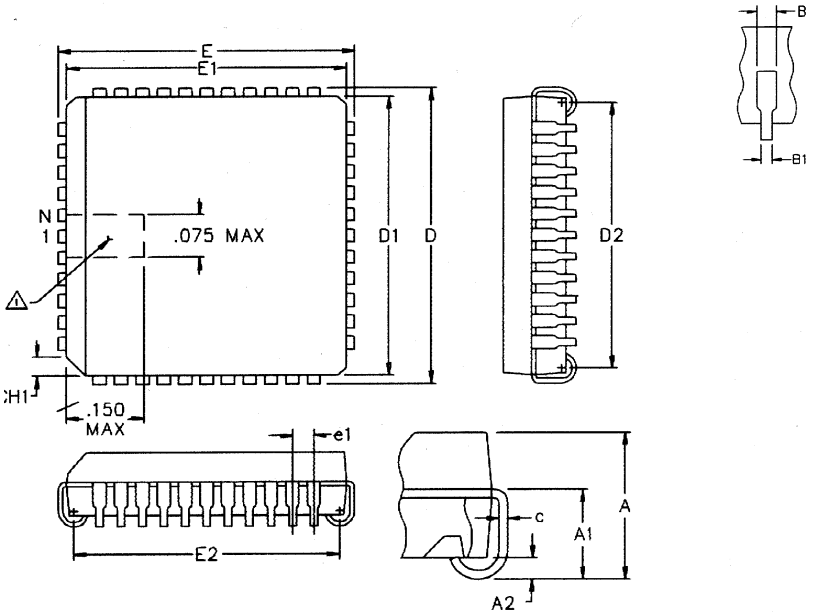


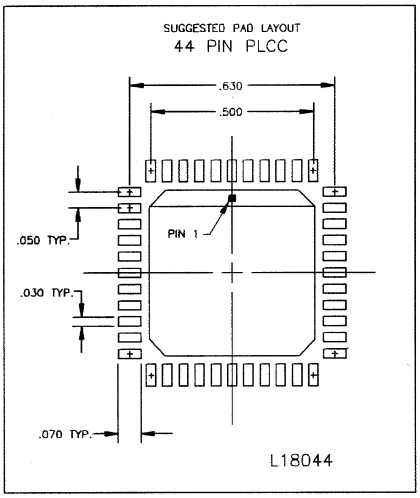
ALL DIMENSIONS ARE IN INCHES.

PKG	40-PIN	
DIM	MIN	MAX
A	-	0.200
A1	0.015	-
A2	0.140	0.160
b	0.014	0.022
c	0.008	0.012
D	1.980	2.085
E	0.600	0.625
E1	0.530	0.555
e	0.090	0.110
L	0.115	0.145
eB	0.600	0.700

44-PIN PLCC

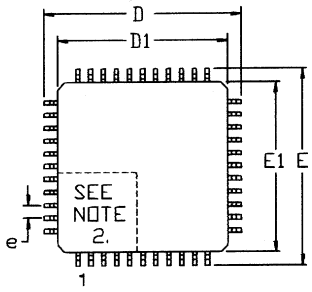
NOTE:
1. PIN-1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.
2. CONTROLLING DIMENSIONS ARE IN INCHS





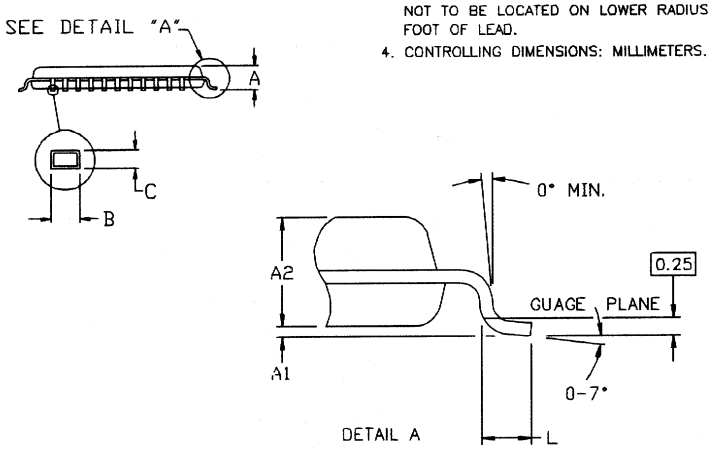
PKG	44-PIN	
DIM	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	-
B	0.026	0.033
B1	0.013	0.021
c	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	-

44-PIN TQFP



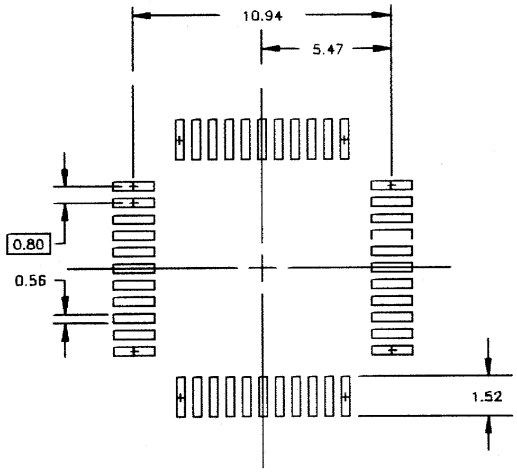
NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. CONTROLLING DIMENSIONS: MILLIMETERS.



SUGGESTED PAD LAYOUT

44 PIN TQFP, 10*10*1.0



PKG	44-PIN	
DIM	MIN	MAX
A	-	1.20
A1	0.05	0.15
A2	0.95	1.05
D	11.80	12.20
D1	10.00 BSC	
E	11.80	12.20
E1	10.00 BSC	
L	0.45	0.75
e	0.80 BSC	
B	0.30	0.45
C	0.09	0.20

56-G4012-001

DATA SHEET REVISION SUMMARY

The following represent the key differences between 02/19/98 and 09/01/98 version of the DS80C310 data sheet. Please review this summary carefully.

1. Add note to clarify I_{IL} specification.
2. Change serial port mode 0 timing diagram label from t_{QVXL} to t_{QVXH}.
3. Changed minimum oscillator frequency to 1 MHz when using external crystal.
4. Corrected “Data memory write with stretch” diagrams to show falling edge of ALE coincident with rising edge of C3 clock.