July 1998

National Semiconductor

LM9810/20 10/12-Bit Image Sensor Processor Analog Front End

General Description

The LM9810 and LM9820 are high performance Analog Front Ends (AFEs) for image sensor processing systems. The LM9810/20 performs all the analog and mixed signal functions (correlated double sampling, color specific gain and offset correction, and analog to digital conversion) necessary to digitize the output of a wide variety of CIS and CCD sensors. The LM9810 has a 10 bit 6MHz ADC, and the LM9820 has a 12 bit 6MHz ADC. The LM9810 and LM9820 are pin-for-pin and functionally compatible.

Applications

- Color Flatbed Document Scanners
- Color Sheetfed Scanners
- Multifunction Imaging Products
- Digital Copiers
- General Purpose Linear CCD Imaging

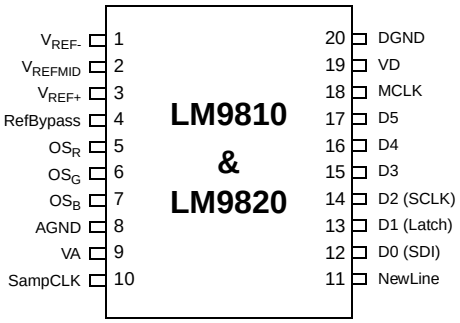
Features

- 6 million pixels/s conversion rate
- Digitally programmed gain and offset for red, green and blue pixels
- Correlated Double Sampling for lowest noise
- TTL/CMOS input/output compatible

Key Specifications

• Output Data Resolution	10/12 Bits
• Pixel Conversion Rate	6MHz
• Supply Voltage	5V±5%
• Power Dissipation	300mW

Connection Diagrams



Ordering Information

Commercial (0°C ≤ T_A ≤ +70°C)	Package
LM9810CCWM	20 Pin Wide SOIC
LM9810CCWMX	20 Pin Wide SOIC, Tape & Reel
LM9820CCWM	20 Pin Wide SOIC
LM9820CCWMX	20 Pin Wide SOIC, Tape & Reel

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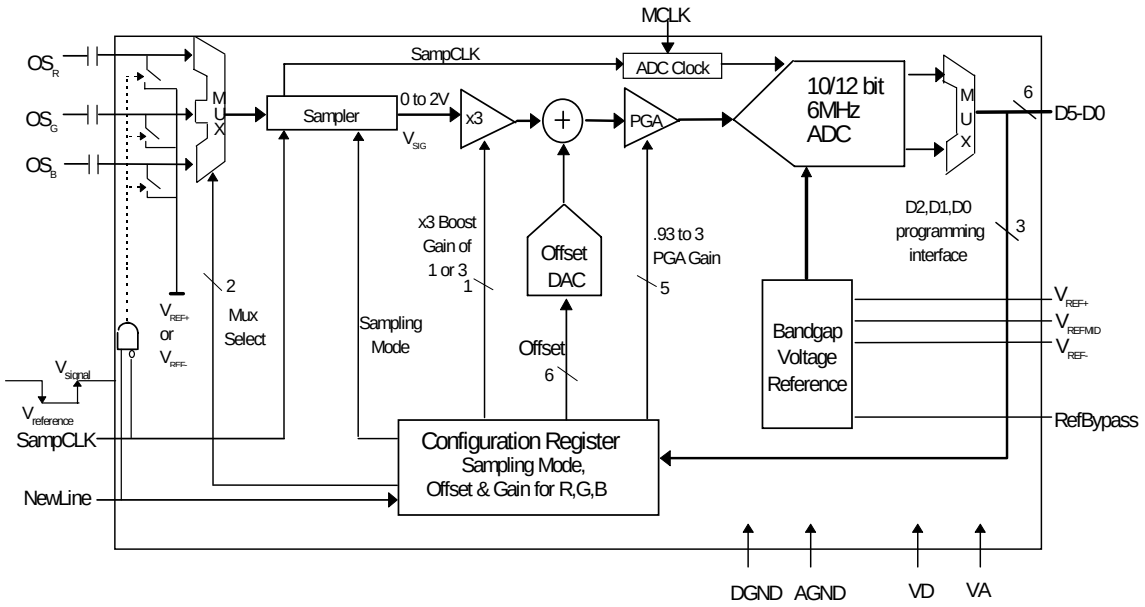
Block Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

Positive Supply Voltage (V^+=VA=VD)	
With Respect to GND=AGND=DGND	6.5V
Voltage On Any Input or Output Pin	-0.3V to V^++0.3V
Input Current at any pin (Note 3)	±25mA
Package Input Current (Note 3)	±50mA
Package Dissipation at T_A = 25°C	(Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2000V
Soldering Information	
Infrared, 10 seconds (Note 6)	300°C
Storage Temperature	-65°C to +150°C

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	T_{MIN}=0°C≤T_A≤T_{MAX}=+70°C
VA Supply Voltage	+4.75V to +5.25V
VD Supply Voltage	+4.75V to +5.25V
|VA-VD|	≤ 100mV
OS_R, OS_G, OS_B	
Input Voltage Range	-0.05V to VA + 0.05V
NewLine, SampCLK, D0-D2, MCLK	
Input Voltage Range	-0.05V to VD + 0.05V

Electrical Characteristics

The following specifications apply for AGND=DGND=0V, VA=VD=+5.0V_{DC}, f_{MCLK}=24MHz, R_s=25Ω. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7, 8, & 12)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
CCD/CIS Source Requirements for Full Specified Accuracy and Dynamic Range (Note 12)					
$V_{OS\ PEAK}$	Sensor's Maximum Peak Differential Signal Range	Gain = 0.933 Gain = 3.0 Gain = 9.0	2.1 0.65 0.21		V V V
Analog Input Characteristics					
	OS_R, OS_G, OS_B Input Capacitance		5		pF
	OS_R, OS_G, OS_B Input Leakage Current	Measured with OS = 3.5V_{DC} CDS disabled, selected OS input	20	**25**	µA (max)
		CDS disabled, unselected OS input	10		nA
Coarse Color Balance PGA Characteristics					
	Monotonicity			**5**	bits (min)
	G_0 (Minimum PGA Gain)	PGA Setting = 0	0.93	**.90** **.96**	V/V (min) V/V (max)
	G_{31} (Maximum PGA Gain)	PGA Setting = 31	3.0	**2.96** **3.15**	V/V (min) V/V (max)
	x3 Boost Gain	x3 Boost Setting On (bit B5 of Gain Register is set)	3.0	**2.93** **3.05**	V/V (min) V/V (max)
	Gain Error at any gain (Note 13)		±0.4	**1.67**	% (max)
Internal Reference Characteristics					
V_{REFMID}	Mid Supply Output Voltage		2.5		V
V_{REF+}	Positive Reference Output Voltage		3.5		V
V_{REF-}	Negative Reference Output Voltage		1.5		V
ΔV_{REF}	Differential Reference Voltage V_{REF+} - V_{REF-}		2.0		V

LM9810 Electrical Characteristics

The following specifications apply for AGND=DGND=0V, VA=VD=+5.0V$_{DC}$, f_{MCLK}=24MHz, R_s=25Ω. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. All LSB limits are in units of the LM9810's 10 bit ADC. (Notes 7, 8, & 12)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
ADC Characteristics					
	Resolution with No Missing Codes			**10**	bits (min)
INL	Integral Non-Linearity Error (Note 11)		±0.35	**±1.5**	LSB (max)
DNL	Differential Non-Linearity		±0.25	**±1.0**	LSB (max)
Full Channel Linearity (Note 14)					
INL	Integral Non-Linearity Error (Note 11)		±0.9		LSB
DNL	Differential Non-Linearity		±0.40		LSB
Static Offset DAC Characteristics					
	Monotonicity			**6**	bits (min)
	Offset DAC LSB size	PGA gain = 1	5	**3.4** **6.4**	LSB (min) LSB (max)
	Offset DAC Adjustment Range	PGA gain = 1	±150	**±140**	LSB (min)
System Characteristics (see section 1.7.1, Internal Offsets)					
C	Analog Channel Gain Constant (ADC Codes/V)	Includes voltage reference variation, gain setting = 1	502	**468** **532**	LSB (min) LSB (max)
V_{OS1}	Pre-Boost Analog Channel Offset Error, CCD Mode		4.4	**-7.2** **+15.7**	LSB (min) LSB (max)
V_{OS1}	Pre-Boost Analog Channel Offset Error, CIS Mode		4.5	**-6.5** **+15.2**	LSB (min) LSB (max)
V_{OS2}	Pre-PGA Analog Channel Offset Error		-10	**-28** **+5.3**	LSB (min) LSB (max)
V_{OS3}	Post-PGA Analog Channel Offset Error		-11	**-30.6** **+7.3**	LSB (min) LSB (max)

LM9820 Electrical Characteristics

The following specifications apply for AGND=DGND=0V, VA=VD=+5.0V$_{DC}$, f_{MCLK}=24MHz, R_s=25Ω. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. All LSB limits are in units of the LM9820's 12 bit ADC. (Notes 7, 8, & 12)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
ADC Characteristics					
	Resolution with No Missing Codes			**12**	bits (min)
INL	Integral Non-Linearity Error (Note 11)		±1.1	**±4.0**	LSB (max)
DNL	Differential Non-Linearity		±0.6	**+1.75** **-1.0**	LSB (max)
Full Channel Linearity (Note 14)					
INL	Integral Non-Linearity Error (Note 11)		±3.4		LSB
DNL	Differential Non-Linearity		±0.65		LSB

LM9820 Electrical Characteristics (Continued)

The following specifications apply for AGND=DGND=0V, VA=VD=+5.0V$_{DC}$, f_{MCLK}=24MHz, R_s=25Ω. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. All LSB limits are in units of the LM9820's 12 bit ADC. (Notes 7, 8, & 12)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
Static Offset DAC Characteristics					
	Monotonicity			**6**	bits (min)
	Offset DAC LSB size	PGA gain = 1	20	**14** **26**	LSB (min) LSB (max)
	Offset DAC Adjustment Range	PGA gain = 1	±590	**±575**	LSB (min)
System Characteristics (see section 1.7.1, Internal Offsets)					
C	Analog Channel Gain Constant (ADC Codes/V)	Includes voltage reference variation, gain setting = 1	2008	**1873** **2129**	LSB (min) LSB (max)
V_{OS1}	Pre-Boost Analog Channel Offset Error, CCD Mode		17.6	**-32.1** **+68.9**	LSB (min) LSB (max)
V_{OS1}	Pre-Boost Analog Channel Offset Error, CIS Mode		18	**-22.2** **+57**	LSB (min) LSB (max)
V_{OS2}	Pre-PGA Analog Channel Offset Error		-40	**-94.3** **+16.4**	LSB (min) LSB (max)
V_{OS3}	Post-PGA Analog Channel Offset Error		-44	**-121** **+28**	LSB (min) LSB (max)

DC and Logic Electrical Characteristics

The following specifications apply for AGND=DGND=0V, VA=VD=+5.0V$_{DC}$, f_{MCLK}=24MHz, R_s=25Ω. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
D0-D2, MCLK, NewLine, SampCLK Digital Input Characteristics					
$V_{IN(1)}$	Logical "1" Input Voltage	VD=5.25V		**2.0**	V (max)
$V_{IN(0)}$	Logical "0" Input Voltage	VD=4.75V		**0.8**	V (min)
I_{IN}	Input Leakage Current	V_{IN}=VD V_{IN}=DGND	0.1 -0.1		µA(max) µA(max)
C_{IN}	Input Capacitance		5		pF
D0-D5 Digital Output Characteristics					
$V_{OUT(1)}$	Logical "1" Output Voltage	VD=4.75V, I_{OUT}=-360µA VD=4.75V, I_{OUT}=-10µA		**2.4** **4.4**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	VD=5.25V, I_{OUT}=1.6mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current (D0-D5 only)	V_{OUT}=DGND V_{OUT}=VD	0.1 -0.1		µA µA
Power Supply Characteristics					
I_A	Analog Supply Current	Operating Standby with input clocks stopped Standby with input clocks running	45 0.8 3.0	**57** **0.9**	mA (max) mA (max) mA
I_D	Digital Supply Current (Note 15)	Operating Standby with input clocks stopped Standby with input clocks running	220 110 220	**320** **200**	µA (max) µA (max) µA

AC Electrical Characteristics

The following specifications apply for AGND=DGND=0V, VA=VD=+5.0V$_{DC}$, f_{MCLK}=24MHz, t_{MCLK}=1/f_{MCLK}, t_r=t_f=5ns, R_s=25Ω. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
f_{MCLK}	Maximum MCLK Frequency			**24**	MHz (min)
	MCLK Duty Cycle			**40** **60**	% (min) % (max)
t_{MCLK}	MCLK period		41		ns (min)
t_{SCNL}	SampCLK falling edge before NewLine falling edge			**3**	t_{MCLK}(min)
$t_{SampCLK}$	SampCLK period			**4**	t_{MCLK}(min)
t_{SampLo}	Low time for SampCLK		50		ns (min)
t_{SampHi}	High time for SampCLK		50		ns (min)
t_{SampSU}	SampCLK falling edge before rising edge of MCLK			**4**	ns (min)
t_{DDO}	falling edge of MCLK before new valid data			**40**	ns (max)
t_{HDO}	hold time of current data from falling edge of MCLK			**15**	ns (min)
t_{SCLK}	D2(SCLK) Serial Clock Period		1		t_{MCLK}(min)
t_{DSU}	Input data setup time before D2(SCLK) rising edge			**0**	ns (min)
t_{DH}	Input data hold time after D2(SCLK) rising edge			**3**	ns (min)
t_{SCLKLA}	D2(SCLK) rising edge after bit B0 before D1(Latch) rising edge			**3**	ns (min)
t_{LASCLK}	D1(Latch) rising edge before next D2(SCLK) rising edge			**3**	ns (min)
t_{LA}	High time for D1(Latch)			**3**	t_{MCLK} (min)
t_{LANL}	D1(Latch) rising edge before NewLine falling edge			**3**	$t_{SampCLK}$ (min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND=AGND=DGND=0V, unless otherwise specified.

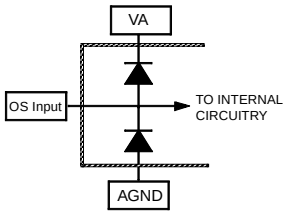
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN}<GND or V_{IN}>VA or VD), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is P_D = ($T_J$max - T_A) / Θ_{JA}. $T_J$max = 150°C for this device. The typical thermal resistance (Θ_{JA}) of this part when board mounted is 84°C/W for the M20B SOIC package.

Note 5: Human body model, 100pF capacitor discharged through a 1.5kΩ resistor.

Note 6: See AN450 “Surface Mounting Methods and Their Effect on Product Reliability” or the section titled “Surface Mount” found in any National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Two diodes clamp the OS analog inputs to AGND and VA as shown below. This input protection, in combination with the external clamp capacitor and the output impedance of the sensor, prevents damage to the LM9810/20 from transients during power-up.



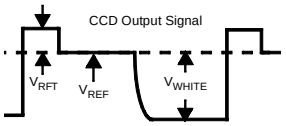
Note 8: To guarantee accuracy, it is required that VA and VD be connected together to the same power supply with separate bypass capacitors at each supply pin.

Note 9: Typicals are at T_J=T_A=25°C, f_{MCLK} = 24MHz, and represent most likely parametric norm.

Note 10: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Integral non-linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that best fits the actual transfer function of the ADC.

Note 12: V_{REF} is defined as the CCD OS voltage for the reference period following the reset feedthrough pulse. V_{WHITE} is defined as the peak CCD pixel output voltage for a white (full scale) image with respect to the reference level, V_{REF} . V_{RFT} is defined as the peak positive deviation above V_{REF} of the reset feedthrough pulse. The maximum correctable range of pixel-to-pixel V_{WHITE} variation is defined as the maximum variation in V_{WHITE} (due to PRNU, light source intensity variation, optics, etc.) that the LM9810/20 can correct for using its internal PGA.



Note 13: PGA Gain Error is the maximum difference between the measured gain for any PGA code and the ideal gain calculated by using the formula $\text{Gain}_{PGA}\left(\frac{V}{V}\right) = G_0 + X\frac{\text{PGA code}}{32}$ where $X = (G_{31} - G_0)\frac{32}{31}$.

Note 14: Full Channel INL and DNL are tested with CDS disabled, negative signal polarity, and a single OS input with a gain register setting of 1 (000001b) and an offset register setting of 0 (000000b).

Note 15: The digital supply current (I_D) does not include the load, data and switching frequency dependent current required to drive the digital output bus on pins (D5 - D0). The current required to switch the digital data bus can be calculated from: Isw = 2*Nd*Psw*CL*VD/tSampCLK where Nd is total number of data pins, Psw is the probability of each data bit switching, CL is the capacitive loading on each data pin, VD is the digital supply voltage and tSampCLK is the period of the SampCLK signal. Since Nd is 6, Psw should be .5, and VD is nominally 5V, the switching current can usually be calculated from: Isw = 30*CL/tSampCLK. For example, if the capacitive load on each digital output pin (D5 - D0) is 20pF and the period of tSampCLK is 1/6MHz or 167ns , then the digital switching current would be 7.2mA. The calculated digital switching current will be drawn through the VD pin and should be considered as part of the total power budget for he LM9810/20.

Pin Descriptions

Analog Power	
VA	This is the positive supply pin for the analog supply. It should be connected to a voltage source of +5V and bypassed to AGND with a 0.1µF monolithic capacitor in parallel with a 10µF tantalum capacitor.
AGND	This is the ground return for the analog supply.
Analog I/O	
OS_R, OS_G, OS_B,	Analog Inputs. These inputs (for Red, Green, and Blue) should be tied to the sensor's OS (Output Signal) through DC blocking capacitors.
RefBypass	Internally generated reference voltage bypass pin. It should be bypassed to AGND through a .05uF monolithic capacitor.
V_{REF+}, V_{REFMID}, V_{REF-}	Voltage reference bypass pins. They should each be bypassed to AGND through a .05uF monolithic capacitor.
Input & Timing Control	
MCLK	Master Clock. The ADC conversion rate will be a maximum of ¼ of MCLK. Nominally 24MHz.
SampCLK	Sample Clock. SampCLK controls the conversion rate of the ADC (up to ¼ of the MCLK rate) and sample timing. The signal level is sampled while SampCLK is low and held on the rising edge of SampCLK. When CDS is enabled, the falling edge of SampCLK causes the CCD reference level to be held. If CDS is not enabled, V_{REF+} or V_{REF-} is held on the falling edge of SampCLK, depending on the programmed signal polarity. SampCLK is also used with NewLine to clamp the external coupling capacitors.
NewLine	New Line signal. Used to indicate the start of active pixels on a new line, to allow clamping of the AC coupling caps, and to allow programming of the configuration register. When NewLine is high and SampCLK is low, the OS inputs will be connected to either V_{REF+} or V_{REF-}. On the first rising edge of MCLK after NewLine goes low, the internal mux and the offset and gain settings will be set to the appropriate values for the first color of the next line set in the color mode setting in the Sampler and Color Mode Register. When NewLine is low, D[5-0] transmit the pixel conversion data from the ADC. When NewLine is high, D[5-0] enter TRI-STATE and D2, D1 and D0 act as a serial interface for programming the configuration registers.

Digital Power				
VD	This is the positive supply pin for the digital supply. It should be connected to a voltage source of +5V and bypassed to DGND with a 0.1µF monolithic capacitor.			
DGND	This is the ground return for the digital supply.			
Digital I/O				
D5-D0	Data Input/Output pins. When NewLine is low, the 10 or 12 bit conversion results of the ADC are multiplexed to D5-D0. When NewLine is high, the output drivers enter TRI-STATE and D2, D1 & D0 act as a serial interface for writing to the configuration registers.			
LM9810 Output Mode (NewLine Low)	MCLK0, MCLK1, MCLK2, MCLK3			
D5	b9,	b9,	b3,	b3
D4	b8,	b8,	b2,	b2
D3	b7,	b7,	b1,	b1
D2	b6,	b6,	b0,	b0
D1	b5,	b5,	0,	0
D0	b4,	b4,	0,	0
LM9820 Output Mode (NewLine Low)	MCLK0, MCLK1, MCLK2, MCLK3			
D5	b11,	b11,	b5,	b5
D4	b10,	b10,	b4,	b4
D3	b9,	b9,	b3,	b3
D2	b8,	b8,	b2,	b2
D1	b7,	b7,	b1,	b1
D0	b6,	b6,	b0,	b0
Input Mode (NewLine High)				
D5-D3	Don't Care			
D2 (SCLK)	Serial Data Clock.			
D1 (Latch)	Latch and shift enable signal. When D1(Latch) is low, data is shifted into D0(SDI). When D1(Latch) goes high, the last nine bits shifted into D0(SDI) will be used to program the addressed configuration register. To avoid erroneous writes to the configuration registers, D1(Latch) should be pulled low when NewLine is high.			
D0 (SDI)	Serial input data. Data is valid on D2(SCLK) rising edge. Three address bits followed by six data bits (MSB first) should be shifted into D0 before D1(Latch) goes high.			

Timing Diagrams

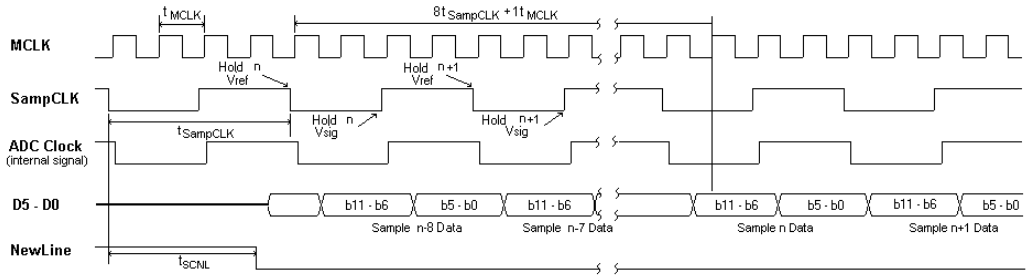


Diagram 1: Pixel Conversion Timing and Latency

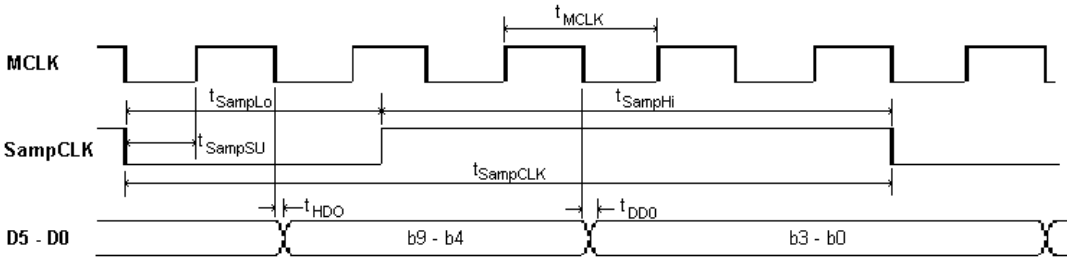


Diagram 2: SampCLK and Output Data Timing (NewLine low)

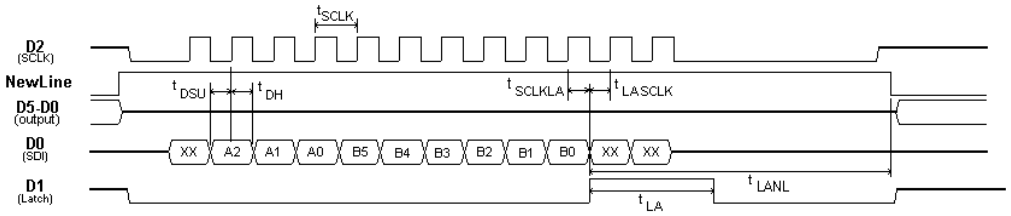


Diagram 3: Timing for Programming the Configuration Registers

Timing Diagrams

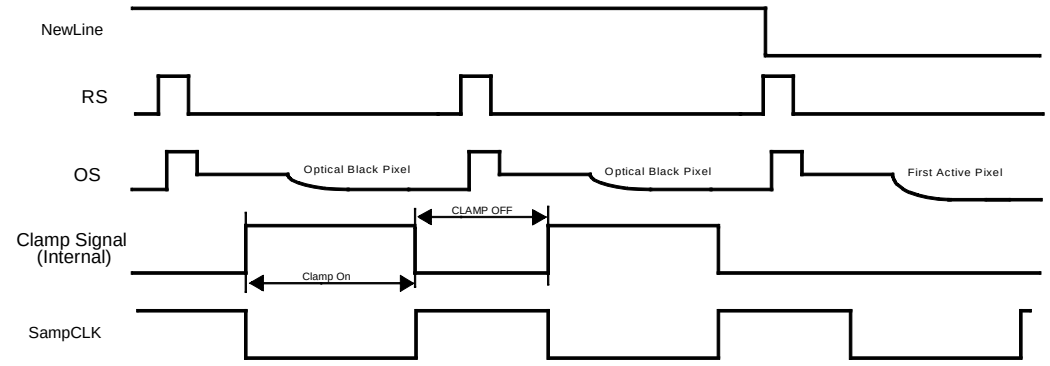


Diagram 4: CCD Clamping Timing

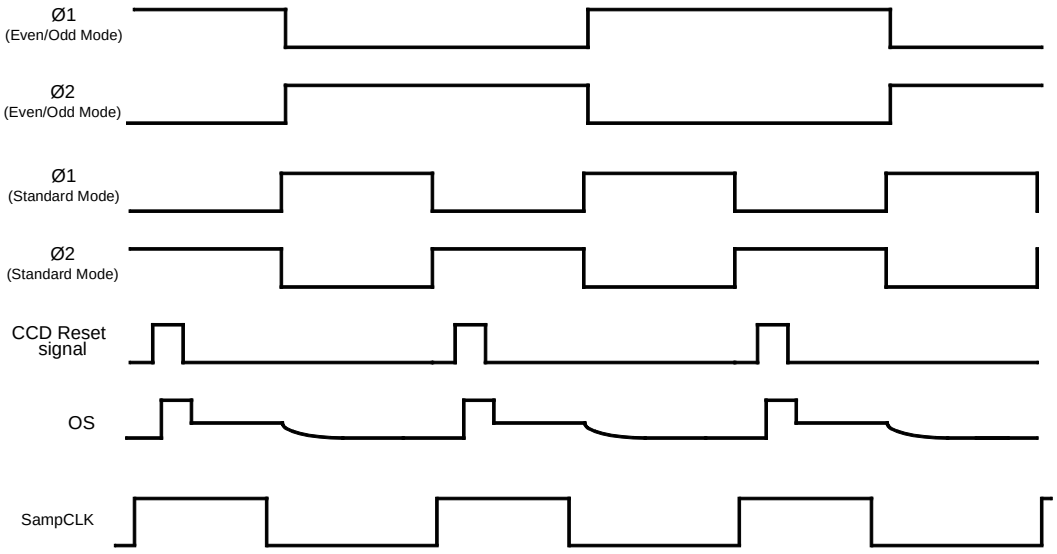


Diagram 5: CDS Timing

Table 1: Configuration Register Address Table

Address (Decimal)	Address (Binary)			Data Bits					
	A2	A1	A0	B5	B4	B3	B3	B2	B1
0	0	0	0	Sampler and Color Mode					
				CDS	Polarity	N/A	Mode2	Mode1	Mode0
1	0	0	1	Red DAC Offset Setting					
				Polarity	MSB				LSB
2	0	1	0	Green DAC Offset Setting					
				Polarity	MSB				LSB
3	0	1	1	Blue DAC Offset Setting					
				Polarity	MSB				LSB
4	1	0	0	Red Gain Setting					
				x3	MSB				LSB
5	1	0	1	Green Gain Setting					
				x3	MSB				LSB
6	1	1	0	Blue Gain Setting					
				x3	MSB				LSB
7	1	1	1	Production Test and Power Down					
				Test	Test	Test	Test	Test	PD

Table 2: Configuration Register Parameters

Parameter (Address)	Control Bits			Result
Sampler and Color Mode (0)				
CDS Enable (0)	**B5** 0 1			**CDS Enabled** **Single Ended (CDS disabled)**
Signal Polarity (0)	**B4** 0 1			**Negative Polarity** **Positive Polarity**
Color Mode (0)	**B2**	**B1**	**B0**	
	0	0	0	**Line Rate Color** - *Mux, Gain & Offset change at the line rate:* **1st line: Mux = OS_R, Gain & Offset = R* *2nd line: Mux = OS_G Gain & Offset = G* *3rd line: Mux = OS_B Gain & Offset = B* *repeat…* ** state of the first line after a write to this register*
	0	0	1	**Single Input Color** - *Mux selects OS_B input. Gain & Offset change at the pixel rate:* *Gain & Offset = R,G,B,R,G,B…*
	0	1	0	**RESERVED**
	0	1	1	**Monochrome** *Mux selects OS_R input. Gain & Offset = R*
	1	0	0	**Monochrome** *Mux selects OS_G input. Gain & Offset = G*
	1	0	1	**Monochrome** *Mux selects OS_B input. Gain & Offset = B*
	1	1	0	**Bayer** - *Mux selects OS_B input. Gain & Offset change at the pixel rate:* **1st line: Gain & Offset = G,R,G,R,...* *2nd line: Gain & Offset = B,G,B,G,…* *repeat…* ** state of the first line after a write to this register*
	1	1	1	**Green Stripe** - *Mux selects OS_B input. Gain & Offset change at the pixel rate:* **1st line: Gain & Offset = R,G,B,G,R,G,B,...* *2nd line: Gain & Offset = B,G,R,G,B,G,R,…* *repeat…* ** state of the first line after a write to this register*

Table 2: Configuration Register Parameters (Continued)

Parameter (Address)	Control Bits						Result	
Red, Green and Blue Offset DAC Settings (1, 2 & 3)								
Offset Polarity (1,2 & 3)	B5 0 1	Positive Offset Negative Offset						
Offset Value (1,2 & 3)	B4(MSB)	B3	B2	B1	B0(LSB)	LM9810: Offset = 5LSBs * Offset Value * PGA Gain LM9820: Offset = 20LSBs * Offset Value * PGA Gain		
Typical Offset Values (1,2 & 3)	B5 (SIGN)	B4 (MSB)	B3	B2	B1	B0 (LSB)	Typical Offset (with PGA Gain = 1)	
							LM9810 LSBs	LM9820 LSBs
	0	0	0	0	0	0	0.00	0.00
	0	0	0	0	0	1	+5	+20
	0	0	0	0	1	0	+10	+40
	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
	0	1	1	1	1	0	+150	+600
	0	1	1	1	1	1	+155	+620
	1	0	0	0	0	0	0	0
	1	0	0	0	0	1	-5	-20
	1	0	0	0	1	0	-10	-40
	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
	1	1	1	1	1	0	-150	-600
	1	1	1	1	1	1	-155	-620
Red, Green and Blue Gain Settings (4,5 & 6)								
Boost Gain Enable (4,5 & 6)	B5 0 1	Boost Gain = 1V/V Boost Gain = 3V/V						
PGA Gain Value (4,5 & 6)	B4	B3	B2	B1	B0	PGA Gain (V/V) =.933 + 0.0667 * (PGA Gain Value)		
Gain (4,5 & 6)	Gain = Boost Gain * PGA Gain							
Typical Gain Values (4, 5 & 6)	B5 (x3)	B4 (MSB)	B3	B2	B1	B0 (LSB)	Typical Gain (V/V)	
	0	0	0	0	0	0	0.93	
	0	0	0	0	0	1	1.00	
	0	0	0	0	1	0	1.13	
	• • •	• • •	• • •	• • •	• • •	• • •	• • •	
	0	1	1	1	0	1	2.87	
	0	1	1	1	1	0	2.93	
	0	1	1	1	1	1	3.00	
	• • •	• • •	• • •	• • •	• • •	• • •	• • •	
	1	0	0	0	0	0	2.79	
	1	0	0	0	0	1	3.00	
	1	0	0	0	1	0	3.20	
	• • •	• • •	• • •	• • •	• • •	• • •	• • •	
	1	1	1	1	0	1	8.60	
	1	1	1	1	1	0	8.80	
	1	1	1	1	1	1	9.00	

Table 2: Configuration Register Parameters (Continued)

Parameter (Address)	Control Bits					Result
Production Test and Power Down (7)						
Production Test (7)	B5	B4	B3	B2	B1	Should all be set to zero for normal operation
Power Down Enable (7)	B0 0 1	Normal Operation Power Down				

Applications Information

1.0 Programming the LM9810/20

1.1 Writing to the Configuration Register

When NewLine is high, D2, D1 & D0 act as a serial interface for writing to the configuration registers. D2 is the input serial clock (SCLK), D0 is the input data pin (SDI), and D1 is the latch and shift enable signal (Latch). When D1(Latch) is low, serial data is shifted into D0(SDI), and must be valid on each rising edge of D2(SCLK). Three register address bits followed by six data bits should be shifted into D0(SDI), MSB first. When D1(Latch) transitions from low to high, the last 6 data bits will be stored into the configuration register addressed by the previous 3 address bits (as shown in Diagram 3). D1(Latch) must remain high for at least 3 cycles of the serial clock on D2(SCLK) to write to the configuration register.

1.2 CDS Mode

The LM9810/20 uses a high-performance CDS (Correlated Double Sampling) circuit to remove many sources of noise and error from the CCD signal. It also supports CIS image sensors with a single sampling mode.

Figure 1 shows the output stage of a typical CCD and the resulting output waveform:

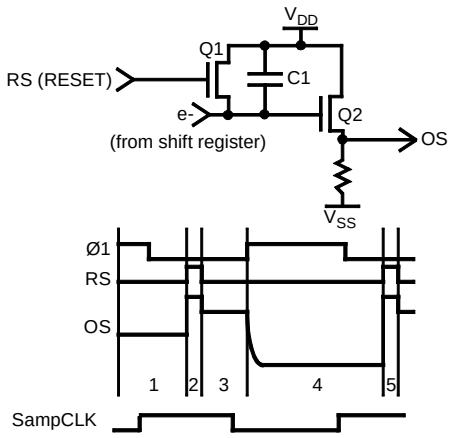


Figure 1: CDS

Capacitor C1 converts the electrons coming from the CCD's shift register to an analog voltage. The source follower output stage (Q2) buffers this voltage before it leaves the CCD. Q1 resets the voltage across capacitor C1 between pixels at intervals 2 and 5. When Q1 is on, the output signal (OS) is at its most positive voltage. After Q1 turns off (period 3), the OS level represents the residual voltage across C1 ($V_{RESIDUAL}$). $V_{RESIDUAL}$ includes charge injection from Q1, thermal noise from the ON resistance of Q1, and other sources of error. When the shift register clock (Ø1) makes a low to high transition (period 4), the electrons from the next pixel flow into C1. The charge across C1 now contains the voltage proportional to the number of electrons plus $V_{RESIDUAL}$, an error term. If OS is sampled at the end of period 3 and that voltage is subtracted from the OS at the end of period 4, the $V_{RESIDUAL}$ term is canceled and the noise on the signal is reduced ($[V_{SIGNAL}+V_{RESIDUAL}]-V_{RESIDUAL} = V_{SIGNAL}$). This is the principal of Correlated Double Sampling.

If the LM9810/20 is programmed for correlated double sampling (bit B5 of register 0 is cleared), then the falling edge of SampCLK should occur toward the end of period 3 and the rising edge of SampCLK should occur towards the end of period 4. While SampCLK is high, the Reference level ($V_{RESIDUAL}$) is sampled, and it is held at the falling edge of SampCLK. While SampCLK is low, the signal level ($V_{SIGNAL}+ V_{RESIDUAL}$) is sampled and it is held at the rising edge of SampCLK. The output from the sampler is the potential difference between the two samples, or V_{SIGNAL}.

1.3 CIS Mode

The LM9810/20 supports CIS (Contact Image Sensor) devices by offering a sampling mode for capturing positive going signals, as opposed to the CCD's negative going signal. The output signal of a CIS sensor (Figure 2) differs from a CCD signal in two primary ways: its output increases with increasing signal strength, and it does not usually have a reference level as an integral part of the output waveform of every pixel.

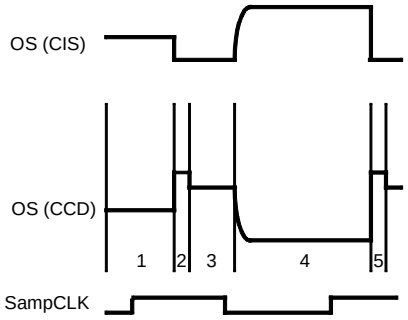


Figure 2: CIS

When the LM9810/20 is in CIS mode (Register 0, B5=1), it uses either V_{REF+} or V_{REF-} depending on the signal polarity setting (B4 of the Sampling and Color Mode register) as the reference (or black) voltage for each pixel. If the signal polarity is set to one, then V_{REF-} will be held on the falling edge of SampCLK and the OS signal will be held on the rising edge of SampCLK. If it is set to zero, then V_{REF+} will be held on the falling edge of SampCLK and the OS signal will be held on the rising edge of SampCLK. The rising edge of SampCLK should occur near the end of period 4, and at least 50ns after the falling edge of SampCLK.

1.4 Multiplexer/Channel Switching

The offset and gain settings automatically switch after each ADC conversion according to the color mode setting in the Sampler and Color Mode register (register 0). For example, if the color mode (bits B2,B1 & B0) is set to 001, the offset and gain will alternately switch between the R, G and B settings after each conversion. The input multiplexer never changes during a line, but if the color mode is set to Line Rate Color (000), the mux will automatically switch after each new line.

The offset and gain settings will always start with the first channel of the programmed mode after a falling edge on NewLine. For

example, the R offset and gain settings will be used for the first conversion following a falling edge on NewLine if the color mode is set to Single Input Color (001).

For the Single Input Color, Bayer and Green Stripe modes, the mux will always connect the OS_B input to the sampler. The offset and gain settings will alternate values every pixel according to the order indicated by the Sampler and Color Mode register (see Table 2). The first falling edge of NewLine following a write to the Sampler and Color Mode register will ready the offset and gain to cycle through the colors of the first line of the programmed color mode. Each subsequent falling edge of NewLine will switch the offset and gain settings to the first color of the next line. The LM9810/20's unused OS inputs should not be left unconnected. All three OS inputs should be tied together on the LM9810/20 side of the clamp capacitor (see Figure 3).

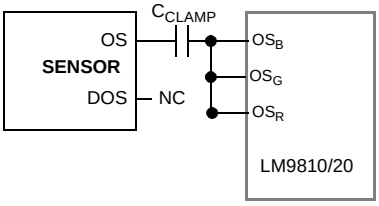


Figure 3: OS Connections for single output sensors

For the Line Rate Color mode, the mux will cycle through the OS_R, OS_G and OS_B inputs after each falling edge of NewLine. The R, G and B offset & gain settings will be used when the mux is set to the OS_R, OS_G and OS_B input, respectively. OS_R and the R offset & gain settings will always be used on the first line following a write register 0.

1.5 Data Latency

The latency through the LM9810/20 is 8 SampCLK periods plus one MCLK period. The data output on D5 - D0 (MSBs b11 - b6 or b9 - b4) represents data whose reference signal was sampled 8 tSampCLK + tMCLK + tSampSU earlier (see Diagram 1).

1.6 Programmable Gain

The output of the Sampler drives the input of the x3 Boost gain stage. The gain of the x3 Boost gain is 3V/V if bit B5 of the current color's gain register (registers 4,5, and 6) is set, or 1V/V if bit B5 is cleared. The output of the x3 gain stage is the input to the offset DAC and the output of the offset DAC is the input to the PGA (Programmable Gain Amplifier). The PGA provides 5 bits of gain correction over a 0.93V/V to 3V/V (-0.6 to 9.5dB) range. The x3 Boost gain stage and the PGA can be combined for an overall gain range of .93V/V to 9.0V/V (-.6 to 19dB). The gain setting for each color (registers 4, 5 and 6) should be set during calibration to bring the maximum amplitude of the strongest pixel to a level just below the desired maximum output from the ADC. The PGA gain is determined by the following equation:

$$\text{PGA Gain}\left(\frac{V}{V}\right) = 0.933 + .0667\ (\text{value in bits B4-B0})$$

Equation 1: PGA Gain

If the x3 Boost gain is enabled then the overall signal gain will be three times the PGA gain.

1.7 Offset DAC

The Offset DAC removes the DC offsets generated by the sensor and the LM9810/20's analog signal chain (see section 1.7.1, Internal Offsets). The DAC value for each color (registers 1,2 and 3) should be set during calibration to the lowest value that still results in an ADC output code greater than zero for all the pixels when scanning a black line. With a PGA gain of 1V/V, each LSB of the offset DAC typically adds the equivalent of 5 LM9810 LSBs or 20 LM9820 LSBs, providing a total offset adjustment range of ±150 LM9810 LSBs or ±590 LM9820 LSBs. The Offset DAC's output voltage is given by:

$$V_{DAC} = 9.75\text{mV} \cdot (\text{value in B4 - B0})$$

Equation 2: Offset DAC Output Voltage

In terms of output codes, the offset is given by:

$$\text{Offset} = 5\text{LSBs} \cdot (\text{value in B4 - B0}) \cdot \text{PGA Gain}$$

Equation 3: LM9810 Offset Equation

$$\text{Offset} = 20\text{LSBs} \cdot (\text{value in B4 - B0}) \cdot \text{PGA Gain}$$

Equation 4: LM9820 Offset Equation

The offset is positive if bit B5 is cleared and negative if B5 is set. Since the analog offset is added before the PGA gain, the value of the PGA gain must be considered when selecting the offset DAC values.

1.7.1 Internal Offsets

Figure 4 is a model of the LM9810/20's internal offsets. Equation 5 shows how to calculate the expected output code given the input voltage (VIN), the LM9810/20 internal offsets (VOS1, VOS2, VOS3), the programmed offset DAC voltage (VDAC), the programmed gains (GB, GPGA) and the analog channel gain constant C.

C is a constant that combines the gain error through the AFE, reference voltage variance, and analog voltage to digital code conversion into one constant. Ideally, C = 2048 codes/V (4096 codes/2V) for the LM9820 and 512 codes/V (1024 codes/2V) for the LM9810. Manufacturing tolerances widen the range of C (see Electrical Specifications).

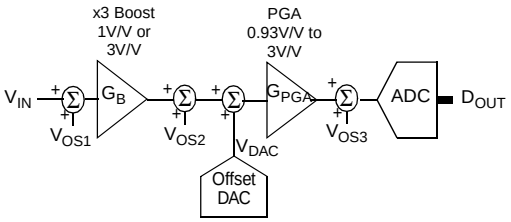


Figure 4: Internal Offset Model

$$D_{OUT} = (((V_{IN} + V_{OS1})G_B + V_{DAC} + V_{OS2})G_{PGA} + V_{OS1})C$$

Equation 5: Output code calculation with internal offsets

Equation 6 is a simplification of the output code calculation, neglecting the LM9810/20's internal offsets.

$$D_{OUT} = (V_{IN}G_B + V_{DAC})G_{PGA}C$$

Equation 6: Simplified output code calculation

1.8 Power Down Mode

Setting the Power Down (bit B0 of register 7) puts the device in a low power standby mode. The analog sections are turned off to conserve power. The digital logic will continue to operate if MCLK continues, so for minimum power dissipation MCLK should be stopped when the LM9810/20 enters the Power Down mode. Recovery from Power Down typically takes 50µs (the time required for the reference voltages to settle to 0.5 LSB accuracy).

2.0 Clamping

To perform a DC restore across the AC coupling capacitors at the beginning of every line, the LM9810/20 implements a clamping function. When NewLine is high and SampCLK is low, all three OS inputs will be connected to either V_{REF+} or V_{REF-}, depending on B4 of the Sampling and Color Mode register. If B4 is set to one (positive signal polarity), then the OS inputs will be connected to V_{REF-}. If B4 is set to zero (negative signal polarity), then they will be connected to V_{REF+}.

2.1 Clamp Capacitor Selection

This section explains how to select appropriate clamp capacitor values.

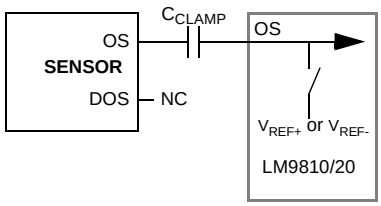


Figure 5: OS Clamp Capacitor and Internal Clamp

The output signal of many sensors rides on a DC offset (greater than 5V for many CCDs) which is incompatible with the LM9810/20's 5V operation. To eliminate this offset without resorting to additional higher voltage components, the output of the sensor is AC coupled to the LM9810/20 through a DC blocking capacitor, C_{CLAMP} The sensor's DOS output, if available, is not used. The value of this capacitor is determined by the leakage current of the LM9810/20's OS input and the output impedance of the sensor. The leakage through the OS input determines how quickly the capacitor value will drift from the clamp value of V_{REF+} or V_{REF-}, which then determines how many pixels can be processed before the droop causes errors in the conversion (±0.1V is the recommended limit for CDS operation). The output impedance of the sensor determines how quickly the capacitor can be charged to the clamp value during the black reference period at the beginning of every line.

The minimum clamp capacitor value is determined by the maximum droop the LM9810/20 can tolerate while converting one sensor line. The minimum clamp capacitor value is much smaller for CDS mode applications than it is for CIS mode applications. The LM9810/20 input leakage current is considerably less when the LM9810/20 is operating in CDS mode. In CDS mode, the LM9810/20 leakage current should be no more than 20nA. With CDS disabled, which will likely be the case when CIS sensors are used, the LM9810/20 leakage current can be as high as 25uA at the maximum conversion rate.

2.1.1 CDS mode Minimum Clamp Capacitor Calculation:

The following equation takes the maximum leakage current into the OS input, the maximum allowable droop, the number of pixels on the sensor, and the pixel conversion rate, $f_{SampCLK}$, and provides the minimum clamp capacitor value:

$$C_{CLAMP\ MIN} = \frac{i}{dV}dt$$
$$= \frac{\text{leakage current (A)}}{\text{max droop(V)}}\frac{\text{number of pixels}}{f_{SampCLK}}$$

Equation 7: CDS mode $C_{CLAMP\ MIN}$ Calculation

For example, if the OS input leakage current is 20nA worst-case, the sensor has 2700 active pixels, the conversion rate is 2MHz ($t_{SampCLK}$ = 500ns), and the max droop desired is 0.1V, the minimum clamp capacitor value is:

$$C_{CLAMP\ MIN} = \frac{20nA}{0.1V}\frac{2700}{2MHz}$$
$$= 270pF$$

Equation 8: CDS mode $C_{CLAMP\ MIN}$ Example

2.1.2 CIS mode Minimum Clamp Capacitor Calculation:

If CDS is disabled, then the maximum LM9810/20 OS input leakage current can be calculated from:

$$I_{leakage} = V_{SAT}f_{SampCLK}C_{SAMP}$$

Equation 9: CIS mode Input Leakage Current Calculation

where VSAT is the peak pixel signal swing of the CIS OS output and CSAMP is the capacitance of the LM9810/20's internal sampling capacitor (2pF). Inserting this into Equation 7 results in:

$$C_{CLAMP\ MIN} = \frac{i}{dV}dt$$
$$= \frac{V_{SAT}}{t_{SampCLK}}C_{SAMP}\frac{t_{SampCLK}}{\text{max droop(V)}}\text{num pixels}$$

Equation 10: CIS mode $C_{CLAMP\ MIN}$ Calculation

with CSAMP equal to 2pF and VSAT equal to 2V (the LM9810/20's maximum input signal), then Equation 10 reduces to:

$$C_{CLAMP\ MIN} = \frac{4p(F)(V)}{\text{max droop(V)}}\text{num pixels}$$

Equation 11: CIS mode $C_{CLAMP\ MIN}$ Calculation

In CIS mode (CDS disabled), the max droop limit must be much more carefully chosen, since any change in the clamp capacitor's DC value will affect the LM9810/20's conversion results. If a droop of one 10 bit LSB across a line is considered acceptable, then the allowed droop voltage is calculated as: 2V/1024, or

approximately 2mV. If there are 2700 active pixels on a line then:

$$C_{CLAMP\ MIN} = \frac{4p(F)(V)}{2mV}2700 = 5.4uF$$

Equation 12: CIS mode $C_{CLAMP\ MIN}$ Calculation Example

2.1.3 Maximum Clamp Capacitor Calculation:

The maximum size of the clamp capacitor is determined by the amount of time available to charge it to the desired value during the optical black portion of the sensor output. The internal clamp is on when NewLine is high and SampCLK is low. If the applied SampCLK is low for half its cycle, then the available charge time per line can be calculated using:

$$t_{CLAMP} = \frac{\text{Number of optical black pixels}}{2f_{SampCLK}}$$

Equation 13: Clamp Time Per Line Calculation

For example, if a sensor has 18 black reference pixels and $f_{SampCLK}$ is 2MHz with a 50% duty cycle, then t_{CLAMP} is 4.5µs.

The following equation takes the number of optical black pixels, the amount of time (per pixel) that the clamp is closed, the sensor's output impedance, and the desired accuracy of the final clamp voltage and provides the maximum clamp capacitor value that allows the clamp capacitor to settle to the desired accuracy within a single line:

$$C_{CLAMP\ MAX} = \frac{t}{R}\frac{1}{\ln(accuracy)} = \frac{t_{CLAMP}}{R_{CLAMP}}\frac{1}{\ln(accuracy)}$$

Equation 14: $C_{CLAMP\ MAX}$ for a single line of charge time

Where t_{CLAMP} is the amount of time (per line) that the clamp is on, R_{CLAMP} is the output impedance of the CCD plus 50Ω for the LM9810/20's internal clamp switch, and accuracy is the ratio of the worst-case initial capacitor voltage to the desired final capacitor voltage. If t_{CLAMP} is 4.5µs, the output impedance of the sensor is 1500Ω, the worst case voltage change required across the capacitor (before the first line) is 5V, and the desired accuracy after clamping is to within 0.1V (accuracy = 5/0.1 = 50), then:

$$C_{CLAMP\ MAX} = \frac{4.5\mu s}{1550\Omega}\frac{1}{\ln(50)} = 728pF$$

Equation 15: $C_{CLAMP\ MAX}$ Example

The final value for C_{CLAMP} should be less than or equal to $C_{CLAMP\ MAX}$, but no less than $C_{CLAMP\ MIN}$.

In some cases, depending primarily on the choice of sensor, $C_{CLAMP\ MAX}$ may actually be *less* than $C_{CLAMP\ MIN}$, meaning that the capacitor can not be charged to its final voltage during the black pixels at the beginning of a line and hold it's voltage without drooping for the duration of that line. This is usually not a problem because in most applications the sensor is clocked continuously as soon as power is applied. In this case, a larger capacitor can be used (guaranteeing that the $C_{CLAMP\ MIN}$ requirement is met), and the final clamp voltage is forced across the capacitor over multiple lines. This equation calculates how many lines are required before the capacitor settles to the desired accuracy:

$$lines = \left(R_{CLAMP}\frac{C_{CLAMP}}{t_{CLAMP}}\right)\ln\left(\frac{\text{Initial Error Voltage}}{\text{Final Error Voltage}}\right)$$

Equation 16: Number of Lines Required for Clamping

Using the values shown before and a clamp capacitor value of 0.01µF, this works out to be:

$$lines = \left(1550\frac{0.01\mu F}{4.5\mu s}\right)\ln\left(\frac{5V}{0.1V}\right) = 13.5\ lines$$

Equation 17: Clamping Lines Required Example

In this example, a 0.01µF capacitor takes 14 lines after power-up to charge to its final value. On subsequent lines, the only error will be the droop across a single line which should be significantly less than the initial error. **If the LM9810/20 is operating in CDS mode and multiple lines are used to charge up the clamping capacitors after power-up, then a clamp capacitor value of 0.01µF should be significantly greater than the calculated $C_{CLAMP\ MIN}$ value and can virtually always be used.**

If the LM9810/20 is operating in CIS mode, then significantly larger clamp capacitors must be used. Fortunately, the output impedance of most CIS sensors is significantly smaller than the output impedance of CCD sensors, and R_{CLAMP} will be dominated by the 50Ω from the LM9810/20's internal clamp switch. With a smaller R_{CLAMP} value, the clamp capacitors will charge faster.

3.0 Performance Considerations

3.1 Power Supply

The LM9810/20 should be powered by a single +5V source. The analog supplies (VA) and the digital supply (VD) are brought out individually to allow separate bypassing for each supply input. They should *not* be powered by two or more different supplies.

In systems with separate analog and digital +5V supplies, all the supply pins of the LM9810/20 should be powered by the analog +5V supply. Each supply input should be bypassed to its respective ground with a 0.1µF capacitor located as close as possible to the supply input pin. A single 10µF tantalum capacitor should be placed near the VA supply pin to provide low frequency bypassing.

To minimize noise, keep the LM9810/20 and all analog components as far as possible from noise generators, such as switching power supplies and high frequency digital busses. If possible, isolate all the analog components and signals (OS, reference inputs and outputs, VA, AGND) on an analog ground plane, separate from the digital ground plane. The two ground planes should be tied together at a single point, preferably the point where the power supply enters the PCB.

3.2 SampCLK Timing

SampCLK is used to time the stages of the LM9810/20's sampler, offset DAC and programmable gain amplifier. To allow for optimum input signal sampling times, SampCLK may be applied asynchronously to MCLK. The LM9810/20's ADC is synchronized with the its AFE (including the sampler, the offset DAC and the PGA) by MCLK.

The LM9810/20's internal ADC clock is created through a combi-

nation of the applied SampCLK and MCLK signals. MCLK is used to synchronize the applied SampCLK signal. The internal ADC clock will go low after the falling edge of SampCLK is clocked by a rising of MCLK. The ADC clock will stay low for two MCLK cycles and then go high. It will stay high until the next falling edge of SampCLK is clocked by MCLK. Figure 6 illustrates this SampCLK, MCLK, and ADC clock timing relationship.

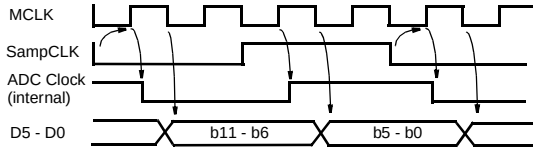


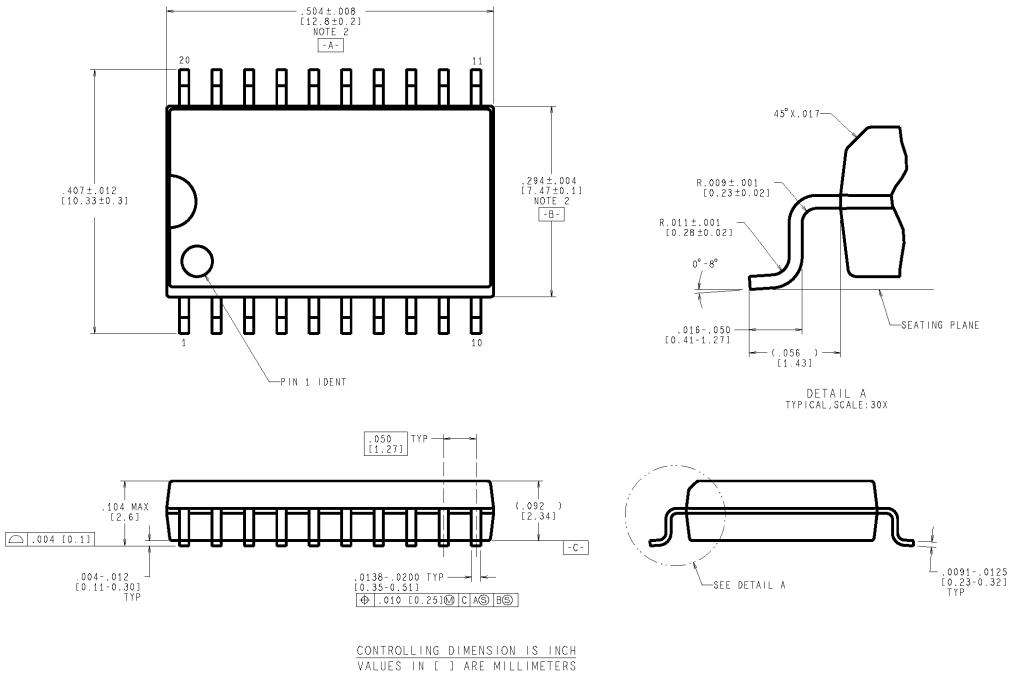
Figure 6: LM9810/20 Relative Event Timing

The LM9810/20 is a densely designed, mixed-signal, monolithic semiconductor. In creating the timing for the LM9810/20, it must be considered that internal events, such as ADC sampling, and output data bus switching can potentially affect coincident events such as input signal sampling or offset DAC settling. One event can interfere with another by coupling noise on shared resources such as the supply lines, internal voltage references, or the silicon substrate.

To optimize the performance of the LM9810/20, SampCLK should be timed so that the input signal hold times do not coincide with output data switching and ADC clock transitions. In other words, the rising and falling edges of SampCLK should not be placed close to ADC clock edges or to output data transitions. SampCLK edges should be at least 20ns away from ADC clock edges to avoid interference between the ADC and the sampler. SampCLK edges should also be placed at least 40ns after output data transition times to avoid transition noise coupling.

Figure 6 is an example of SampCLK timing that will meet these requirements at the maximum MCLK frequency of 24MHz. In diagram 6, SampCLK transitions occur on MCLK falling edges which will keep them more than 20ns away from ADC transitions, and 40ns after output data transitions.

Physical Dimensions inches (millimeters)



NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH TO BE 200 MICROINCHES/ 5.08 MICROMETERS MINIMUM LEAD/TIN(SOLDER) ON COPPER.
2. DIMENSION DOES NOT INCLUDE MOLD FLASH.
3. REFERENCE JEDEC REGISTRATION MS-013, VARIATION AC, DATED MAY 1990.

20 pin (.300” Wide) Molded Small Outline Package

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: a49 (0) 180-530 85 86
Email: europe.support @ nsc.com
Deutsch Tel: + 49 (0) 180-530 85 85
English Tel: + 49 (0) 180-532 78 32
Francais Tel: + 49 (0) 180-532 93 58
Italiano Tel: + 49 (0) 180-534 16 80

National Semiconductor Hong Kong
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Ltd. Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408