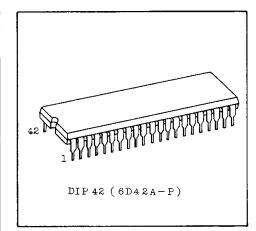
#### TC5070P/TC5071P/TC5072P 6 DIGIT UNIVERSAL COUNTER

TC5070P/TC5071P/TC5072P are 6-digit universal counter containing 6-digit memory register in addition to functions of up/down counting, data presetting, zero suppress, and latch. The counted contents are output in BCD and seven segment dynamically stepwise from most significant digit in synchronization with input of SCAN. The seven-segment output can directly drive the common cathode type LED. In addition to CARRY and ZERO outputs, these counter are provided with EQUAL output, permitting a wide range of applications such as for measuring instruments, timers, etc. Maximum counting value TC5070P 9999999 COUNTER

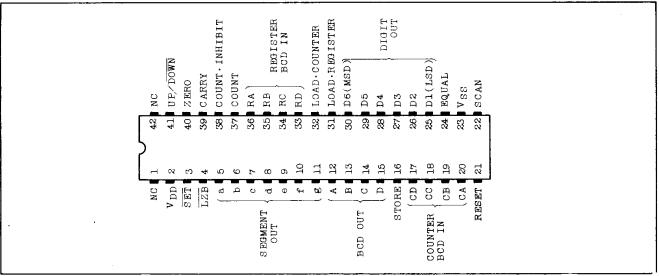
TC5070P 999999 COUNTER TC5071P 995959 TIMER TC5072P 595999 TIMER



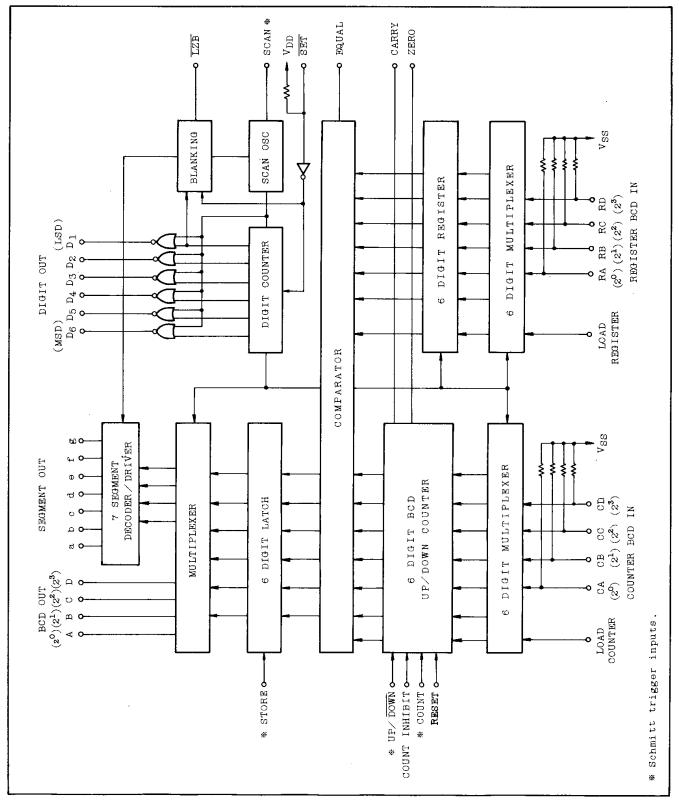
#### ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V <sub>DD</sub>	$V_{SS}-0.5 \sim V_{SS}+10$	v
Input Voltage	VIN	Vss-0.5~VDD+0.5	v
Output Voltage	VOUT	V <sub>SS</sub> -0.5~V <sub>DD</sub> +0.5	v
DC Input Current	IIN	±10	mA
Power Dissipation	PD	300	m₩
Storage Temperature Range	Tstg	-65~150	°C
Lead Temp./Time	T <sub>sol</sub>	260°C • 10sec	

#### PIN ASSIGNMENT



BLOCK DIAGRAM



# TC5070P, TC5071P, TC5072P

## DESCRIPTION OF PIN FUNCTION

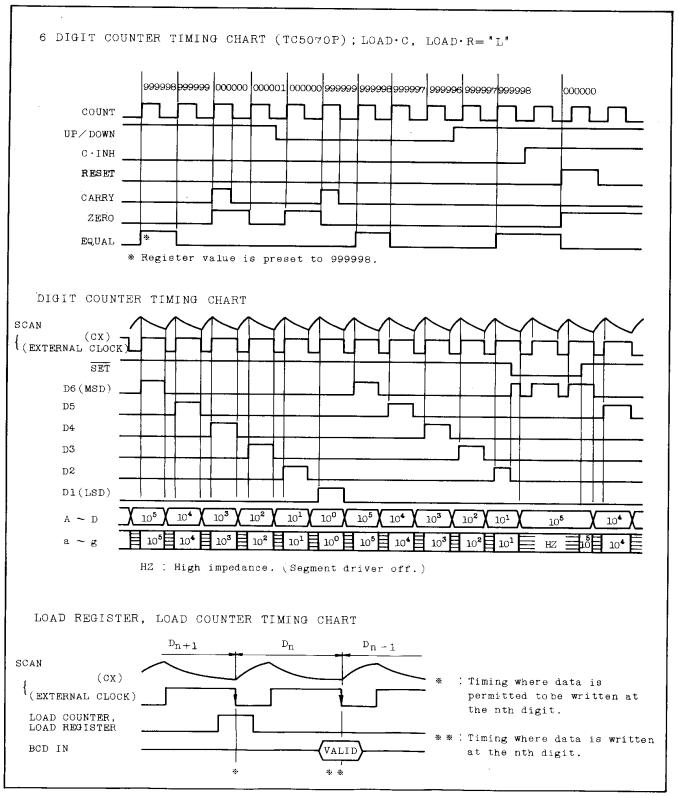
PIN No.	SYMBOL	FUNCTION								
1	NC	No connection								
2	V <sub>DD</sub>	VDD power supply (3-8V)								
3	SET	At "L" level, the digit counter is reset, and D6 (MSD) only provide. The Segment-out changes to the blanking state. At "H" level, normal display operation.								
4	LZB	"H" No zero blanking								
-	220	"L" Leading zero blanking in the higher order 5 digits.								
5	a	· · · · · · · · · · · · · · · · · · ·								
6	Ъ									
7	c	Fach pin is now a compart output of 6 digit counter. The cutru								
8	d	Each pin is seven segment output of 6-digit counter. The output is synchronized with the digit-out and is provided stepwise								
9	e	from the most significant digit.								
10	f									
11	g									
12	А	Each pin is BCD output of 6-digit counter. The output is synchronized with the digit-out and is provided stepwise from the most significant digit. When SET input is at "L" level, the most significant digit data								
13	В									
14	С									
15	D	is provided.								
16	STORE	"H" At positive edge of the STORE input, the contents of the counter are latched.								
10	O TONE	"L" The contents of the counter are straight transferred to the miltiplexer.								
17	CD									
18	СС	BCD input at the time when data are preset to the 6-digit								
19	СВ	counter. (With the LOAD COUNTER input at "H" level.)								
20	CA	(with the bond booklink input at in rever.)								
21	RESET	At "H" level, the 6-digit counter is reset, and the contents of the counter become ALL "O". ZERO output become at "H" level.								
22	SCAN	Auto scan oscillator is operated by connecting a capacitor (2000-20000pF) between No.22 (SCAN) and No.23 (VSS) terminals. External scan oscillator may also be used to drive the scan input.								
23	V <sub>SS</sub>	GND (OV)								

### DESCRIPTION OF PIN FUNCTION (Cont'd)

PIN No.	SYMBOL	FUNCTION								
24	EQUAL	When the contents of the 6-digit register set by the input of RA, RB, RC, and RD coincide with the contents of 6-digit counter, EQUAL output is provided at "H" level. Even if both the contents coincide each other during setting by the inputs of LOAD REGISTER and LOAD COUNTER, the output is inhibited and "L" level remains unchanged.								
25	D1(LSD)									
26	D2	These are the outputs to display the digits of segment out and BCD-out.								
27	D3	When SET input reaches "L" level, the digit counter is reset								
28	D4	and D6 (MSD) only is provided. When SET input rises at "H" level, the output is provided in the order of D5, D4in								
29	D5	ynchronization with the SCAN clock.								
30	D6 (MSD)									
31	LOAD • REGISTER	"H" RA~RD input is set to 6-digit register.								
51	(LOAD.R)	"L" Write operation to the register is inhibited.								
32	LOAD · COUNTER	"H" CA~CD input is preset to the 6-digit counter.								
52	(LOAD·C)	"L" Write operation to the counter is inhibited.								
33	RD									
34	RC	BCD input at the time when the data are set to the 6-digit								
35	RB	register. (With the LOAD REGISTER input at "H" level.)								
36	RA	(with the bond abording input at a fereit)								
37	COUNT	Clock input of 6-digit counter (Counting at the positive edge of clock)								
38	COUNT · INHIBIT	"H" No counting								
50	(C·INH)	"L" Counting								
39	CARRY	When the contents of counter have become "000000" at time of up-counting, CARRY output is provided at "H" level during this time from rise to fall of COUNT input. When the contents of counter have become "9999999" (for TC5070P). "995959" (for TC5071P), and "595999" (for TC5072P) at time of down-counting, CARRY output is also provided at "H" level during this time from rise and fall of COUNT input.								
40	ZERO	When the contents of counter have become "00000", ZERO is provided at "H" level. During presetting by the LOAD COUNTER input, output operation is inhibited and "L" level remains unchanged.								
41	UP/DOWN	"H" Up count.								
······································		"L" Down count.								
42	NC	No connection.								

# TC5070P, TC5071P, TC5072P

TIMING CHART



#### OPERATING CONSIDERATION

1.	COUNTER OPERATION
	Counting is stepped by the rise of clock when the clock is added to COUNT input at
	state of the inputs of LOAD·C, C·INH, and RESET at "L" level. At time of up-
	counting, CARRY and ZERO outputs are "H" level at "000000", and at time of down-
	counting, CARRY output is at "H" level at "9999999" (for TC5070P), "995959" (for
	TC5071P), and "595999: (for TC5072P).
	When CARRY output is at "H" level, CARRY output remain at "H" leve until COUNT
	input falls, even if RESET and LOAD·C inputs are changed to "H" level.
	For COUNT and UP/DOWN inputs is shaped schmitt trigger, COUNT and UP/DOWN inputs
	rarely miscounts if waveform is not sharp.
2.	COMPARATOR OPERATION

EQUAL output is provided at "H" level, when the contents of the counter coincide with the comparator value set by LOAD.R input. However, even if they concide each other during setting by LOAD.C and LOAD.R input, output operation is inhibited and "L" level remains unchanged.

3. LOAD COUNTER AND LOAD REGISTER OPERATIONS

When the data required to preset the counter or when the comprating value is required to set to the register, such operation is made by LOAD·C and LOAD·R input. The presetting of data to the counter is acquired by setting LOAD·C input to "H" level, synchronizing CA ~ CD input with the digit counter, and setting the digits one after another. For the purpose, the external circuits are required for timing of D6 ~ D1 output with CA ~ CD input. The comprator value can be set to the register in the same way. Load register operation is independently of counting operation; therfore, even during setting of the data to the register, counting can be performed. (See an example of input setting circuits.)

(Note) that normal operation is not acquired when the data exceeding the maximum counting value (for each digit) shown on page 1 for the individual items are set to the counter and register.

4. LATCH OPERATION

At STORE input is at "L" level, the contents of counter are straight transferred to the multiplexer, and the output indicates the contents of counter.

At STORE input is at "H" level, the indicating output remains unchanged although the count varies for the contents of counter are latched at the positive edge of

#### OPERATING CONSIDERATION (Cont'd)

STORE input. When STORE is turned to "L" level, the contents of counter at that time are provided. STORE input shape schmitt trigger.
5. DISPLAY OPERATION
At ITE input is at "L" level, the higher order 5 digits of SECMENT-OUT output are

At  $\overline{\text{LZB}}$  input is at "L" level, the higher order 5 digits of SEGMENT-OUT output are changed to the state of leading zero blanking.

At "H" level, the function of leading zero blanking is released.

At SET input is at "L" level, the SEGMENT-OUT output is changed to the state of blanking, and the digit counter is reset, and D6 (MSD) only is provided. At that time, the BCD-OUT output provided the data of the 6th digit. At "H" level, the DIGIT-OUT output provided in the order of D6, D5, D4, ... in synchronization with SCAN, and SEGMENT-OUT and CD-OUT output are also provided in synchronization.

Segment Display Format (Common Cathod type LED)

# $\begin{bmatrix} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 \sim 15 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 6 & 7 & 6 & 9 & 10 \sim 15 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 6 & 7 & 6 & 9 & 10 \sim 15 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 6 & 7 & 6 & 9 & 10 \sim 15 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 6 & 7 & 6 & 9 & 10 \sim 15 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 6 & 7 & 6 & 9 & 10 \sim 15 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 6 & 7 & 6 & 9 & 10 \sim 15 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 6 & 7 & 8 & 9 & 10 \sim 15 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 6 & 7 & 6 & 9 & 10 \sim 15 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 6 & 7 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 6 & 7 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 5 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 4 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 10 & 10 & 10 & 10 \\ \hline 1 & 2 & 3 & 10 & 10 & 10 & 10 \\ \hline 1 & 3 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 10 \\ \hline 1 & 1 & 10 & 10 & 10 & 10 & 1$

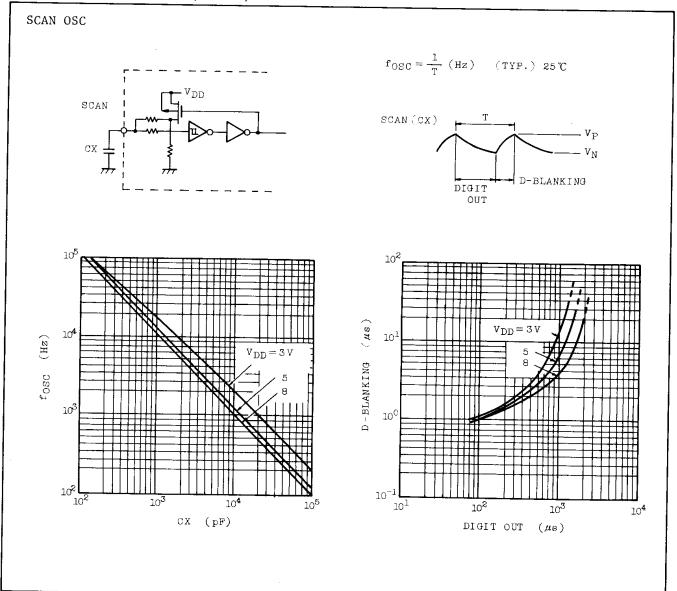
6. SCANNING OPERATION

AUTO SCAN operation can be performed by inserting a capacitor between the terminal SCAN and the terminal VSS. By adding an external clock to the terminal SCAN, MANUAL SCAN operation can be performed.

SCAN OSC actuates the digit counter, and at the AUTO SCAN operation, the digit blanking is applied to each DIGIT OUT for the T/150 period of one cycle (T) of SCAN OSC, therfore, can be prevented overlap of each DIGIT OUT. One cycle of DIGIT OUT is equal to 6 cycles of SCAN OSC.

SCAN signal synchronize with data signal setting by the LOAD REGISTER and/or LOAD COUNTER inputs. An external capacitor of 2000 to 20000pF is required for SCAN (CX).

(Note) BCD-OUT output may involve some hazards at the change of COUNT input and DIGIT-OUT output; However, such hazards do not hinder operation because they occur during the blanking hours for DIGIT-OUT and SEGMENT-OUT output.



## OPERATING CONSIDERATION (Cont'd)

# RECOMMENDED OPERATING CONDITIONS ( $v_{SS}=ov$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V <sub>DD</sub>		3	-	8	v
Input Voltage	VIN		0		V <sub>DD</sub>	v
Operating Temperature Range	Topr		-40	-	85	°C

CHARACTERISTIC	SYM-	TEST	<b>v</b> <sub>DD</sub>	-40	°C		25°C		85	5°C	UNIT
CHARACTERIDITE	BOL	CONDITION	(V)	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage (Except SEGMENT OUTPUT)	V <sub>OH</sub>	I <sub>OUT</sub>  <1#A VIN=VSS,VDD	5	4.95	-	4.95	5.00	-	4.95	-	
Low-Level Output Voltage (Except SEGMENT OUTPUT)	V <sub>OL</sub>	1 <sub>OUT</sub>  <1#A V <sub>IN</sub> =V <sub>SS</sub> ,V <sub>DD</sub>	5	_	0.05	-	0.00	0.05	-	0.05	v
High-Level Output Voltage (SEGMENT OUTPUT)	VOH	I <sub>OUT</sub>  <1#A V <sub>IN</sub> =V <sub>SS</sub> ,V <sub>DD</sub>	5	4.0	-	4.0	4.5	-	4.0	_	
Output High Current (A~D, EQ, CA, ZE OUTPUT)	IОН	V <sub>OH</sub> =4.6V V <sub>IN</sub> =V <sub>SS</sub> ,V <sub>DD</sub>	5	-0.2	_	-0.16	-0.8	-	-0.12	_	
Output High Current (D1~D6 OUTPUT)	IOH	V <sub>OH</sub> =4.2V V <sub>IN</sub> =V <sub>SS</sub> ,V <sub>DD</sub>	5	-0.75	_	-0.7	-1.5	-	-0.6	_	mA
Output Low Current (Except SEGMENT OUTPUT)	I <sub>OL</sub>	V <sub>OL</sub> =0.4V V <sub>IN</sub> =V <sub>SS</sub> ,V <sub>DD</sub>	5	0.52	_	0.44	1.2	-	0.36	_	
Output High Current (SEGMENT OUTPUT)		V <sub>OH</sub> =3.5V V <sub>IN</sub> =V <sub>SS</sub> ,V <sub>DD</sub>	5	-25	-	-25	-50	-	-20	-	
Input Low Voltage (Except Schmitt Trigger Input)	VIH	V <sub>OH</sub> =4.0V V <sub>OL</sub> =0.5V  I <sub>OUT</sub>  <1#A	5	3.5	_	3.5	2.75	-	3.5	_	v
Input High Voltage (Except Schmitt Trigger Input)	vIL	V <sub>OH</sub> =4.0V V <sub>OL</sub> =0.5V  I <sub>OUT</sub>   <1#A	5	-	1.5	-	2.15	1.5	_	1.5	
High-Level Input Current (Except Pull Up/ Down Resistance Input)	IIH	V <sub>IH</sub> =8V	8	-	0.3	-	10-5	0.3	-	1.0	μA

.

## STATIC ELECTRICAL CHARACTERISTICS ( $V_{SS}=0V$ )

CHARACTERISTIC	SYM-		VDD	-4	0°C		25°C		8	UNIT	
	BOL	CONDITION	(V)	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	UNII
Low-Level Input Current (Except Pull Up/ Down Resistance Input)	IIL	V <sub>IL</sub> =0V	8	-	-0.3	_	10-5	-0.3	-	-1.0	
High-Level Input Current (SET IN)	IIH	V <sub>IH</sub> =8V	8	-	5.0	-	-	5.0	-	5.0	
Low-Level Input Current (SET IN)	IIL	v <sup>IT</sup> =0N	8	-	-180	_	-70	-160	-	-140	μA
High-Level Input Current (CA~CD, RA~RD, SCAN IN)	IIH	V <sub>IH</sub> =8V	8	-	180	_	80	160	_	140	
Low-Level Input Current (CA~CD, RA~RD IN)	IIL	V <sub>IL</sub> =0V	8	-	-5.0		-	-5.0	_	-5.0	
Low-Level Input Current (SCAN IN)	IIL	ν <sup>1Γ</sup> =0Λ	5 8	-	-2.3 -3.6	-	-1.0 -1.6	-2.0 -3.2	-	-1.8 -2.8	mA
Output Leakage Current (SEGMENT OUT)	I <sub>DL</sub>	V <sub>OL</sub> =0V	8	-	-3.0	_	-10-4	-3.0	-	-1.5	μA
Quiescent Device Current		SCAN= $V_{DD}$ SET, CA~CD, RA~RD OPEN	5 8	-	750 1500		180 250	500 1000	-	1000 2000	μA

STATIC ELECTRICAL CHARACTERISTICS (V<sub>SS</sub>=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t <sub>TLH</sub>	SEGMENT OUT ( $R_L=1k\Omega$ )	-	70	200	
(Low to High)	t <sub>TLH</sub>	OTHER OUT	-	100	400	
Output Transition Time (High to Low)	t <sub>THL</sub>	Except SEGMENT OUT	-	70	200	
	t <sub>pLH</sub> , t <sub>pHL</sub>	COUNT-BCD, SEGMENT OUT (RL=1kΩ)		750	1500	
	t <sub>pLH</sub> , t <sub>pHL</sub>	COUNT-CARRY OUT	-	150	400	]
Propagation Delay Time	tpLH, tpHL	COUNT-ZERO OUT	-	200	400	ns
	t <sub>pLH</sub> , t <sub>pHL</sub>	COUNT-EQUAL OUT	-	270	500	
	t <sub>pLH</sub> , t <sub>pHL</sub>	SCAN-DIGIT OUT	_	250	500	
	tpLH, tpHL	SCAN-BCD OUT		750	1500	
Propagation Delay Time	t <sub>pLH</sub>	SCAN-SEGMENT OUT $(R_L=1k\Omega)$	-	500	1000	
riopagación beily rime	t <sub>pHL</sub>	SCAN-SEGMENT OUT $(R_L=1k\Omega)$	-	300	700	]
	f <sub>CL</sub> -1	COUNT IN *	2.0	4.0	-	MHz
Max. Clock Frequency	f <sub>CL</sub> -2		1.0	1.6	[	
	f <sub>CL</sub>	SCAN IN	0.5	1.0	-	1
Min. Pulse Width	tw	RESET IN	-	250	500	
nin. ruise widen	tw	STORE IN	-	80	160	1
	t <sub>SU</sub>	COUNT-STORE	-	70	150	1
	t <sub>SU</sub>	COUNT-UP/DOWN	-	230	500	1
Min. Set-up Time	t <sub>SU</sub>	STORE-CLEAR	-	130	300	1
min. Det up rime	t <sub>SU</sub>	COUNT-C · IN	-	0	100	1
	t <sub>SU</sub>	SCAN IN-LOAD.C, LOAD.R	-	-40	50	ns
	t <sub>SU</sub>	SCAN IN-BCDIN	-	200	450	
	t <sub>H</sub>	COUNT-UP/DOWN	-	40	150	1
Min. Hold Time	t <sub>H</sub>	SCAN IN-LOAD·C, LOAD·R	-	70	200	1
	t <sub>H</sub>	SCAN IN-BCDIN	-	140	300	
Min. Removal Time	trem	COUNT-RESET	-	60	150	1
Max. Input Rise/Fall	t <sub>rCL</sub>	Except Schmitt Trigger	20	_	-	
Time	t <sub>rCL</sub>	Except Schmitt Trigger Input	20	_	-	μs
Positive Trigger Threshold Voltage	VP			3.0	4.0	<u> </u>
Negative Trigger Threshold Voltage	VN		1.0	1.8	-	V
Hysteresis Voltage	V <sub>H</sub>		0.5	1.2	-	

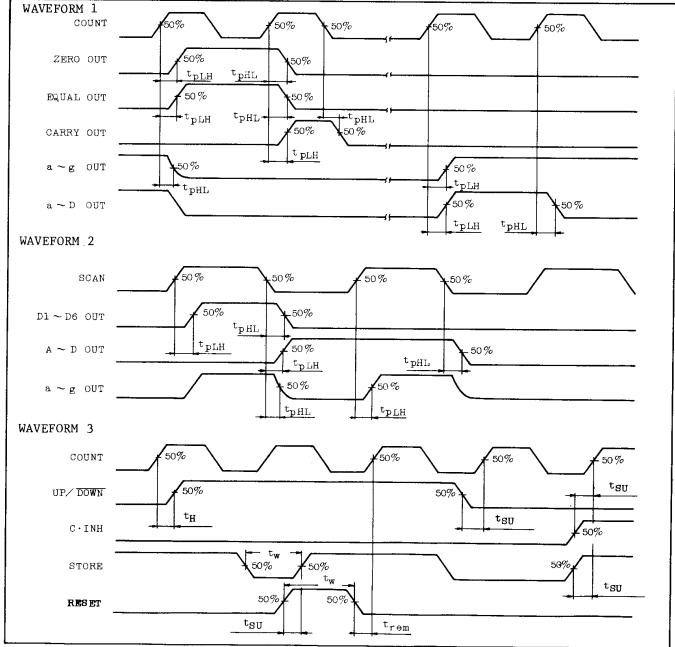
DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, VDD=5.0V, VSS=0V, CL=50pF)

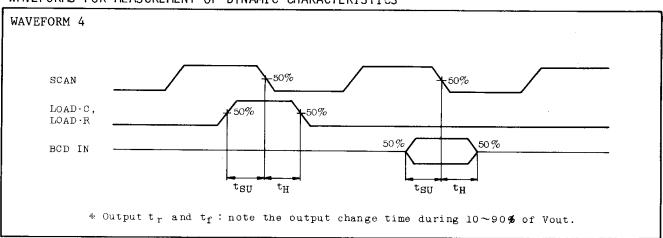
	· · · · · · · · · · · · · · · · · · ·	1a-25 C, VDD-5.0V, VSS-0V,	<u></u>			
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Device Current	IDD	COUNT IN = H & L	-	250	-	μA
$(C_X=2000 \sim 20000 \text{pF})$		COUNT IN = $1 \text{ MHz}$	_	650	-	μ11
Input Capacitance	CIN	Except SCAN IN	-	5.0	7.5	pF

DYNAMIC ELECTRICAL CAHRACTERISTICS (Ta=25°C, VDD=5.0V, VSS=0V, CL=50pF)

\* The count operation can respond as far as  $f_{\rm CL}-1,$  and CARRY, EQUAL, and ZERO outputs can respond as far as  $f_{\rm CL}-2.$ 

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS





#### WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

#### TYPICAL INPUT SELECT CIRCUIT

