

# DATA SHEET

## **74LVC244A/74LVCH244A**

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)title

Product specification  
Supersedes data of 1996 Sep 06  
IC24 Data Handbook

1998 May 20

# Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

## 74LVC244A 74LVCH244A

### FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when  $V_{CC} = 0V$
- Bushold on all data inputs (74LVCH244A only)

### DESCRIPTION

The 74LVC244A/74LVCH244A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC244A/74LVCH244A is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs  $1\overline{OE}$  and  $2\overline{OE}$ . A HIGH on  $n\overline{OE}$  causes the outputs to assume a high impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

The '244' is functionally identical to the '240', but the '240' has non-inverting outputs.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay $1A_n$ to $1Y_n$ ; $2A_n$ to $2Y_n$	$C_L = 50pF$ $V_{CC} = 3.3V$	3.5	ns
$C_I$	Input capacitance		4.4	pF
$C_{PD}$	Power dissipation capacitance per buffer	Notes 1 and 2	22.6	pF

#### NOTE:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.
- The condition is  $V_I = GND$  to  $V_{CC}$

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	-40°C to +85°C	74LVC244A D	74LVC244A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	-40°C to +85°C	74LVC244A DB	74LVC244A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	-40°C to +85°C	74LVC244A PW	7LVC244APW DH	SOT360-1
20-Pin Plastic Shrink Small Outline (SO)	-40°C to +85°C	74LVCH244A D	74LVCH244A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	-40°C to +85°C	74LVCH244A DB	74LVCH244A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	-40°C to +85°C	74LVCH244A PW	LVCH244APW DH	SOT360-1

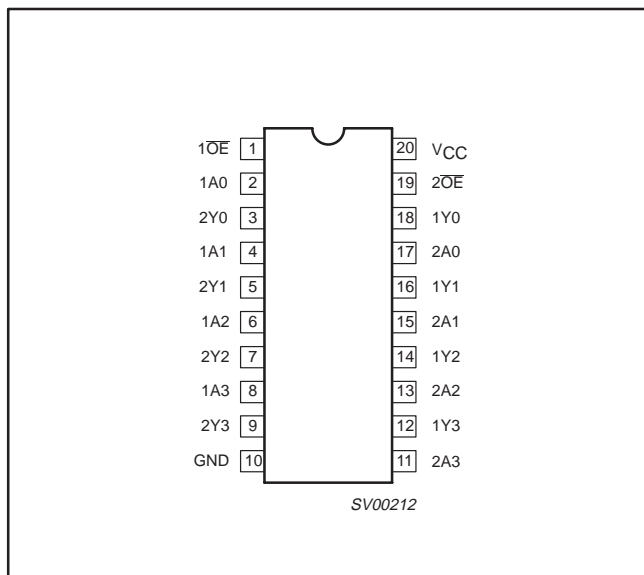
# Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A  
74LVCH244A

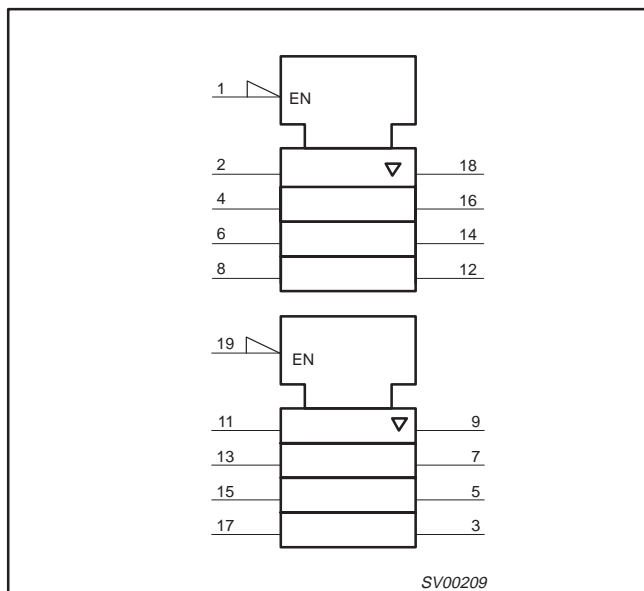
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	1OE	Output enable input (active LOW)
2, 4, 6, 8	1A <sub>0</sub> to 1A <sub>3</sub>	Data inputs
3, 5, 7, 9	2Y <sub>0</sub> to 2Y <sub>3</sub>	Bus outputs
10	GND	Ground (0V)
17, 15, 13, 11	2A <sub>0</sub> to 2A <sub>3</sub>	Bus inputs
18, 16, 14, 12	1Y <sub>0</sub> to 1Y <sub>3</sub>	Bus outputs
19	2OE	Output enable input (active-LOW)
20	V <sub>CC</sub>	Positive supply voltage

## PIN CONFIGURATION



## LOGIC SYMBOL (IEEE/IEC)

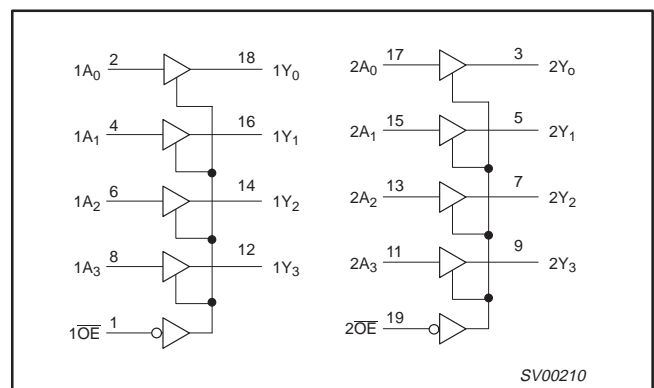


## FUNCTION TABLE

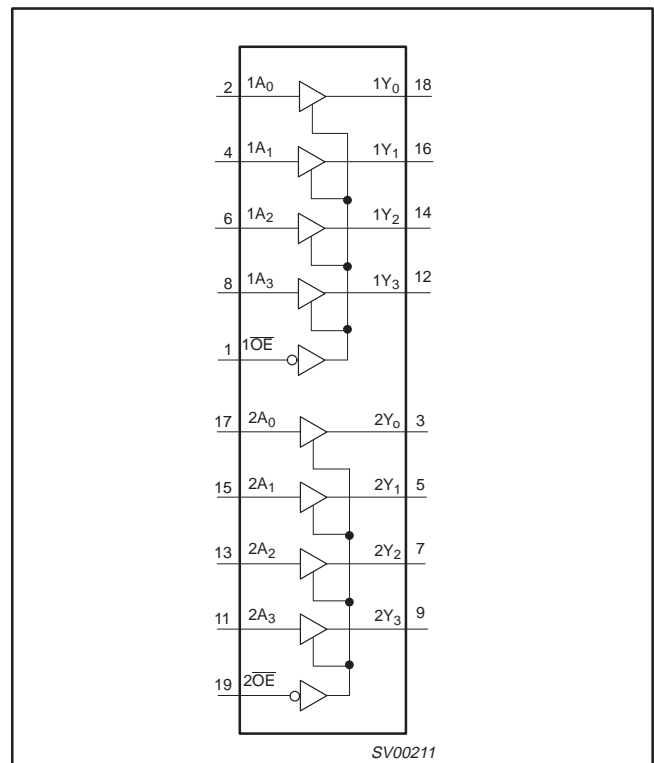
INPUTS		OUTPUT
nOE	nA <sub>n</sub>	nY <sub>n</sub>
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level  
L = LOW voltage level  
X = Don't care  
Z = High impedance OFF-state

## LOGIC SYMBOL



## FUNCTIONAL DIAGRAM



# Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

## 74LVC244A 74LVCH244A

### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
$V_I$	DC Input voltage range		0	5.5	V
$V_O$	DC Output voltage range; output HIGH or LOW state		0	$V_{CC}$	V
	DC output voltage range; output 3-State		0	5.5	
$T_{amb}$	Operating ambient temperature range in free-air		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$	0	20	ns/V
		$V_{CC} = 2.7$ to $3.6V$	0	10	

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +6.5	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	Note 2	-0.5 to +6.5	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_O$	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to $V_{CC} + 0.5$	V
	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		±100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package			mW
	- plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	

#### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

## 74LVC244A 74LVCH244A

### DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA	V <sub>CC</sub> - 0.6			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 0.8			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND		± 0.1	± 5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5V or GND		0.1	± 5	μA
I <sub>off</sub>	Power off leakage supply	V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		0.1	± 10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	10	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	μA
I <sub>BHL</sub>	Bushold LOW sustaining current <sup>2, 3, 4</sup>	V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V	75	-	-	μA
I <sub>BHH</sub>	Bushold HIGH sustaining current <sup>2, 3, 4</sup>	V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V	-75	-	-	μA
I <sub>BHLO</sub>	Bushold LOW overdrive current <sup>2, 3, 5</sup>	V <sub>CC</sub> = 3.6V	500	-	-	μA
I <sub>BHHO</sub>	Bushold HIGH overdrive current <sup>2, 3, 5</sup>	V <sub>CC</sub> = 3.6V	-500	-	-	μA

#### NOTES:

1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
2. Valid for data inputs of bushold parts (LVCH-A) only.
3. For data inputs only, control inputs do not have a bushold circuit
4. The specified sustaining current at the data inputs do not have a bushold circuit.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bushold parts, the bushold circuit is switched off when V<sub>I</sub> exceeds V<sub>CC</sub> allowing 5.5V on the input terminal.

# Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A  
74LVCH244A

## AC CHARACTERISTICS

GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		$V_{CC} = 1.2V$	
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	TYP	
$t_{PHL}$ $t_{PLH}$	Propagation delay $1A_n$ to $1Y_n$ ; $2A_n$ to $2Y_n$	1, 3	1.5	3.5	5.9	1.5	6.9	16.0	ns
$t_{PZH}$ $t_{PZL}$	3-State output enable time $\overline{1OE}$ to $1Y_n$ ; $\overline{2OE}$ to $2Y_n$	2, 3	1.5	4.3	7.6	1.5	8.6	19.0	ns
$t_{PHZ}$ $t_{PLZ}$	3-State output disable time $\overline{1OE}$ to $1Y_n$ ; $\overline{2OE}$ to $2Y_n$	2, 3	1.5	3.7	5.8	1.5	6.8	17.0	ns

**NOTE:**

1. Unless otherwise stated, all typical values are at  $V_{CC} = 3.3V$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .

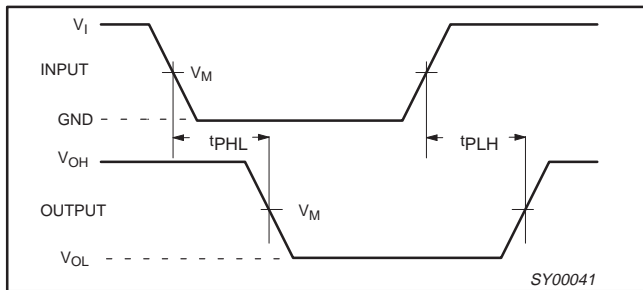
## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$ ;  $V_M = 0.5 V_{CC}$  at  $V_{CC} < 2.7V$

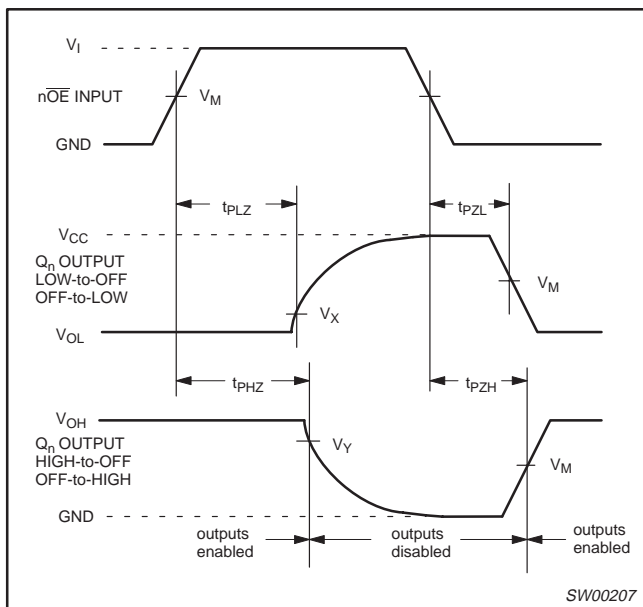
$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_X = V_{OL} + 0.1 V_{CC}$  at  $V_{CC} < 2.7V$

$V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_Y = V_{OH} - 0.1 V_{CC}$  at  $V_{CC} < 2.7V$

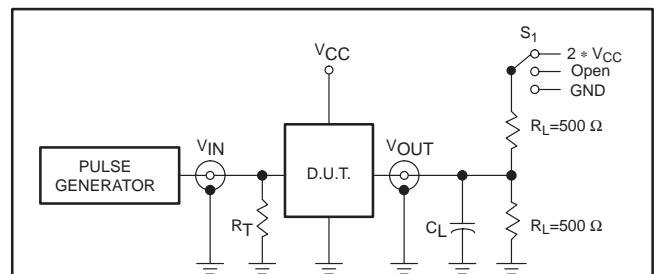


Waveform 1. Input ( $D_n$ ) to output ( $Q_n$ ) propagation delays.



Waveform 2. 3-State enable and disable times.

## TEST CIRCUIT



Test Circuit for 3-State Outputs

**SWITCH POSITION**

TEST	SWITCH
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 * V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$V_{IN}$
$< 2.7V$	$V_{CC}$
$2.7 - 3.6V$	$2.7V$

**DEFINITIONS**

$R_L$  = Load resistor

$C_L$  = Load capacitance includes jig and probe capacitance

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

SW00047

Waveform 3. Load circuitry for switching times.

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A  
74LVCH244A

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

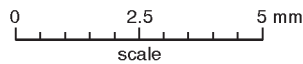
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A  
74LVCH244A

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04



Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A  
74LVCH244A

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16- 95-02-04

# Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A  
74LVCH244A

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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