

# DATA SHEET

**74LV573**

**Octal D-type transparent latch (3-State)**

Product specification  
Supersedes data of 1997 Jun 06  
IC24 Data Handbook

1998 Jun 10

## Octal D-type transparent latch (3-State)

74LV573

## FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between  $V_{CC} = 2.7V$  and  $V_{CC} = 3.6V$
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8V$  at  $V_{CC} = 3.3V$ ,  $T_{amb} = 25^{\circ}C$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2V$  at  $V_{CC} = 3.3V$ ,  $T_{amb} = 25^{\circ}C$
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/microcomputer
- Common 3-State output enable input
- Output capability: bus driver
- $I_{CC}$  category: MSI

## DESCRIPTION

The 74LV573 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT573.

The 74LV573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ( $\overline{OE}$ ) input are common to all internal latches.

The '573' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When  $\overline{OE}$  is LOW, the contents of the eight latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches.

The '573' is functionally identical to the '563' and the '373', but the '563' has inverted outputs and the '373' has a different pin arrangement.

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}C$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay Dn to Qn LE to Qn	$C_L = 15pF$ $V_{CC} = 3.3V$	12 13	ns
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per latch	Notes 1, 2	26	pF

## NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_I = GND$  to  $V_{CC}$ .

## ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	$-40^{\circ}C$ to $+125^{\circ}C$	74LV573 N	74LV573 N	SOT146-1
20-Pin Plastic SO	$-40^{\circ}C$ to $+125^{\circ}C$	74LV573 D	74LV573 D	SOT163-1
20-Pin Plastic SSOP Type II	$-40^{\circ}C$ to $+125^{\circ}C$	74LV573 DB	74LV573 DB	SOT339-1
20-Pin Plastic TSSOP Type I	$-40^{\circ}C$ to $+125^{\circ}C$	74LV573 PW	74LV573PW DH	SOT360-1

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enabled input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0–D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0–Q7	Data outputs
10	GND	Ground (0V)
11	LE	Latch enable input (active HIGH)
20	VCC	Positive supply voltage

# Octal D-type transparent latch (3-State)

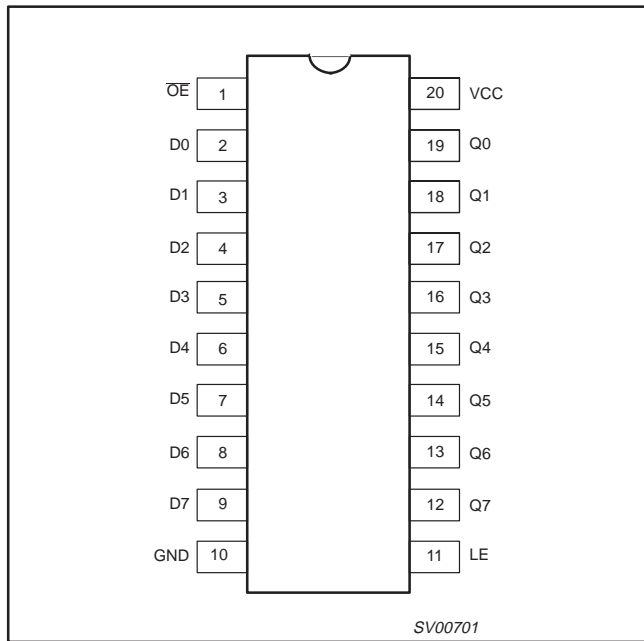
74LV573

## FUNCTION TABLE

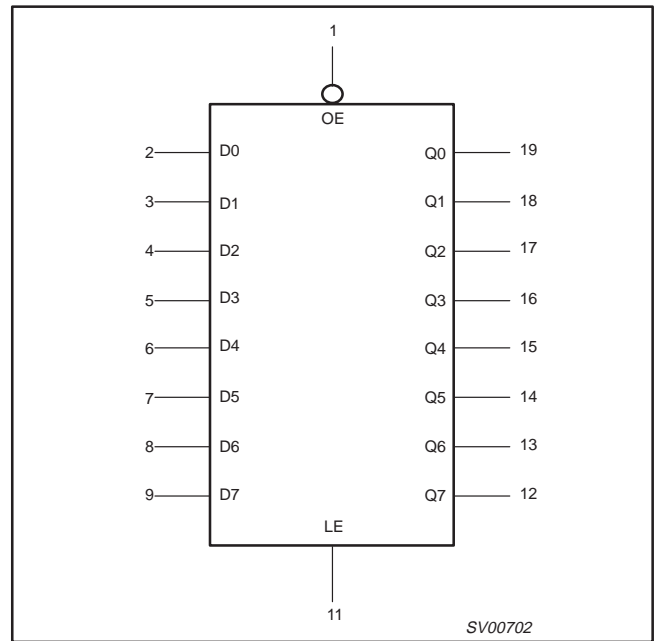
OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q0 to Q7
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 Z = High impedance OFF-state

## PIN CONFIGURATION



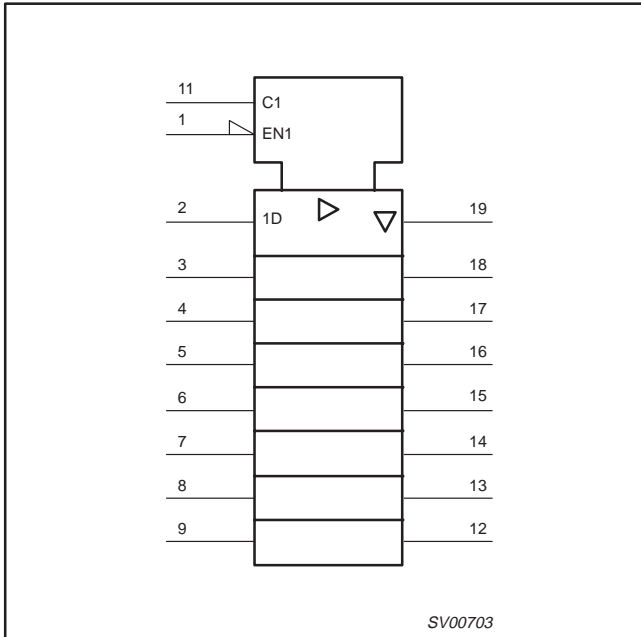
## LOGIC SYMBOL



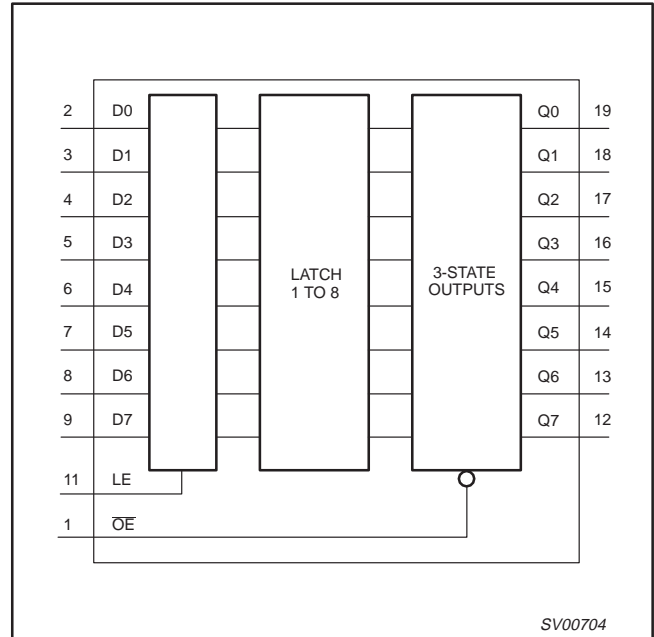
# Octal D-type transparent latch (3-State)

## 74LV573

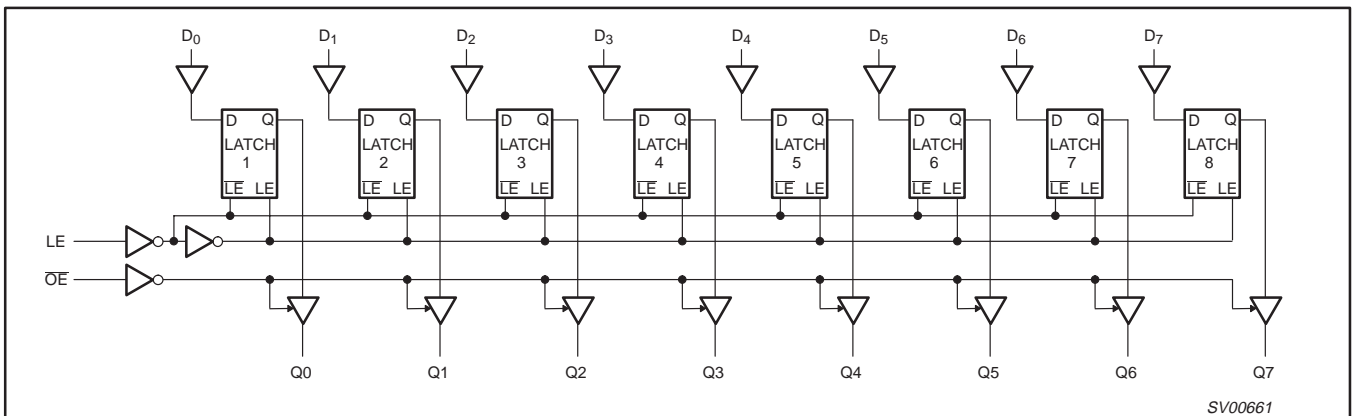
### LOGIC SYMBOL (IEEE/IEC)



### FUNCTIONAL DIAGRAM



### LOGIC DIAGRAM



## Octal D-type transparent latch (3-State)

74LV573

**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC $V_{CC}$ or GND current for types with – bus driver outputs		70	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{tot}$	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note 1	1.0	3.3	5.5	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	-40 -40		+85 +125	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$ $V_{CC} = 3.6V$ to $5.5V$	– – – –	– – – –	500 200 100 50	ns/V

**NOTE:**

- The LV is guaranteed to function down to  $V_{CC} = 1.0V$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2V$  to  $V_{CC} = 5.5V$ .

## Octal D-type transparent latch (3-State)

74LV573

**DC CHARACTERISTICS FOR THE LV FAMILY**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	0.9			0.9		V
		V <sub>CC</sub> = 2.0V	1.4			1.4		
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			2.0		
		V <sub>CC</sub> = 4.5 to 5.5V	0.7*V <sub>CC</sub>			0.7*V <sub>CC</sub>		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			0.3	0.3	V	
		V <sub>CC</sub> = 2.0V			0.6	0.6		
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	0.8		
		V <sub>CC</sub> = 4.5 to 5.5			0.3*V <sub>CC</sub>	0.3*V <sub>CC</sub>		
V <sub>OH</sub>	HIGH level output voltage; all outputs	V <sub>CC</sub> = 1.2V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA		1.2			V	
		V <sub>CC</sub> = 2.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	1.8	2.0		1.8		
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	2.5	2.7		2.5		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	2.8	3.0		2.8		
		V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	4.3	4.5		4.3		
	HIGH level output voltage; BUS driver outputs	V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 8mA	2.40	2.82		2.20		
V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 16mA		3.60	4.20		3.50			
V <sub>OL</sub>	LOW level output voltage; all outputs	V <sub>CC</sub> = 1.2V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0			V	
		V <sub>CC</sub> = 2.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2	0.2		
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2	0.2		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2	0.2		
		V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2	0.2		
	LOW level output voltage; BUS driver outputs	V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8mA		0.20	0.40			0.50
V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 16mA			0.35	0.55		0.65		
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND			1.0		1.0	µA
I <sub>oz</sub>	3-State output OFF-state current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND			5		10	µA
I <sub>CC</sub>	Quiescent supply current; MSI	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0			20.0		160	µA
ΔI <sub>CC</sub>	Additional quiescent supply current per input	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V			500		850	µA

**NOTE:**1. All typical values are measured at T<sub>amb</sub> = 25°C.

## Octal D-type transparent latch (3-State)

74LV573

**AC CHARACTERISTICS**GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 1\text{K}\Omega$ 

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS -40 to +85 °C			LIMITS -40 to +125 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay Dn to Qn	Figures 1, 5	V <sub>CC</sub> (V)						ns
			1.2	-	75	-	-	-	
			2.0	-	26	39	-	49	
			2.7	-	19	29	-	36	
			3.0 to 3.6	-	14 <sup>2</sup>	23	-	29	
4.5 to 5.5	-	-	19	-	24				
$t_{PHL}/t_{PLH}$	Propagation delay LE to Qn	Figures 2, 5	1.2	-	80	-	-	-	ns
			2.0	-	27	43	-	53	
			2.7	-	20	31	-	34	
			3.0 to 3.6	-	15 <sup>2</sup>	25	-	31	
			4.5 to 5.5	-	-	21	-	26	
$t_{PZH}/t_{PZL}$	3-State output enable time OE to Qn	Figures 3, 5	1.2	-	70	-	-	-	ns
			2.0	-	24	37	-	48	
			2.7	-	18	28	-	35	
			3.0 to 3.6	-	13 <sup>2</sup>	22	-	28	
			4.5 to 5.5	-	-	18	-	23	
$t_{PHZ}/t_{PLZ}$	3-State output disable time OE to Qn	Figures 3, 5	1.2	-	80	-	-	-	ns
			2.0	-	29	39	-	48	
			2.7	-	22	29	-	36	
			3.0 to 3.6	-	17 <sup>2</sup>	24	-	29	
			4.5 to 5.5	-	-	20	-	24	
$t_W$	LE pulse width HIGH	Figure 2	2.0	34	9	-	41	-	ns
			2.7	25	6	-	30	-	
			3.0 to 3.6	20	5 <sup>2</sup>	-	24	-	
$t_{su}$	Setup time Dn to LE	Figure 4	1.2	-	25	-	-	-	ns
			2.0	17	9	-	20	-	
			2.7	13	6	-	15	-	
			3.0 to 3.6	10	5 <sup>2</sup>	-	12	-	
$t_h$	Hold time Dn to LE	Figure 4	1.2	-	5	-	-	-	ns
			2.0	8	2	-	8	-	
			2.7	8	2	-	8	-	
			3.0 to 3.6	8	1 <sup>2</sup>	-	8	-	

**NOTES:**All typical values are measured at  $T_{amb} = 25^\circ\text{C}$ 1. Typical values are measured at  $V_{CC} = 3.3\text{V}$

# Octal D-type transparent latch (3-State)

74LV573

## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$  and  $\leq 3.6V$   
 $V_M = 0.5 * V_{CC}$  at  $V_{CC} < 2.7V$  and  $\geq 4.5V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$  and  $\leq 3.6V$   
 $V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7V$  and  $\geq 4.5V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$  and  $\leq 3.6V$   
 $V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7V$  and  $\geq 4.5V$

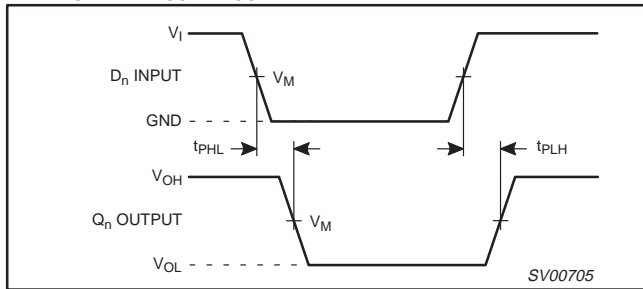


Figure 1. Data input (D<sub>n</sub>) to output (Q<sub>n</sub>) propagation delays and the output transition times

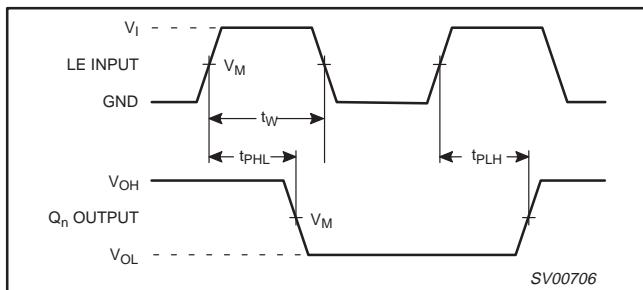


Figure 2. Latch enable input (LE) pulse width, the latch enable input to output (Q<sub>n</sub>) propagation delays and the output transition times.

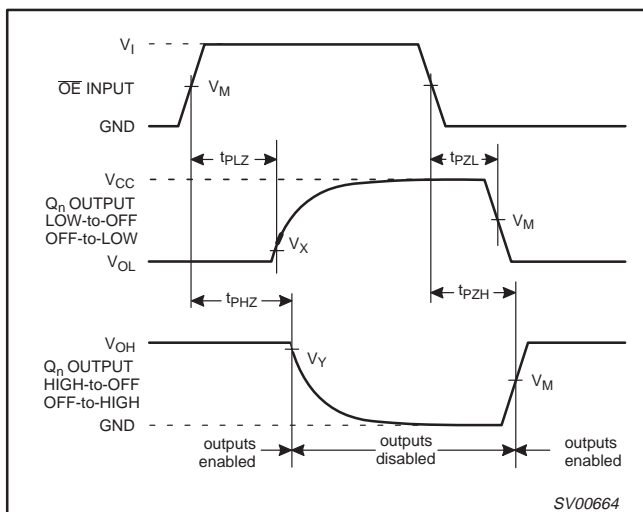


Figure 3. 3-State enable and disable times

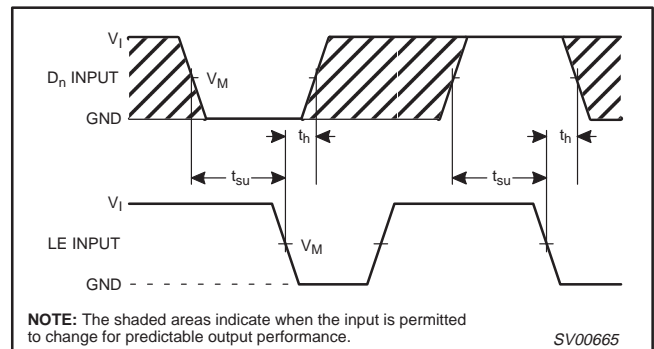
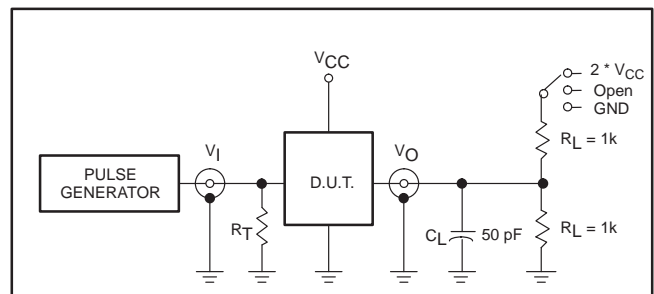


Figure 4. Data set-up and hold times for the D<sub>n</sub> input to the LE input

**NOTE:**  
The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUIT



Test Circuit for Outputs

### DEFINITIONS

$R_L$  = Load resistor  
 $C_L$  = Load capacitance includes jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

### SWITCH POSITION

TEST	S <sub>1</sub>	V <sub>CC</sub>	V <sub>I</sub>
t <sub>PLH</sub> /t <sub>PHL</sub>	Open	< 2.7V	V <sub>CC</sub>
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 * V <sub>CC</sub>	2.7–3.6V	2.7V
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND	≥ 4.5V	V <sub>CC</sub>

SV00896

Figure 5. Load circuitry for switching times

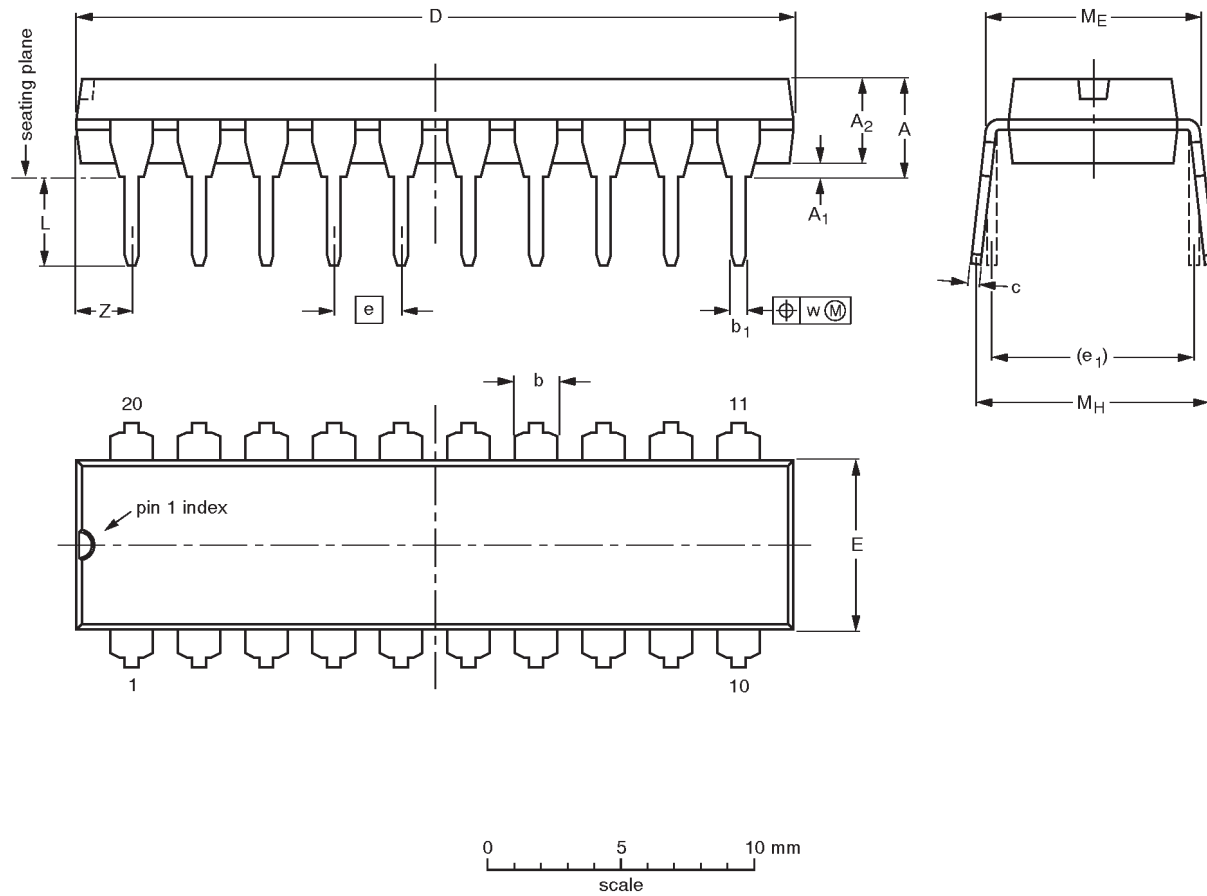


# Octal D-type transparent latch (3-State)

74LV573

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

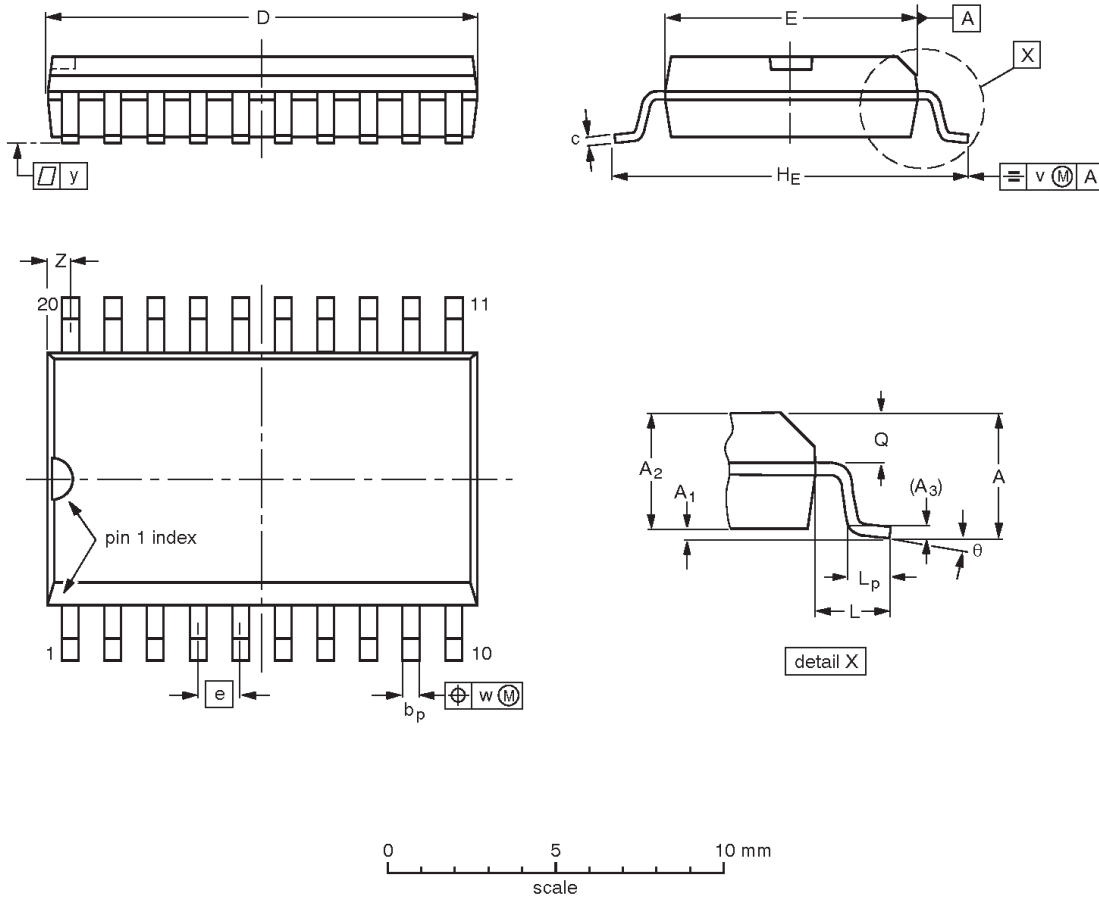
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Octal D-type transparent latch (3-State)

## 74LV573

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	$\theta$
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

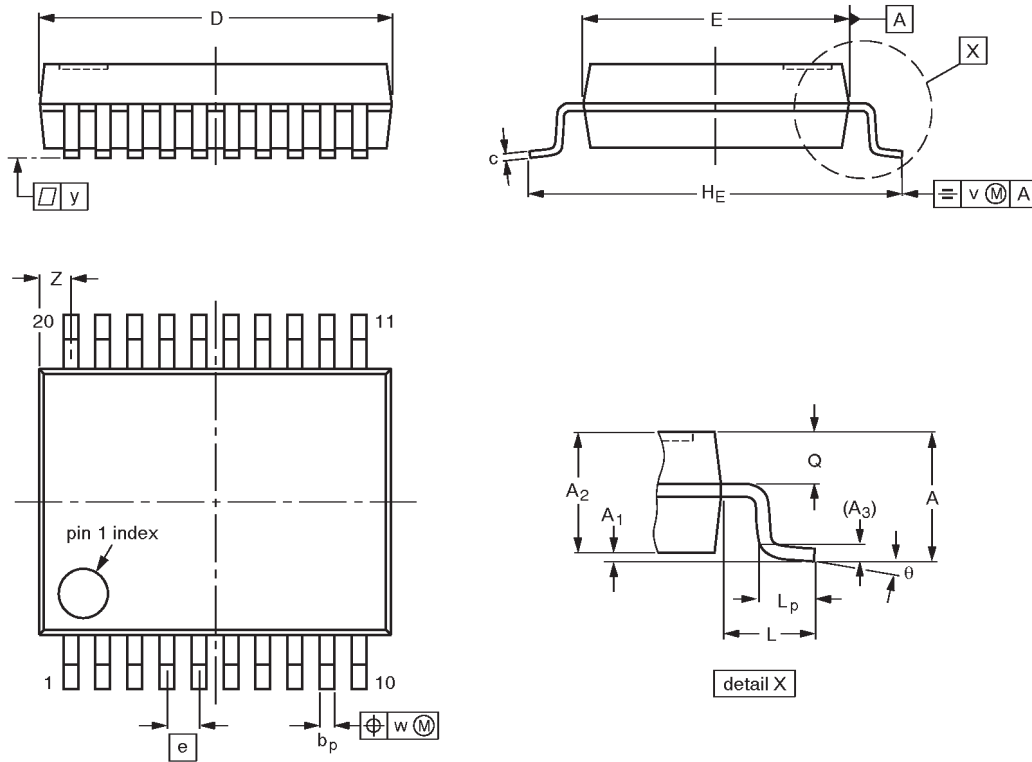
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	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

# Octal D-type transparent latch (3-State)

## 74LV573

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm**

**SOT339-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

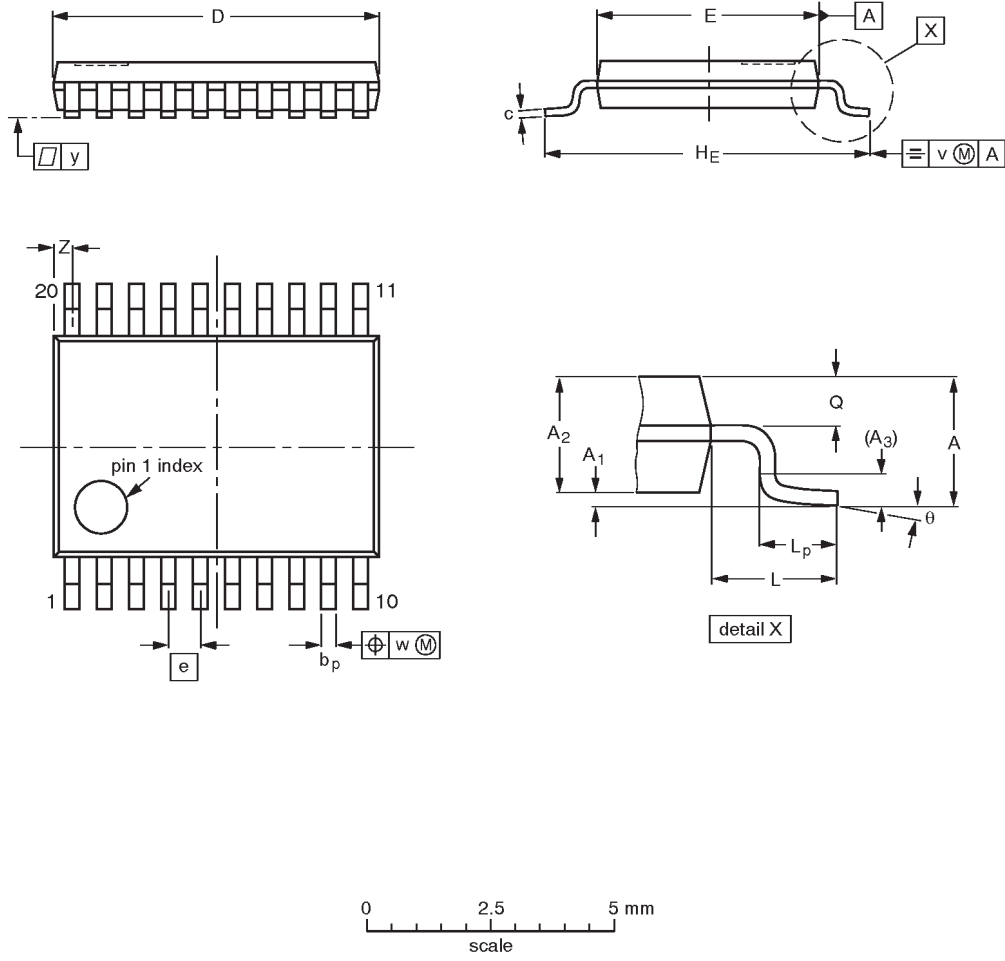
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

# Octal D-type transparent latch (3-State)

## 74LV573

**TSSOP20:** plastic thin shrink small outline package; 20 leads; body width 4.4 mm

**SOT360-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16 95-02-04

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Octal D-type transparent latch (3-State)

74LV573

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**NOTES**

## Octal D-type transparent latch (3-State)

74LV573

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	<b>Full Production</b>	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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