INTEGRATED CIRCUITS



Product specification Supersedes data of 1996 Jan 01 IC24 Data Handbook

1998 Jun 23



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74LV4066

FEATURES

- Optimized for Low Voltage applications: 1.0V to 6.0V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.
- Very low typ "ON" resistance: 25Ω at V_{CC} - VEE = 4.5 V 35Ω at V_{CC} - VEE = 3.0 V 60Ω at V_{CC} - VEE = 2.0 V
- Output capability: non-standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV4066 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT4066.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}C$; $t_r = t_f \le 2.5$ ns

The 74LV4066 has four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the corresponding analog switch is turned off.

The 74LV4066 has an on resistance which is dramatically reduced in comparison with 74HCT4066.

INPUTS	SWITCH			
nE				
L	off			
Н	on			

NOTES:

H = HIGH voltage level

LOW voltage level L =

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PZH} /t _{PZL}	Turn "ON" time: nE to V_{OS}	C _L = 15pF R _L = 1KΩ	10	ns
t _{PHZ} /t _{PLZ}	Turn "OFF" time: nE to V _{OS}	$V_{CC} = 3.3V$	13	ns
Cl	Input capacitance		3.5	pF
C _{PD}	Power dissipation capacitance per switch	Notes 1, 2	11	pF
C _S	Maximum switch capacitances		8	pF

NOTES:

 C_{PD} is used to determine the dynamic power dissipation (P_D in μW) 1.

 $\begin{array}{l} \mathsf{P}_{D} = \mathsf{C}_{PD} \times \mathsf{V}_{CC}^2 \times \mathsf{f}_i + \sum \left(\mathsf{C}_L \times \mathsf{V}_{CC}^2 \times \mathsf{f}_o\right) \text{ where:} \\ \mathsf{f}_i = \mathsf{input} \ \mathsf{frequency} \ \mathsf{in} \ \mathsf{MHz}; \ \mathsf{C}_L = \mathsf{output} \ \mathsf{load} \ \mathsf{capacity} \ \mathsf{in} \ \mathsf{pF}; \\ \mathsf{f}_o = \mathsf{output} \ \mathsf{frequency} \ \mathsf{in} \ \mathsf{MHz}; \ \mathsf{C}_s = \mathsf{maximum} \ \mathsf{switch} \ \mathsf{capacitance} \ \mathsf{in} \ \mathsf{pF}; \\ \sum \left\{ (\mathsf{C}_L + \mathsf{C}_S) \times \mathsf{V}_{CC}^2 \times \mathsf{F}_o \right\} = \mathsf{sum} \ \mathsf{of} \ \mathsf{the} \ \mathsf{outputs}. \end{array}$

 \overline{V}_{CC} = supply voltage in V.

2. The condition is $V_I = GND$ to V_{CC} .

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES							
	PINS	PACKAGE	MATERIAL	CODE				
74LV4066N	16	DIL	Plastic	SOT27-1				
74LV4066D	16	SO	Plastic	SOT108-1				
74LV4066DB	16	SSOP	Plastic	SOT337-1				
74LV4066PW	16	TSSOP	Plastic	SOT402-1				

PIN CONFIGURATION

1Y 1		4 V _{CC}
1Z 2	1:	3 1E
2Z 3	1:	2 4E
2Y 4	1	1 4Y
2E 5	10	0 4Z
3E 6		9 3Z
GND 7	1	B 3Y
	sva	01669

PIN DESCRIPTION

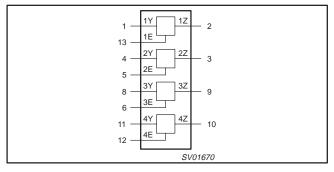
PIN NUMBER	SYMBOL	FUNCTION
1, 4, 8, 11	1Y – 4Y	Independent inputs/outputs
2, 3, 9, 10	1Z – 4Z	Independent inputs/outputs
13, 5, 6, 12	1E to 4E	Enable input (active HIGH)
7	GND	Ground (0V)
14	V _{CC}	Positive supply voltage

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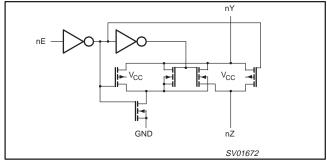
FUNCTION TABLE

74LV4066

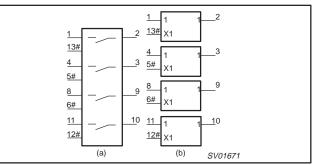
FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM (ONE SWITCH)



IEC LOGIC SYMBOL



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	PARAMETER CONDITIONS		TYP	MAX	UNIT
V _{CC}	DC supply voltage	See Note 1	1.0	3.3	6	V
VI	Input voltage		0	-	V _{CC}	V
V _O	Output voltage		0	-	V _{CC}	V
T _{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	-40 -40		+85 +125	°C
t _r , t _f	Input rise and fall times	$\begin{array}{c} V_{CC} = 1.0V \text{ to } 2.0V \\ V_{CC} = 2.0V \text{ to } 2.7V \\ V_{CC} = 2.7V \text{ to } 3.6V \\ V_{CC} = 3.6V \text{ to } 5.5V \end{array}$	- - - -	- - - -	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_{\rm I} < -0.5 \text{ or } V_{\rm I} > V_{\rm CC} + 0.5 V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_{O} < -0.5 \text{ or } V_{O} > V_{CC} + 0.5 V$	50	mA
$\pm I_{O}$	DC switch current	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
T _{stg}	Storage temperature range		-65 to +150	°C
Power dissipation per package – plastic DIL – plastic mini-pack (SO)		for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:

 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

			LIMITS					
SYMBOL	PARAMETER	TEST CONDITIONS	-4	0°C to +8	5°C	-40°C to	o +125°C	
			MIN	TYP ¹	MAX	MIN	MAX	1
		V _{CC} = 1.2 V	0.90			0.90		
		V _{CC} = 2.0 V	1.40			1.4		1
VIH	HIGH level Input voltage	V _{CC} = 2.7 to 3.6 V	2.00			2.0		V
	voltage	$V_{CC} = 4.5 V$	3.15			3.15		1
		V _{CC} = 6.0 V	4.20			4.20		1
		V _{CC} = 1.2 V			0.30		0.30	
		V _{CC} = 2.0 V			0.60		0.60	1
V _{IL}	LOW level Input	V _{CC} = 2.7 to 3.6 V			0.80		0.80	V
	voltage	V _{CC} = 4.5 V			1.35		1.35	1
		$V_{CC} = 6.0 V$			1.80		1.80	1
±II	Input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND}$ $V_{CC} = 6.0 \text{ V}; V_I = V_{CC} \text{ or GND}$			1.0 2.0		1.0 2.0	μΑ
±IS	Analog switch OFF-state current per channel	$V_{CC} = 3.6 \text{ V}; \text{ V}_{I} = \text{V}_{IH} \text{ or } \text{V}_{IL}$ $V_{CC} = 6.0 \text{ V}; \text{ V}_{I} = \text{V}_{IH} \text{ or } \text{V}_{IL}$			1.0 2.0		1.0 2.0	μA
±IS	Analog switch ON-state current per channel	$ \begin{array}{l} V_{CC} = 3.6 \; V; \; V_{I} = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 6.0 \; V; \; V_{I} = V_{IH} \; \text{or} \; V_{IL} \end{array} $			1.0 2.0		1.0 2.0	μA
I _{CC}	Quiescent supply current	$V_{CC} = 3.6V; V_I = V_{CC} \text{ or GND}; I_O = 0$ $V_{CC} = 6.0V; V_I = V_{CC} \text{ or GND}; I_O = 0$			20 40		40 80	μΑ
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_{I} = V_{CC} – 0.6 V			500		850	μA
R _{ON}	ON-resistance (peak)	$ \begin{array}{l} V_{CC} = 1.2 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 2.0 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 2.7 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 3.0 \; to \; 3.6 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 4.5 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 6.0 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ \end{array} $		300 60 41 37 25 23	- 130 60 72 52 47		- 150 90 83 60 54	Ω
R _{ON}	ON-resistance (rail)	$ \begin{array}{l} V_{CC} = 1.2 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 2.0 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 2.7 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 3.0 \; to \; 3.6 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 4.5 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 6.0 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ \end{array} $		75 35 26 24 15 13	- 98 60 52 40 35		- 115 68 60 45 40	Ω
R _{ON}	ON-resistance (rail)	$ \begin{array}{l} V_{CC} = 1.2 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 2.0 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 2.7 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 3.0 \; to \; 3.6 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 4.5 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 6.0 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ \end{array} $		75 40 35 30 22 20	- 110 72 65 47 40		- 130 85 75 55 47	Ω
ΔR_{ON}	Maximum variation of ON-resistance between any two channels	$ \begin{array}{l} V_{CC} = 1.2 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 2.0 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 2.7 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 3.0 \; to \; 3.6 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 4.5 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ V_{CC} = 6.0 \; V; \; V_{I} = V_{IH} \; or \; V_{IL} \\ \end{array} $		- 5 4 3 2				Ω

NOTE:

All typical values are measured at T_{amb} = 25°C.
At supply voltage approaching 1.2V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

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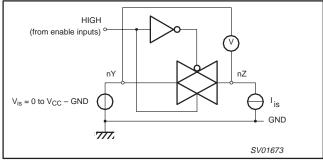


Figure 1. Test circuit for measuring ON-resistance (Ron).

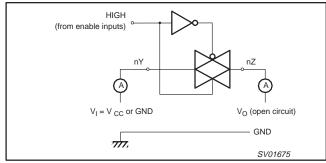


Figure 3. Test circuit for measuring ON-state current.

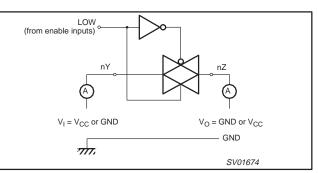


Figure 2. Test circuit for measuring OFF-state current.

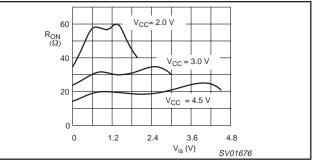


Figure 4. Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to $V_{CC} - V_{EE}$.

		LIMITS				CONDITION			
SYMBOL	PARAMETER	–40 to +85 °C		–40 to +125 °C				UNIT	
		MIN	TYP ¹	MAX	MIN	MAX		V _{CC} (V)	OTHER
			8					1.2	
	Drana action delay		5	26		31		2.0	R _L = ∞;
t _{PHL} /t _{PLH}	Propagation delay V _{is} to V _{os}		3 ²	15		18	ns	2.7 to 3.6	$C_{1} = 50 \text{pF}$
	15 10 105		2	13		15		4.5	Figure 12
			2	10		12		6.0	
			40					1.2	$R_L = 1 k\Omega;$ $C_L = 50 pF$ Figures 13 and 14
	Turn-on time		22	43		51		2.0 2.7 to 3.6	
t _{PZH} /t _{PZL}	nE to V _{os}		12 ²	25		30	ns		
	03		10	21		26		4.5	
			8	16		20		6.0	
			50					1.2	
	Turn-off time		27	65		81		2.0	$R_L = 1 k\Omega;$ $C_L = 50 pF$
t _{PHZ} /t _{PLZ}	nE to V _{os}		15 ²	38		47	ns	2.7 to 3.6	$C_L = 50 \text{ pF}$
	03		13	32		40		4.5	Figures 13 and 14
			12	28		34		6.0]

NOTES:

1. All typical values are measured at $T_{amb} = 25^{\circ}C$. 2. All typical values are measured at $V_{CC} = 3.3V$.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \le 2.5$ ns; $C_L = 50$ pF

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ADDITIONAL AC CHARACTERISTICS

 $GND = 0 \text{ V}; t_r = t_f \leq 2.5 ns; C_L = 50 pF$

SYMBOL	PARAMETER	ТҮР	UNIT	V _{CC} (V)	V _{IS(P-P)} (V)	CONDITIONS
	Sine-wave distortion $f = 1 \text{ kHz}$	0.04	%	3.0	2.75	R _L = 10 kΩ; C _L = 50 pF
	Sine-wave distortion I = 1 kHz		70	6.0	5.50	Figure 15
	Sine-wave distortion f = 10 kHz	0.12	%	3.0	2.75	R_L = 10 kΩ; C_L = 50 pF
		0.06	70	6.0	5.50	Figure 15
	Switch "OFF" signal feed through	-50	dB	3.0	Note 1	$R_L = 600 \text{ k}\Omega; C_L = 50 \text{ pF}; \text{ f=1 MHz}$
	Switch Off Signalieed through	-50	uВ	6.0		Figures 10 and 16
	Crosstalk between any two switches	-60	dB	3.0	Note 1	$R_L = 600 \text{ k}\Omega; C_L = 50 \text{ pF}; \text{ f=1 MHz}$
	orossialik between any two switches	-60	üD	6.0		Figure 12
V _(p-p)	Crosstalk voltage between enable or address	110	mV	3.0		$R_L = 600 \text{ k}\Omega; C_L = 50 \text{ pF}; \text{ f=1 MHz}$ (nE, square wave between V _{CC} and
• (p–p)	v (p-p) input to any switch (peak-to-peak value)		iiiv	6.0		GND, $T_r = t_f = 6$ ns) Figure 13
f	Minimum frequency response (-3 dB)	180	mHz	3.0	Note 2	$R_L = 50 \text{ k}\Omega; C_L = 50 \text{ pF}$
f _{max}		200	111112	6.0		Figures 11 and 14
CS	Maximum switch capacitance	8	pF			

GENERAL NOTES:

 V_{is} is the input voltage at nY or nZ terminal, whichever is assigned as an input. V_{os} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

NOTES:

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).

2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

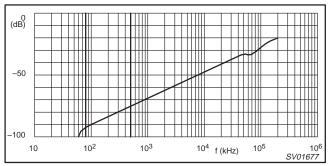


Figure 5. Typical switch "OFF" signal feed-through as a function of frequency.

NOTES TO FIGURES 5 AND 6:

Test conditions: V_{CC} = 3.0 V; GND = 0 V; R_L = 50 Ω ; R_{SOURCE} = 1k Ω .

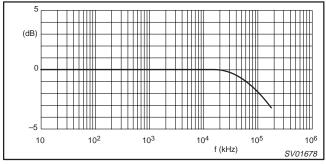


Figure 6. Typical frequency response.

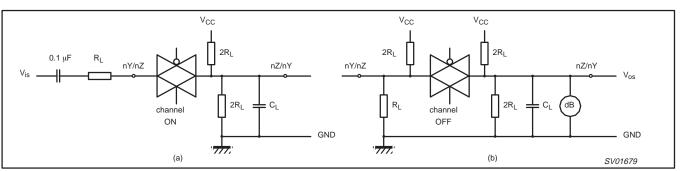


Figure 7. Test circuit for measuring crosstalk between any two switches. (a) channel ON condition; (b) channel OFF condition.

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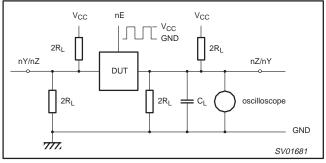
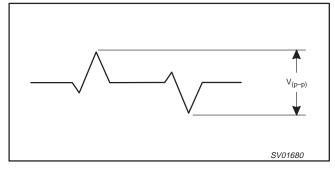
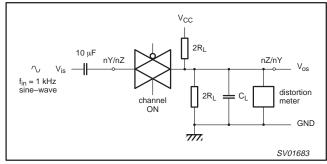


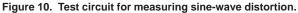
Figure 8. Test circuit for measuring crosstalk between control and any switch.

NOTE TO FIGURE 8:

The crosstalk is defined as follows (oscilloscope output):







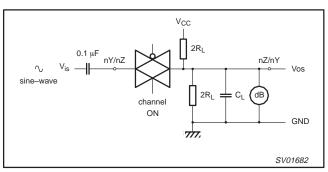
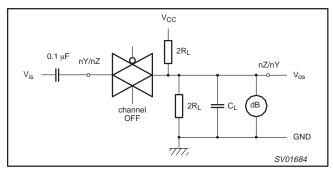
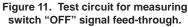


Figure 9. Test circuit for measuring minimum frequency response.

NOTE TO FIGURE 9:

Adjust input voltage to obtain 0 dBm at V_{OS} when F_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of –3 dB at V_{OS}.





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WAVEFORMS

 $\begin{array}{l} V_M = 1.5 \ V \ at \ V_{CC} \geq 2.7 \ V \\ V_M = 0.5 \times V_{CC} \ at \ V_{CC} \leq 2.7 \ V \\ V_{OL} \ and \ V_{OH} \ are the typical output voltage drop that occur with the output load \\ V_X = V_{OL} + 0.3 \ V \ at \ V_{CC} \geq 2.7 \ V \\ V_X = V_{OL} + 0.1 \times V_{CC} \ at \ V_{CC} < 2.7 \ V \\ V_Y = V_{OH} - 0.3 \ V \ at \ V_{CC} \geq 2.7 \ V \\ V_Y = V_{OH} - 0.1 \times V_{CC} \ V_{CC} < 2.7 \ V \\ V_Y = V_{OH} - 0.1 \times V_{CC} \ V_{CC} < 2.7 \ V \\ \end{array}$

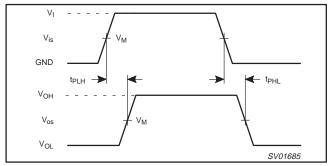


Figure 12. Input (V_{is}) to output (V_{os}) propagation delays.

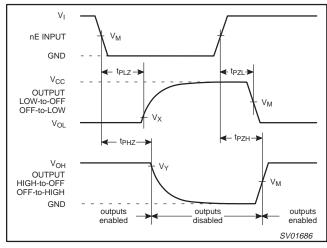
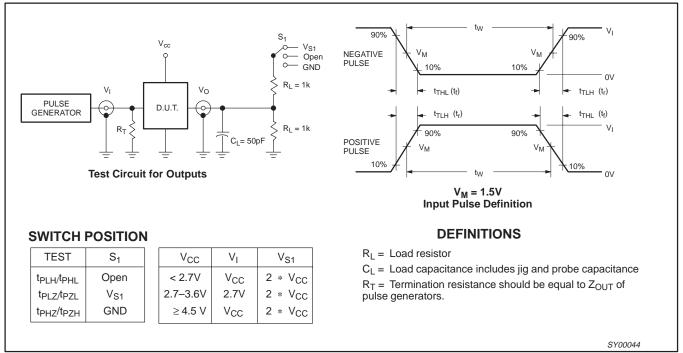


Figure 13. Turn-on and turn-off times for the inputs (nS, \overline{E}) to the output (V_{os}).

TEST CIRCUIT





74LV4066

DEFINITIONS					
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