

DATA SHEET

74LV165

8-bit parallel-in/serial-out shift register

Product specification
Supersedes data of 1997 May 15
IC24 Data Handbook

1998 May 07

8-bit parallel-in/serial-out shift register

74LV165

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_{amb} = 25^{\circ}\text{C}$
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_{amb} = 25^{\circ}\text{C}$
- Asynchronous 8-bit parallel load
- Synchronous serial input
- Output capability: standard
- I_{CC} category: MSI

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay \overline{CE} , CP to Q_7 , \overline{Q}_7 PL to Q_7 , \overline{Q}_7 D ₇ to Q_7 , \overline{Q}_7	$C_L = 15$ pF; $V_{CC} = 3.3$ V	18 18 14	ns
f_{max}	Maximum clock frequency		78	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	$V_{CC} = 3.3$ V $V_I = \text{GND to } V_{CC}^1$	35	pF

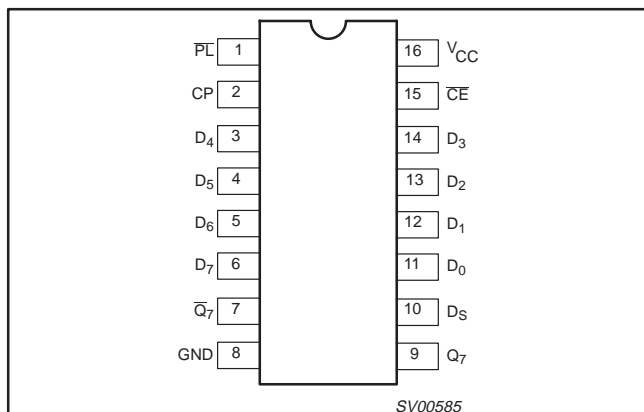
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	$-40^{\circ}\text{C to } +125^{\circ}\text{C}$	74LV165 N	74LV165 N	SOT38-4
16-Pin Plastic SO	$-40^{\circ}\text{C to } +125^{\circ}\text{C}$	74LV165 D	74LV165 D	SOT109-1
16-Pin Plastic SSOP Type II	$-40^{\circ}\text{C to } +125^{\circ}\text{C}$	74LV165 DB	74LV165 DB	SOT338-1
16-Pin Plastic TSSOP Type I	$-40^{\circ}\text{C to } +125^{\circ}\text{C}$	74LV165 PW	74LV165PW DH	SOT403-1

PIN CONFIGURATION



DESCRIPTION

The 74LV165 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT165.

The 74LV165 is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q_7 and \overline{Q}_7) available from the last stage. When the parallel load (PL) input is LOW, parallel data from the D₀ to D₇ inputs are loaded into the register asynchronously. When PL is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable (\overline{CE}) input. The pin assignment for the CP and CE inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input CE should only take place while CP HIGH for predictable operation. Either the CP or the CE should be HIGH before the LOW-to-HIGH transition of PL to prevent shifting the data when PL is activated.

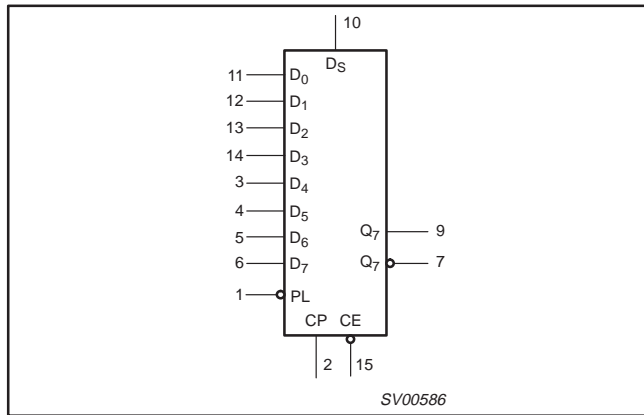
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	\overline{PL}	Asynchronous parallel load input (active LOW)
2	CP	Clock input (LOW to HIGH, edge-triggered)
7	\overline{Q}_7	Complementary output from the last stage
8	GND	Ground (0 V)
9	Q_7	Serial output from last stage
10	D _S	Serial data input
11, 12, 13, 14, 3, 4, 5, 6	D ₀ to D ₇	Parallel data inputs
15	\overline{CE}	Clock enable input (active LOW)
16	V_{CC}	Positive supply voltage

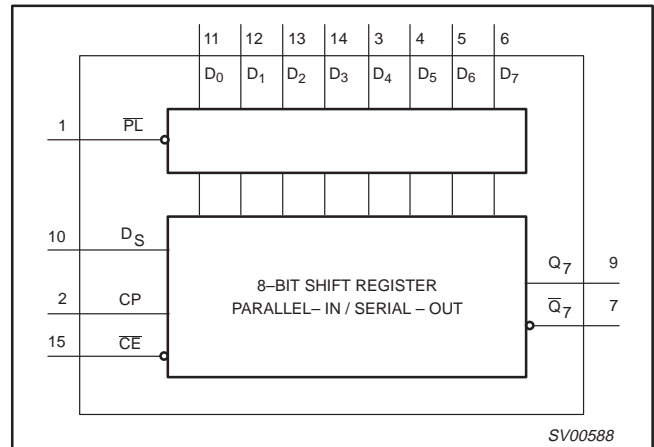
8-bit parallel-in/serial-out shift register

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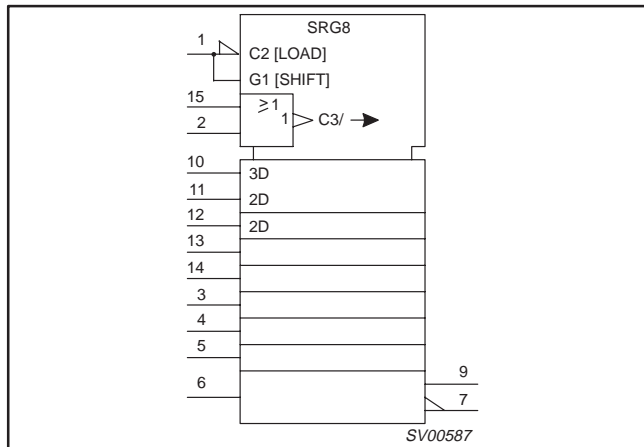
LOGIC SYMBOL



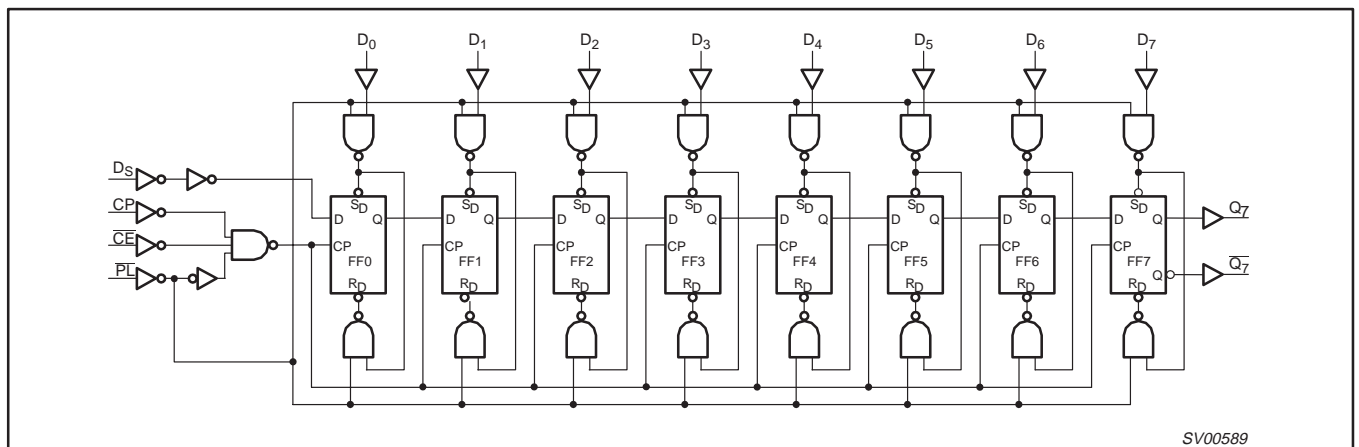
FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



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FUNCTION TABLE

OPERATING MODES	INPUTS					Qn REGISTERS		OUTPUTS	
	PL	CE	CP	D _S	D ₀ -D ₇	Q ₀	Q ₁ -Q ₆	Q ₇	Q̄ ₇
Parallel load	L	X	X	X	L	L	L-L	L	H
	L	X	X	X	H	H	H-H	H	L
Serial Shift	H	L	↑	l	X	L	q ₀ -q ₅	q ₆	q̄ ₆
	H	L	↑	h	X	H	q ₀ -q ₅	q ₆	q̄ ₆
Hold "do nothing"	H	H	X	X	X	q ₀	q ₁ -q ₆	q ₇	q ₇

NOTES:

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition

X = don't care

↑ = LOW-to-HIGH clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V _{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V _I	Input voltage		0	-	V _{CC}	V
V _O	Output voltage		0	-	V _{CC}	V
T _{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	-40 -40		+85 +125	°C
t _r , t _f	Input rise and fall times	V _{CC} = 1.0V to 2.0V V _{CC} = 2.0V to 2.7V V _{CC} = 2.7V to 3.6V V _{CC} = 3.6V to 5.5V	- - - -	- - - -	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
± I _{IK}	DC input diode current	V _I < -0.5 or V _I > V _{CC} + 0.5V	20	mA
± I _{OK}	DC output diode current	V _O < -0.5 or V _O > V _{CC} + 0.5V	50	mA
± I _O	DC output source or sink current - standard outputs	-0.5V < V _O < V _{CC} + 0.5V	25	mA
± I _{GND} , ± I _{CC}	DC V _{CC} or GND current for types with - standard outputs		50	mA
T _{stg}	Storage temperature range		-65 to +150	°C
P _{TOT}	Power dissipation per package - plastic DIL - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2 V	0.9			0.9		V
		V _{CC} = 2.0 V	1.4			1.4		
		V _{CC} = 2.7 to 3.6 V	2.0			2.0		
		V _{CC} = 4.5 to 5.5 V	0.7 * V _{CC}			0.7 * V _{CC}		
V _{IL}	LOW level Input voltage	V _{CC} = 1.2 V			0.3		0.3	V
		V _{CC} = 2.0 V			0.6		0.6	
		V _{CC} = 2.7 to 3.6 V			0.8		0.8	
		V _{CC} = 4.5 to 5.5			0.3 * V _{CC}		0.3 * V _{CC}	
V _{OH}	HIGH level output voltage; all outputs	V _{CC} = 1.2 V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA		1.2				V
		V _{CC} = 2.0 V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	1.8	2.0		1.8		
		V _{CC} = 2.7 V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	2.5	2.7		2.5		
		V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	2.8	3.0		2.8		
		V _{CC} = 4.5 V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	4.3	4.5		4.3		
V _{OH}	HIGH level output voltage; STANDARD outputs	V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; -I _O = 6mA	2.40	2.82		2.20		V
		V _{CC} = 4.5 V; V _I = V _{IH} or V _{IL} ; -I _O = 12mA	3.60	4.20		3.50		
V _{OL}	LOW level output voltage; all outputs	V _{CC} = 1.2 V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0				V
		V _{CC} = 2.0 V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 2.7 V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 4.5 V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
V _{OL}	LOW level output voltage; STANDARD outputs	V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.25	0.40		0.50	V
		V _{CC} = 4.5 V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.35	0.55		0.65	
I _I	Input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND			1.0		1.0	µA
I _{CC}	Quiescent supply current; MSI	V _{CC} = 5.5 V; V _I = V _{CC} or GND; I _O = 0			20.0		160	µA
ΔI _{CC}	Additional quiescent supply current per input	V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V			500		850	µA

NOTE:1. All typical values are measured at T_{amb} = 25°C.

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AC CHARACTERISTICSGND = 0V; $t_r = t_f \leq 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 1\text{K}\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				V _{CC} (V)	MIN	TYP ¹	MAX	MIN	
t _{PLH} /t _{PHL}	Propagation delay CE, CP to Q ₇ , Q ₇	Figures 1, 2	1.2	–	115		–		ns
			2.0	–	38	61	–	76	
			2.7	–	27	43	–	54	
			3.0 to 3.6	–	22 ²	36	–	45	
			4.5 to 5.5	–	15	24	–	30	
t _{PLH} /t _{PHL}	Propagation delay PL to Q ₇ , Q ₇	Figures 1, 2	1.2	–	110		–		ns
			2.0	–	35	56	–	70	
			2.7	–	24	39	–	49	
			3.0 to 3.6	–	20 ²	33	–	41	
			4.5 to 5.5	–	14	22	–	27	
t _{PLH} /t _{PHL}	Propagation delay D ₇ to Q ₇ , Q ₇	Figures 1, 2	1.2	–	90		–		ns
			2.0	–	28	45	–	56	
			2.7	–	20	32	–	40	
			3.0 to 3.6	–	17 ²	27	–	33	
			4.5 to 5.5	–	11	18	–	22	
t _w	Clock Pulse width HIGH or LOW	Figures 1, 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	7 ²	–	24	–	
			4.5 to 5.5	15	5	–	18	–	
t _w	Parallel load pulse width LOW	Figures 1, 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	7 ²	–	24	–	
			4.5 to 5.5	15	5	–	18	–	
t _{rem}	Removal time PL to CP, CE	Figures 1, 2	1.2	–	40	–	–	–	ns
			2.0	24	15	–	30	–	
			2.7	18	11	–	23	–	
			3.0 to 3.6	17	10 ²	–	21	–	
			4.5 to 5.5	12	7	–	15	–	
t _{su}	Set-up time D _S to CP, CE	Figures 1, 2	1.2	–	–8	–	–	–	ns
			2.0	22	–2	–	26	–	
			2.7	16	–1	–	19	–	
			3.0 to 3.6	13	–1 ²	–	15	–	
			4.5 to 5.5	9	0	–	10	–	
t _{su}	Set-up time CE to CP; CP to CE	Figures 1, 2	1.2	–	20	–	–	–	ns
			2.0	22	7	–	26	–	
			2.7	16	5	–	19	–	
			3.0 to 3.6	13	4 ²	–	15	–	
			4.5 to 5.5	9	3	–	10	–	

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AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f \leq 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 1\text{K}\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	-40 to +85 °C			-40 to +125 °C		UNIT
			V _{CC} (V)	MIN	TYP ¹	MAX	MIN	MAX	
t _{su}	Set-up time D _n to $\overline{\text{PL}}$	Figures 1, 2	1.2	-	25	-	-	-	ns
			2.0	22	8	-	26	-	
			2.7	16	6	-	19	-	
			3.0 to 3.6	13	5 ²	-	15	-	
			4.5 to 5.5	9	4	-	10	-	
t _h	Hold time D _s to CP, $\overline{\text{CE}}$ D _n to $\overline{\text{PL}}$	Figures 1, 2	1.2	-	20	-	-	-	ns
			2.0	22	7	-	26	-	
			2.7	16	5	-	19	-	
			3.0 to 3.6	13	4	-	15	-	
			4.5 to 5.5	9	3	-	10	-	
t _h	Hold time $\overline{\text{CE}}$ to CP, CP to $\overline{\text{CE}}$	Figures 1, 2	1.2	-	-30	-	-	-	ns
			2.0	5	-8	-	5	-	
			2.7	5	-6	-	5	-	
			3.0 to 3.6	5	-5 ²	-	5	-	
			4.5 to 5.5	5	-4	-	5	-	
f _{max}	Maximum clock pulse frequency	Figures 1, 2	2.0	14	40	-	12	-	MHz
			2.7	19	60	-	16	-	
			3.0 to 3.6	24	65 ²	-	20	-	
			4.5 to 5.5	36	75	-	30	-	

NOTES:

1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V.

V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V;

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

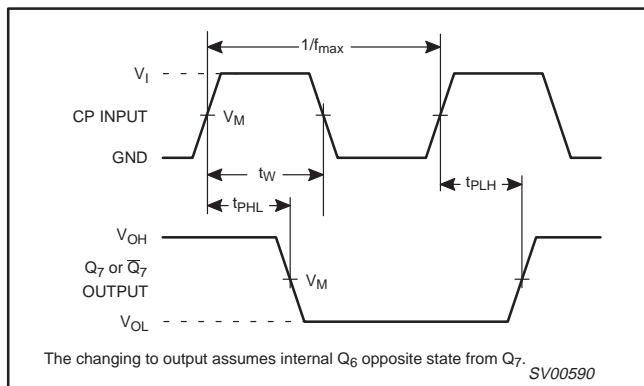


Figure 1. Clock (CP) to output (Q₇ or \overline{Q}_7) propagation delays, the clock pulse width and the maximum clock frequency.

Note to Figures 1 and 2

The changing to output assumes internal Q₆ opposite state from Q₇.

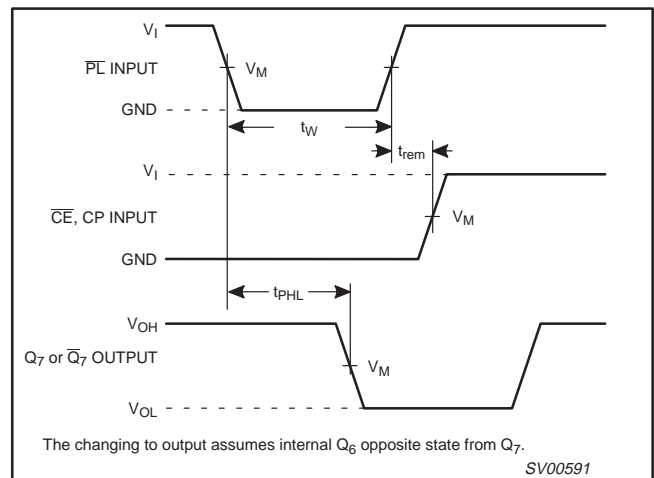


Figure 2. Parallel load ($\overline{\text{PL}}$) pulse width, the parallel load to output (Q₇ or \overline{Q}_7) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{\text{CE}}$) removal time.

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AC WAVEFORMS

$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$.
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$;
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

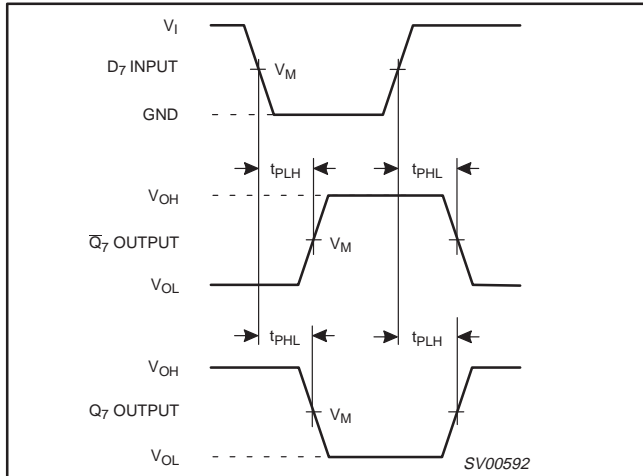


Figure 3. Data input (D_n) to output (Q_7 or \bar{Q}_7) propagation delays when $\bar{P}L$ is LOW.

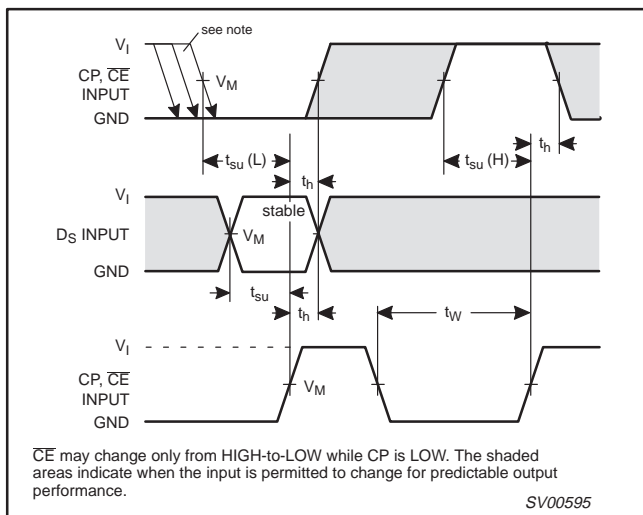


Figure 4. Set-up and hold times from the serial data input (D_S) to the clock (CP) and the clock enable (CE) inputs, from the clock enable input ($\bar{C}E$) to the clock input (CP) and from the clock input (CP) to the clock enable input (CE).

Note to Figure 4

$\bar{C}E$ may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

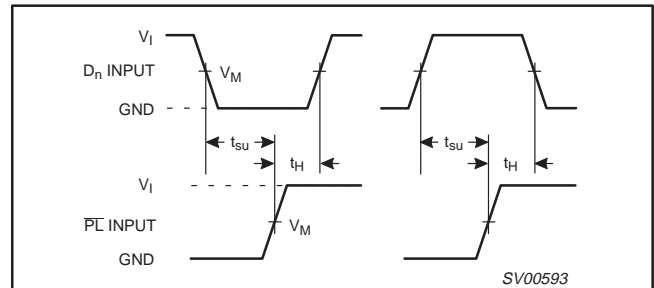


Figure 5. Set-up and hold times from the data inputs (D_n) to the parallel load input ($\bar{P}L$).

TEST CIRCUIT

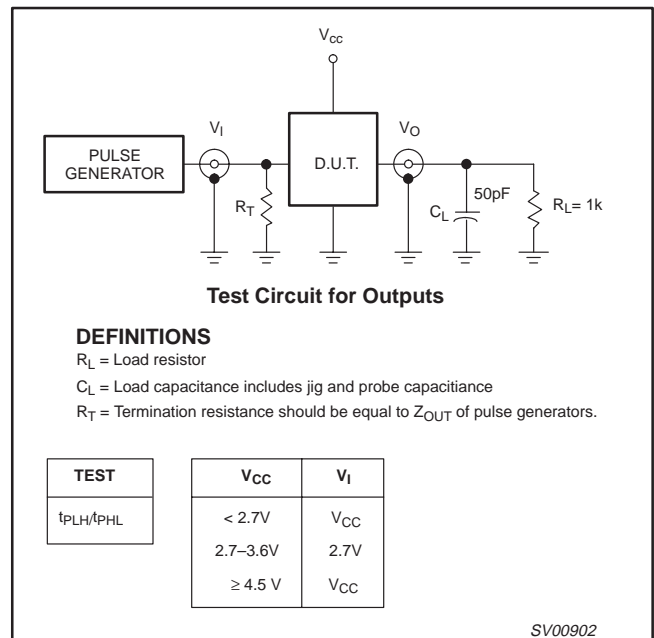


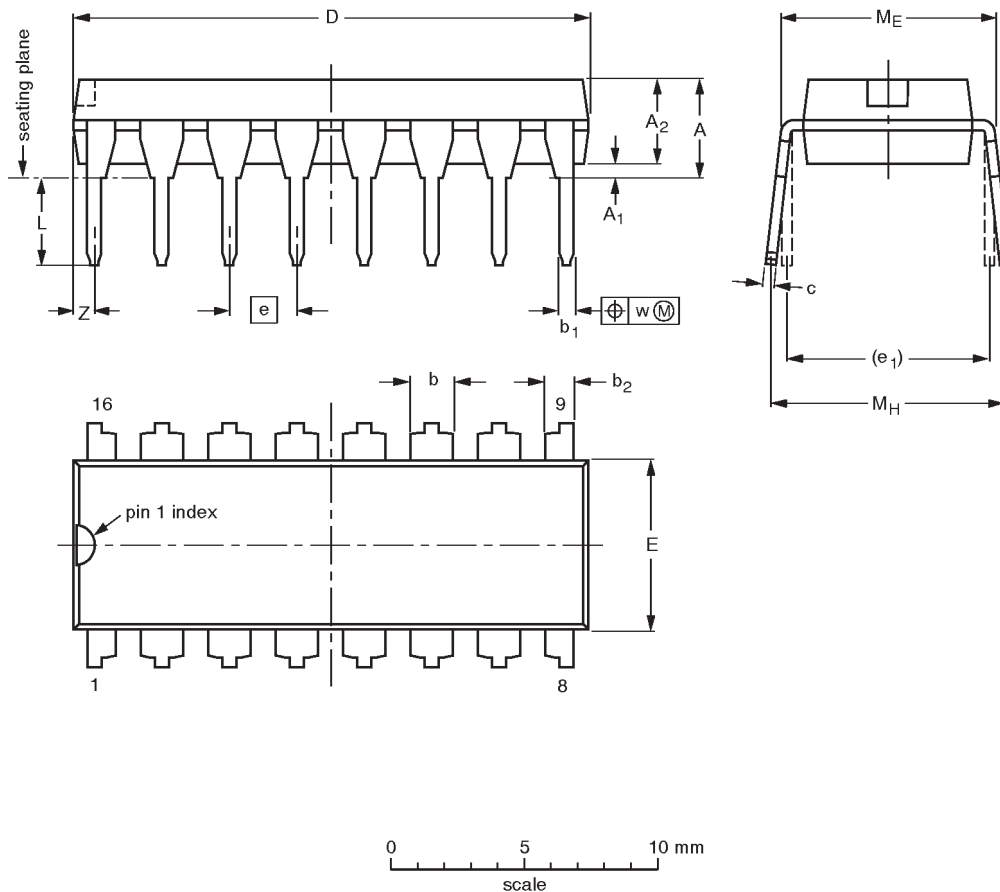
Figure 6. Load circuitry for switching times.

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

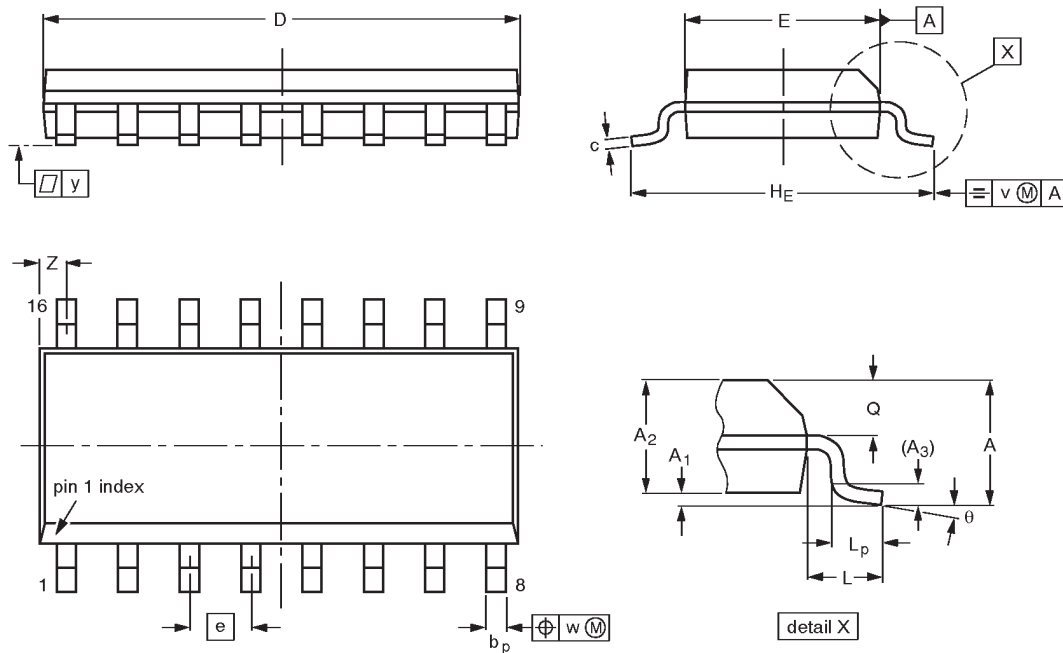
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

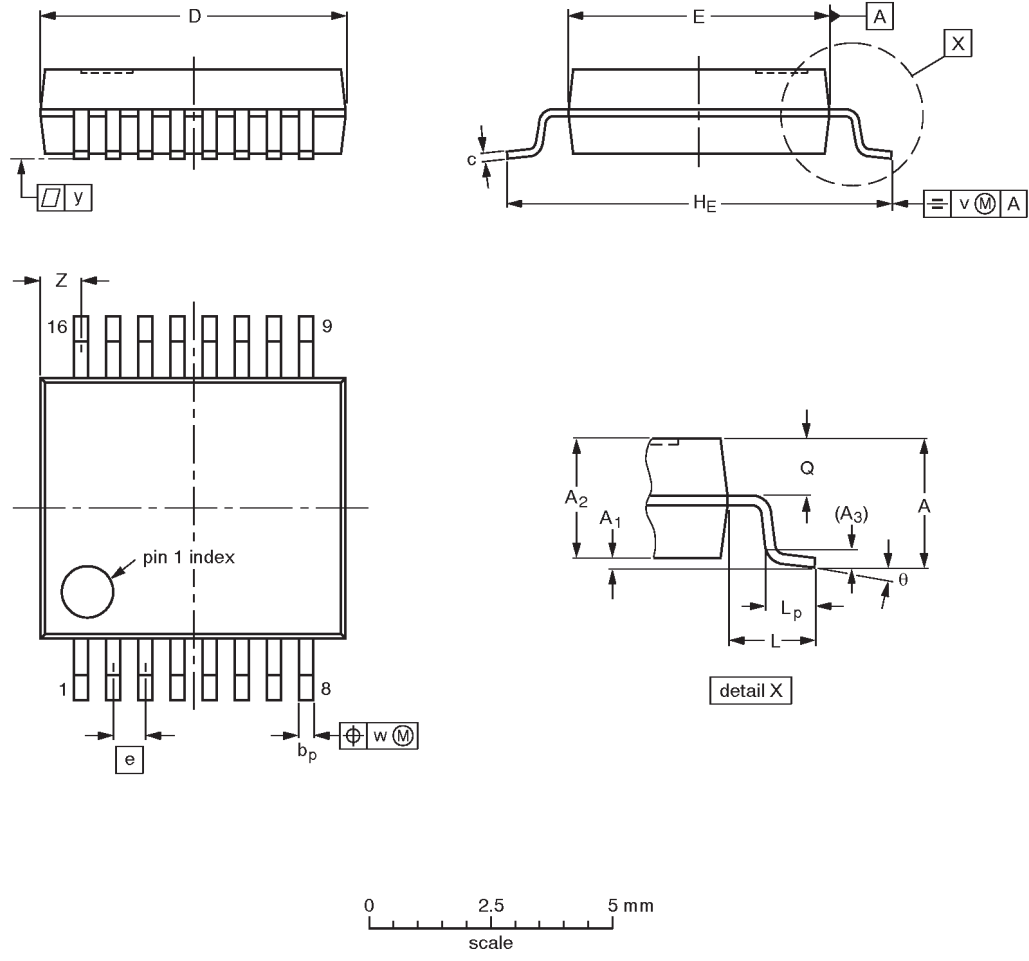
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	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				91-08-13 95-01-23

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

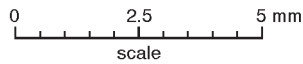
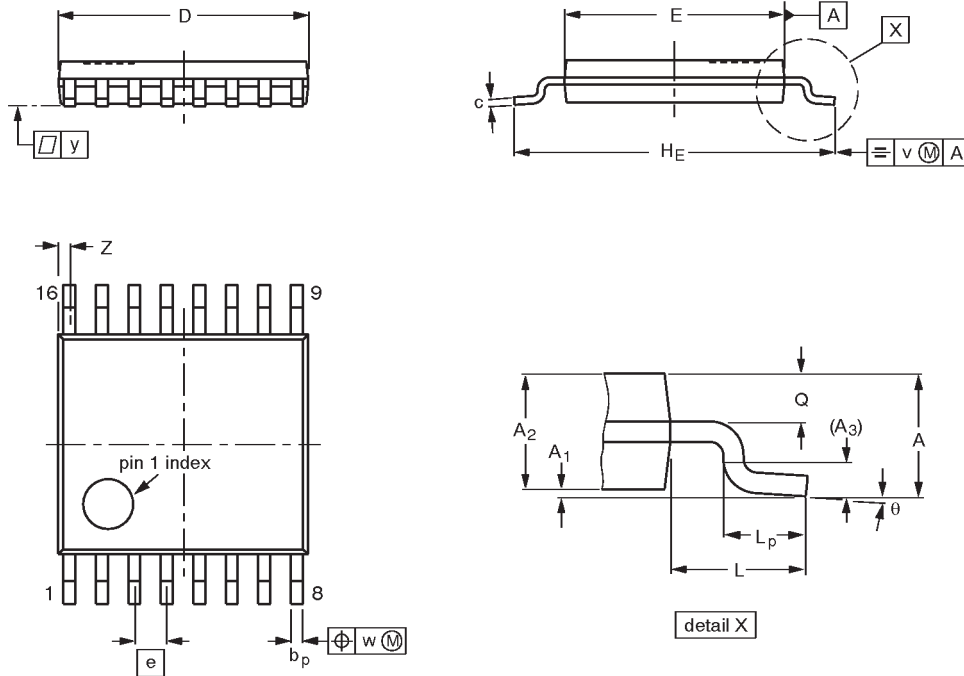
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14- 95-02-04

8-bit parallel-in/serial-out shift register

74LV165

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

8-bit parallel-in/serial-out shift register

74LV165

NOTES

8-bit parallel-in/serial-out shift register

74LV165

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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