DATA SHEET

74LV164
8-bit serial-in/parallel-out shift register

Product specification
Supersedes data of 1997 Mar 28
IC24 Data Handbook

1998 May 07

Philips
Semiconductors

PHILIPS

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8-bit serial-in/parallel-out shift register 74LV164

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Gated serial data inputs
- Asynchronous master reset
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV164 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT164.

The 74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q_0, which is the logical AND of the two data inputs (D_{sa}, D_{sb}) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n $\overline{MR}$ to Q_n	C_L = 15pF V_{CC} = 3.3V	12 12	ns
f_{max}	Maximum clock frequency		78	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_{CC} = 3.3V Notes 1 and 2	40	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV164 N	74LV164 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV164 D	74LV164 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV164 DB	74LV164 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV164 PW	74LV164PW DH	SOT402-1

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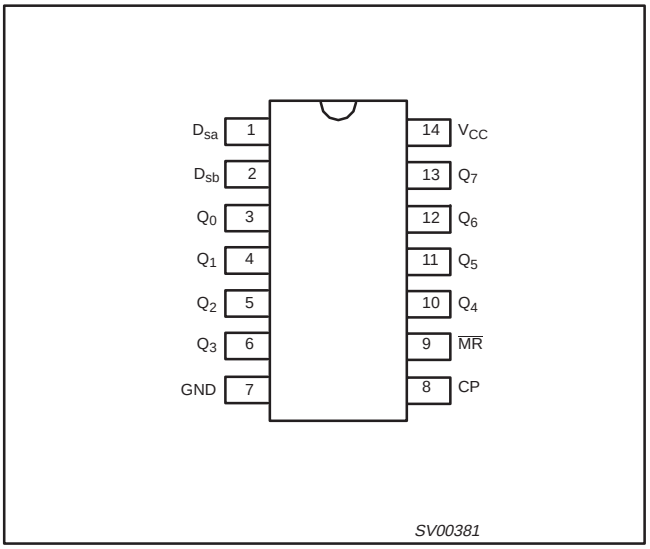
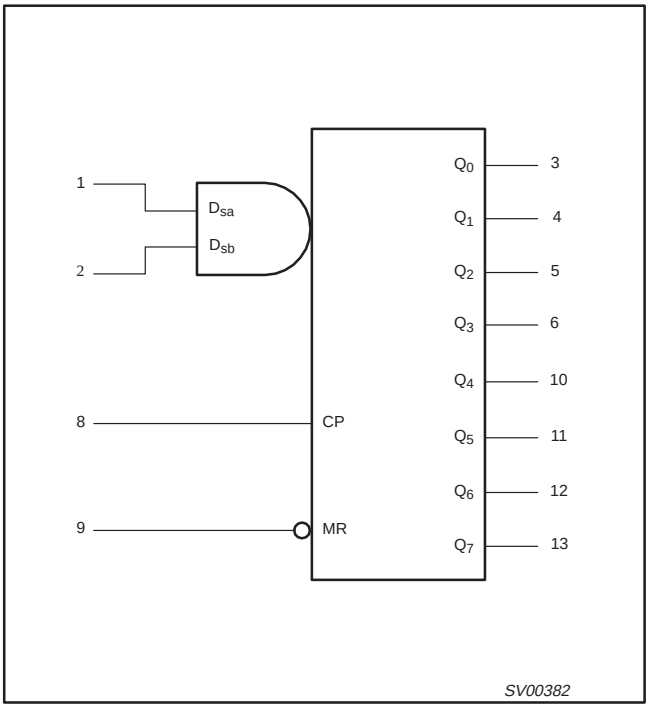
PIN CONFIGURATION



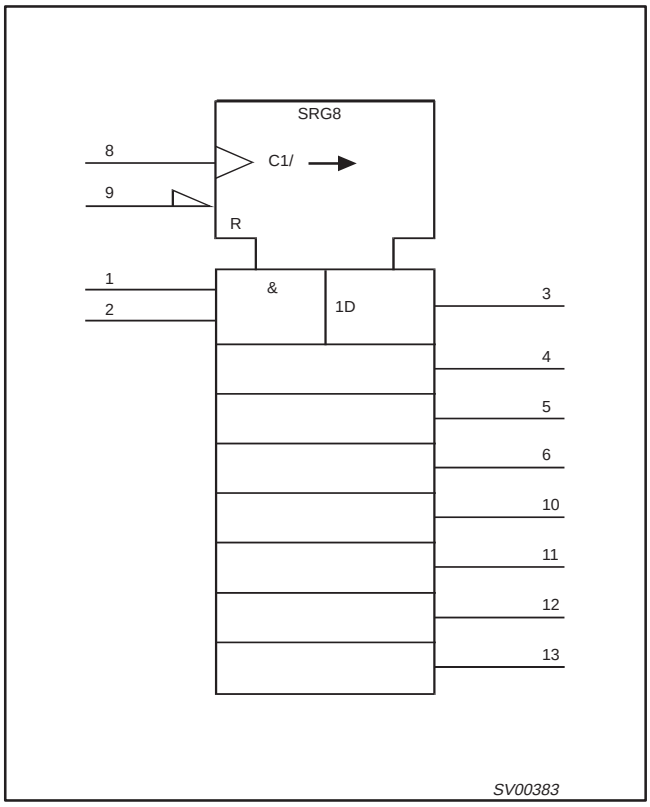
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1,2	D_{sa}, D_{sb}	Data inputs
3, 4, 5, 6, 10, 11, 12, 13	Q_0 to Q_7	Outputs
7	GND	Ground (0V)
8	CP	Clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	Master reset input (active LOW)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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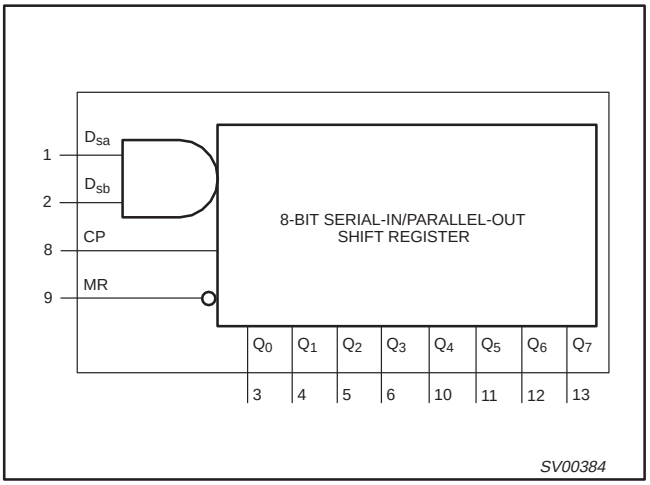
FUNCTIONAL DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	$Q_1 – Q_7$
Reset (clear)	L	X	x	x	L	L – L
Shift	H	↑	l	l	L	$q_0 – q_6$
	H	↑	l	h	L	$q_0 – q_6$
	H	↑	h	l	L	$q_0 – q_6$
	H	↑	h	h	H	$q_0 – q_6$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = Lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < –0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < –0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$–0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTES:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTES:

1. All typical values are measured at T_{amb} = 25°C.

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AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	Figure 1	1.2	–	75	–	–	–	ns
			2.0	–	26	39	–	49	
			2.7	–	19	29	–	36	
			3.0 to 3.6	–	14[2]	23	–	29	
			4.5 to 5.5	–	12[2]	19	–	24	
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Figure 2	1.2	–	75	–	–	–	ns
			2.0	–	26	39	–	49	
			2.7	–	19	29	–	36	
			3.0 to 3.6	–	14[2]	23	–	29	
			4.5 to 5.5	–	12[2]	19	–	24	
t_W	Clock pulse width HIGH to LOW	Figure 1	2.0	34	9	–	41	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5[2]	–	24	–	
			4.5 to 5.5	13	4[2]		16		
t_W	Master reset pulse width; LOW	Figure 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6[2]	–	24	–	
			4.5 to 5.5	13	5[2]		16		
t_{rem}	Removal time $\overline{MR}$ to CP	Figure 2	1.2	–	30	–	–	–	ns
			2.0	19	10	–	24	–	
			2.7	14	8	–	18	–	
			3.0 to 3.6	11	6[2]	–	14	–	
			4.5 to 5.5	8	5[2]		10		
t_{su}	Set-up time D_{sa}, D_{sb} to CP	Figure 3	1.2	–	15	–	–	–	ns
			2.0	22	5	–	26	–	
			2.7	16	4	–	19	–	
			3.0 to 3.6	13	3[2]	–	15	–	
			4.5 to 5.5	9	2[2]		10		
t_h	Hold time D_{sa}, D_{sb} to CP	Figure 3	1.2	–	–10	–	–	–	ns
			2.0	5	–3	–	5	–	
			2.7	5	–2	–	5	–	
			3.0 to 3.6	5	–2[2]	–	5	–	
			4.5 to 5.5	5	–1[2]		5		
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40	–	12	–	MHz
			2.7	19	58	–	16	–	
			3.0 to 3.6	24	70[2]	–	20	–	
			4.5 to 5.5	36	100[2]		30		

NOTE:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25°C$.
2. Typical value measured at $V_{CC} = 3.3$V.
3. Typical value measured at $V_{CC} = 5.0$V.

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AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq 2.7V \leq 3.6V$
V_M = 0.5V * V_{CC} at $V_{CC} < 2.7V$ and $\geq 4.5V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

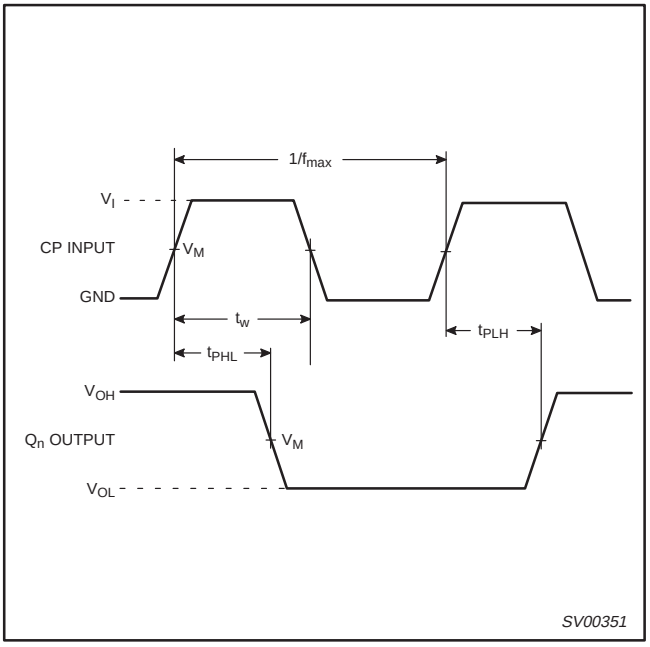


Figure 1. The clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency

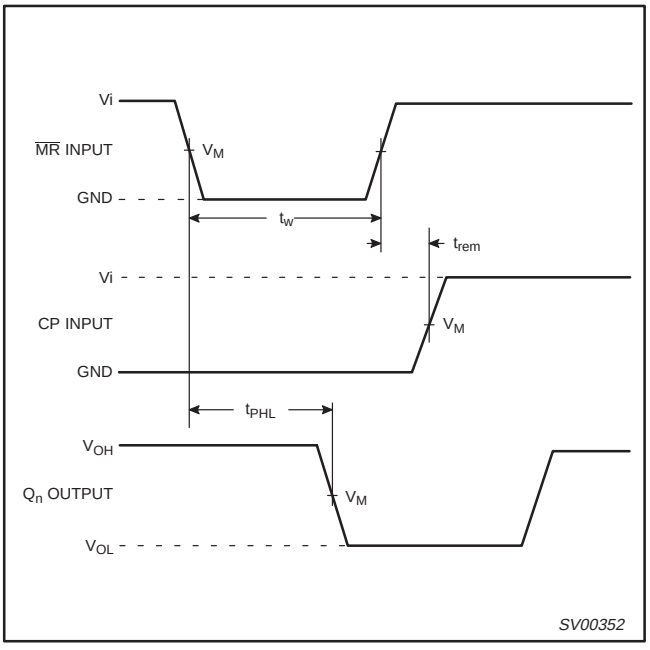


Figure 2. The master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delay and the master reset to clock (CP) removal time

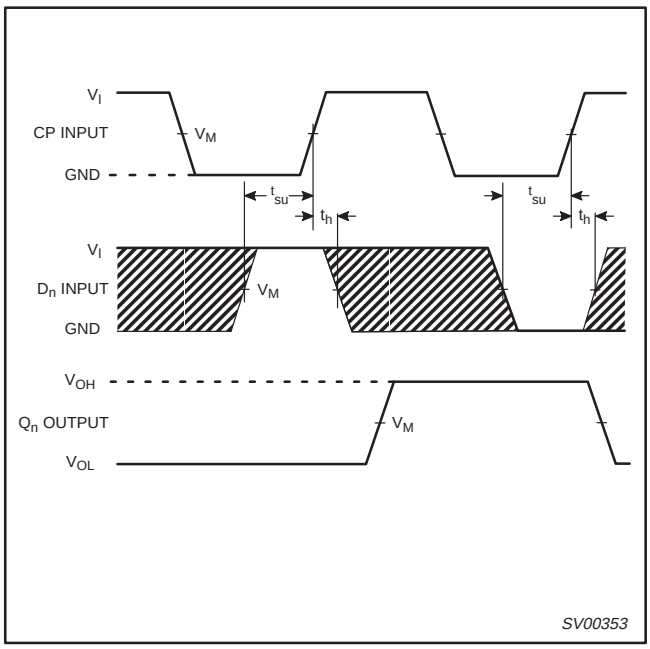
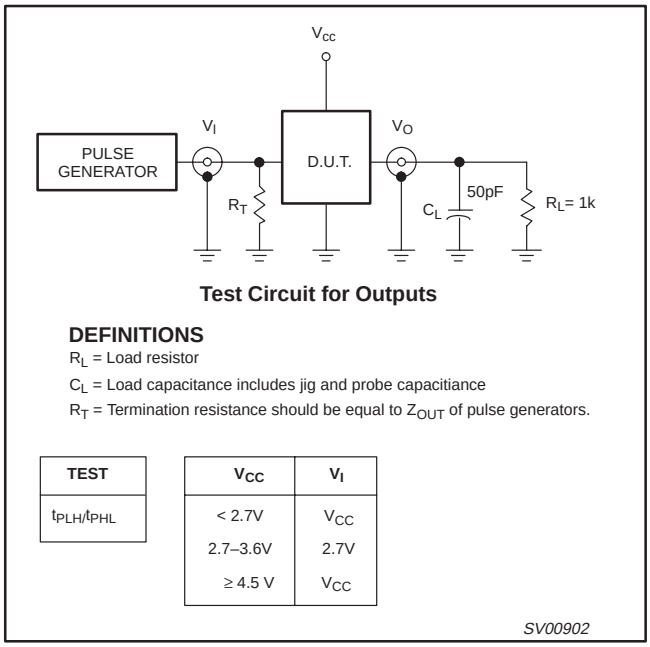


Figure 3. Data set-up and hold times for the D_n inputs

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS
R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5 V	V_{CC}

Figure 4. Load circuitry for switching times

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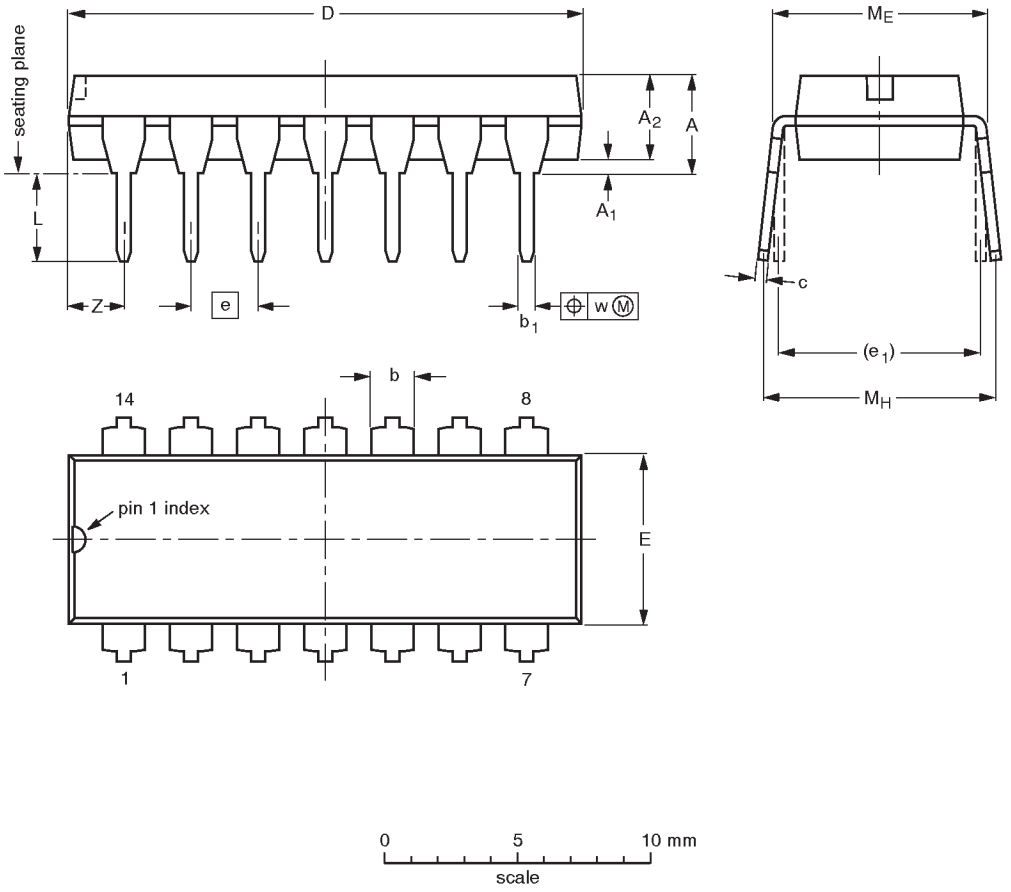
DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

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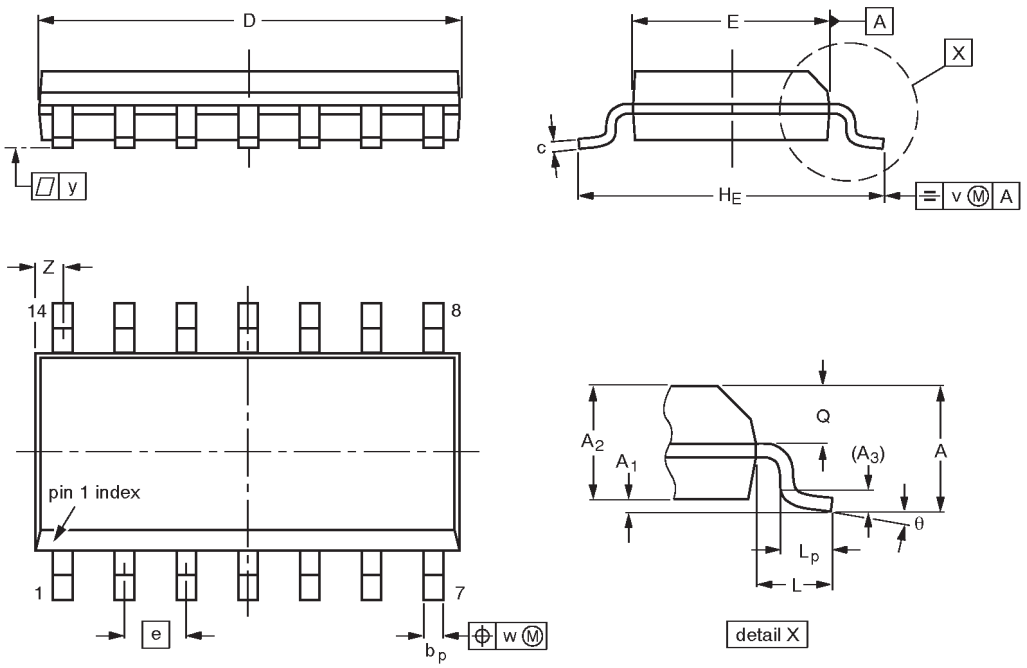
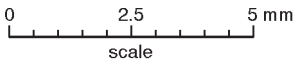
SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

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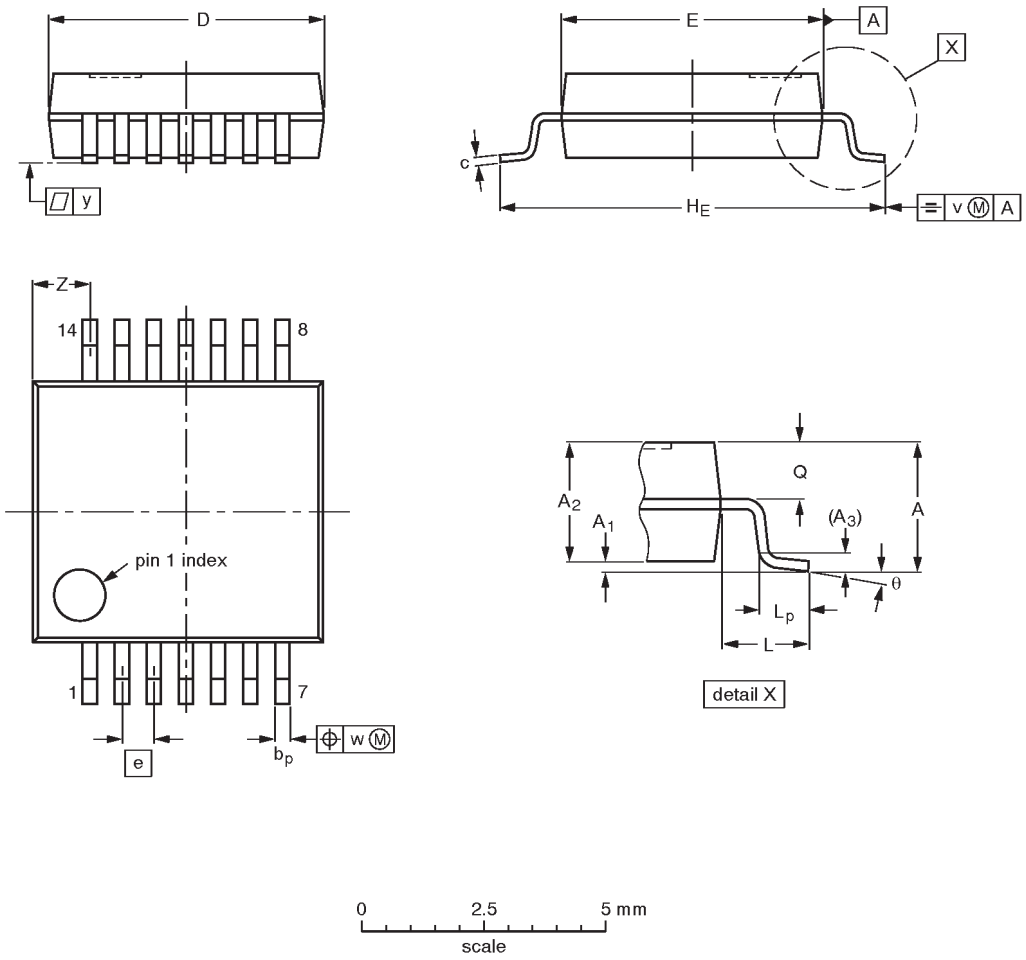
SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~95-02-04~~ 96-01-18

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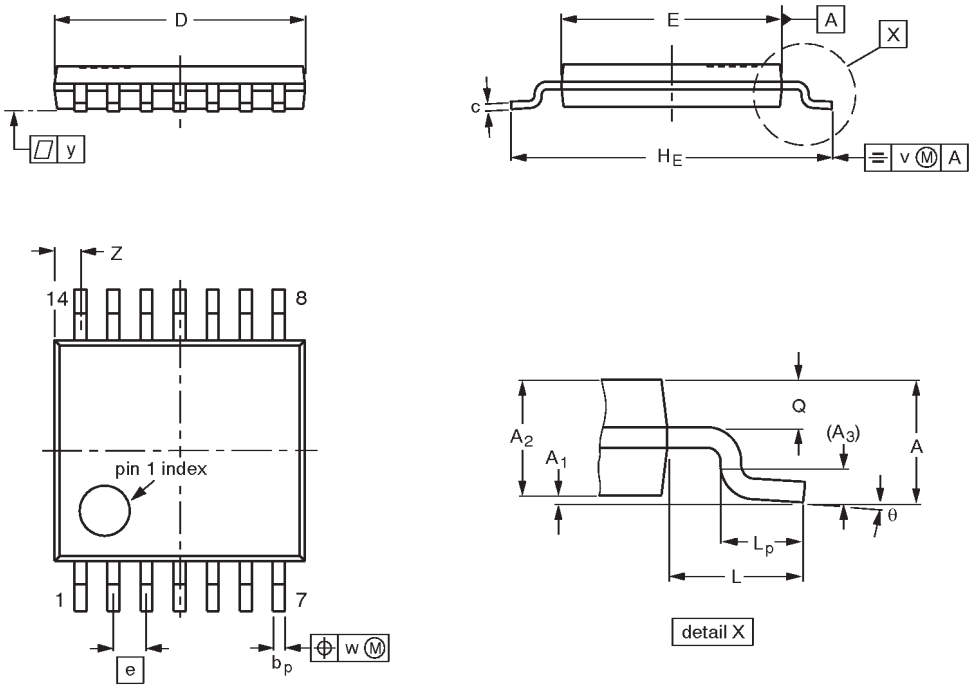
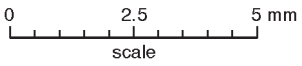
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~94-07-12~~ 95-04-04

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