

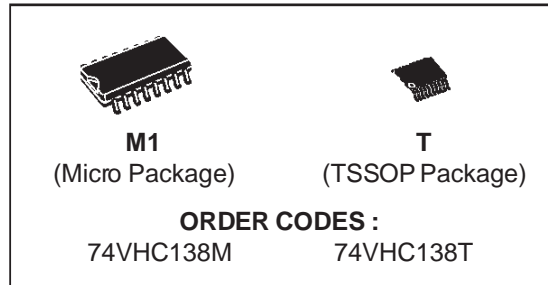
## 3 TO 8 LINE DECODER (INVERTING)

- HIGH SPEED:  $t_{PD} = 5.7 \text{ ns}$  (TYP.) at  $V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4 \mu\text{A}$  (MAX.) at  $T_A = 25 \text{ }^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 2V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH  
74 SERIES 138
- IMPROVED LATCH-UP IMMUNITY

### DESCRIPTION

The 74VHC138 is an advanced high-speed CMOS 3 TO 8 LINE DECODER (INVERTING) fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

If the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs will go low. If enable input G1 is held low or either



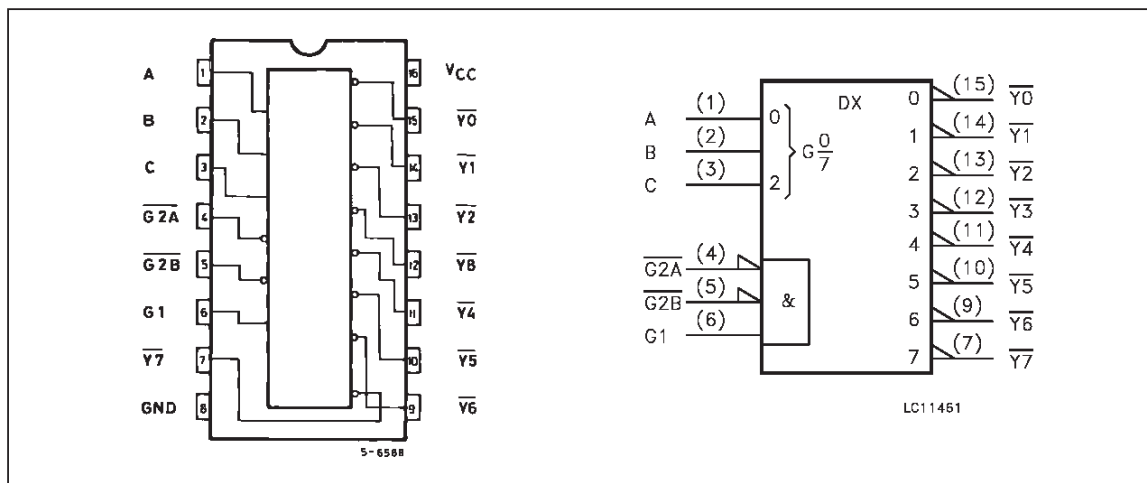
$\overline{G2A}$  or  $\overline{G2B}$  is held high, the decoding function is inhibited and all the 8 outputs go to high.

Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems.

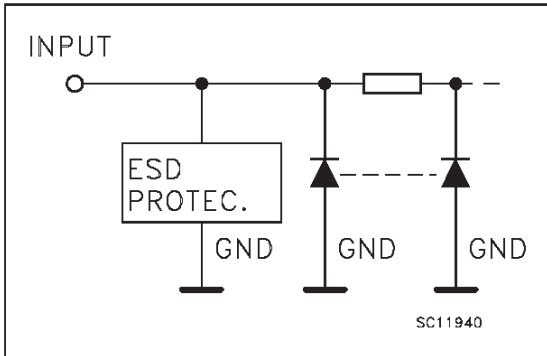
Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

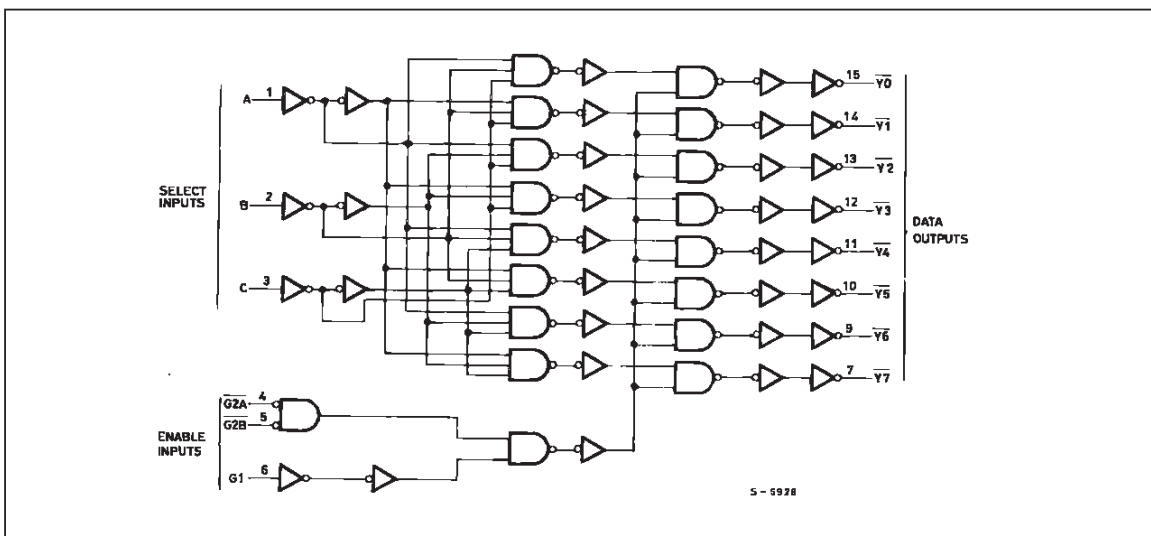
PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5	$\overline{G2A}$ , $\overline{G2B}$	Enable Inputs
6	G1	Enable Input
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ to $\overline{Y7}$	Outputs
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT			$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A								
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X: Don't Care

LOGIC DIAGRAM



This logic diagram has not been used to estimate propagation delays

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 20	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 75$	mA
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	2.0 to 5.5	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-40 to +85	$^{\circ}C$
dt/dv	Input Rise and Fall Time (see note 1) ( $V_{CC} = 3.3 \pm 0.3V$ ) ( $V_{CC} = 5.0 \pm 0.5V$ )	0 to 100 0 to 20	ns/V ns/V

1)  $V_{IN}$  from 30% to 70% of  $V_{CC}$

## DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
				$T_A = 25^{\circ}C$			$-40$ to $85^{\circ}C$		
				$V_{CC}$ (V)	Min.	Typ.	Max.	Min.	
$V_{IH}$	High Level Input Voltage	2.0		1.5			1.5		V
		3.0 to 5.5		$0.7V_{CC}$			$0.7V_{CC}$		
$V_{IL}$	Low Level Input Voltage	2.0				0.5		0.5	V
		3.0 to 5.5				$0.3V_{CC}$		$0.3V_{CC}$	
$V_{OH}$	High Level Output Voltage	2.0	$I_O = -50 \mu A$	1.9	2.0		1.9		V
		3.0	$I_O = -50 \mu A$	2.9	3.0		2.9		
		4.5	$I_O = -50 \mu A$	4.4	4.5		4.4		
		3.0	$I_O = -4 mA$	2.58			2.48		
		4.5	$I_O = -8 mA$	3.94			3.8		
$V_{OL}$	Low Level Output Voltage	2.0	$I_O = 50 \mu A$		0.0	0.1		0.1	V
		3.0	$I_O = 50 \mu A$		0.0	0.1		0.1	
		4.5	$I_O = 50 \mu A$		0.0	0.1		0.1	
		3.0	$I_O = 4 mA$			0.36		0.44	
		4.5	$I_O = 8 mA$			0.36		0.44	
$I_I$	Input Leakage Current	0 to 5.5	$V_I = 5.5V$ or GND			$\pm 0.1$		$\pm 1.0$	$\mu A$
$I_{CC}$	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND			4		40	$\mu A$

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r = t_f = 3 \text{ ns}$ )

Symbol	Parameter	Test Condition		Value					Unit
		$V_{CC}$ (V)	$C_L$ (pF)	$T_A = 25 \text{ }^\circ\text{C}$			$-40 \text{ to } 85 \text{ }^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time A, B, C to $\bar{Y}$	3.3 <sup>(*)</sup>	15		8.2	11.4	1.0	13.5	ns
		3.3 <sup>(*)</sup>	50		10.0	15.8	1.0	18.0	
		5.0 <sup>(**)</sup>	15		5.7	8.1	1.0	9.5	
		5.0 <sup>(**)</sup>	50		7.2	10.1	1.0	11.5	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time G1 to $\bar{Y}$	3.3 <sup>(*)</sup>	15		8.1	12.8	1.0	15.0	ns
		3.3 <sup>(*)</sup>	50		10.6	16.3	1.0	18.5	
		5.0 <sup>(**)</sup>	15		5.6	8.1	1.0	9.5	
		5.0 <sup>(**)</sup>	50		7.1	10.1	1.0	11.5	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time G2A, G2B to $\bar{Y}$	3.3 <sup>(*)</sup>	15		8.2	11.4	1.0	13.5	ns
		3.3 <sup>(*)</sup>	50		10.7	14.9	1.0	17.0	
		5.0 <sup>(**)</sup>	15		5.8	8.1	1.0	9.5	
		5.0 <sup>(**)</sup>	50		7.3	10.1	1.0	11.5	

(\*) Voltage range is  $3.3V \pm 0.3V$

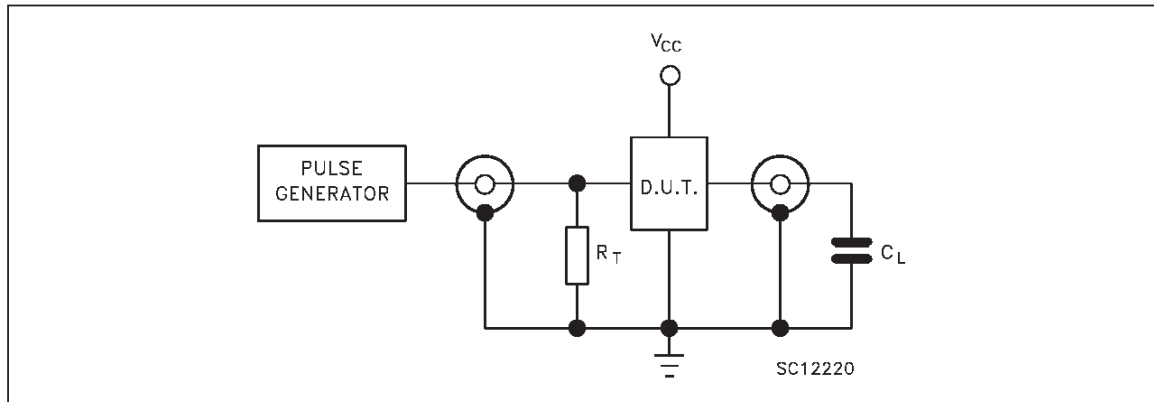
(\*\*) Voltage range is  $5V \pm 0.5V$

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Value				Unit	
			$T_A = 25 \text{ }^\circ\text{C}$			$-40 \text{ to } 85 \text{ }^\circ\text{C}$		
			Min.	Typ.	Max.	Min.		Max.
$C_{IN}$	Input Capacitance			4	10		10	pF
$C_{PD}$	Power Dissipation Capacitance (note 1)			34				pF

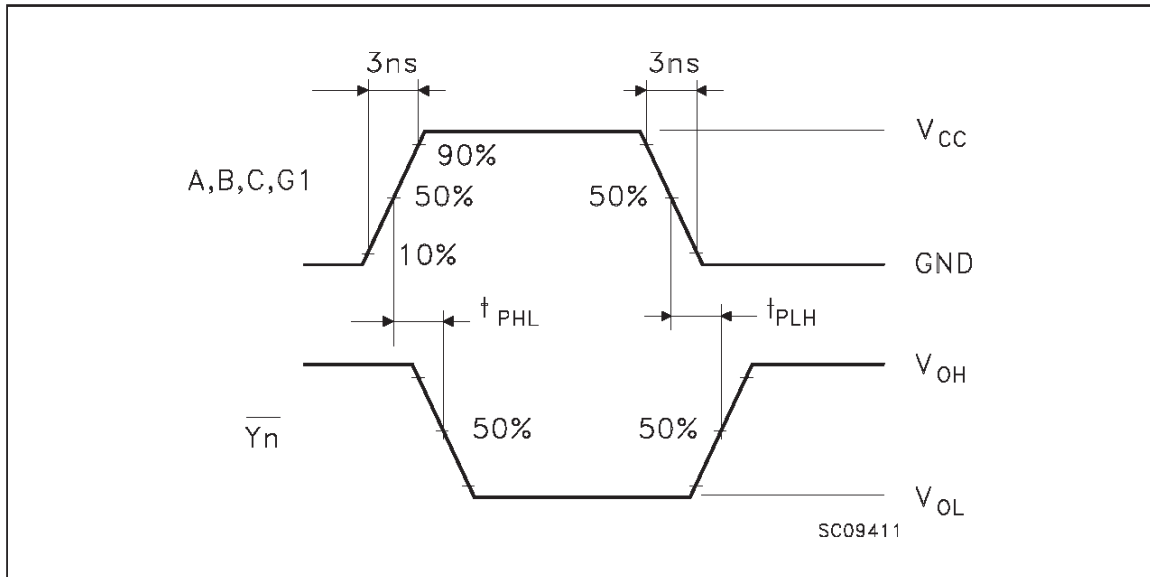
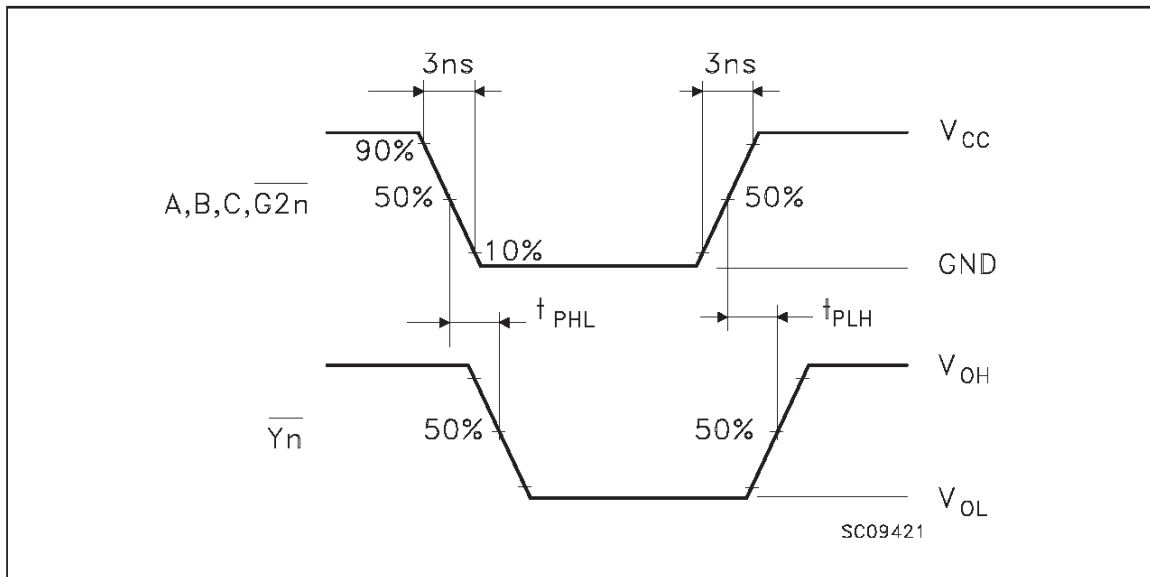
1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

**TEST CIRCUIT**



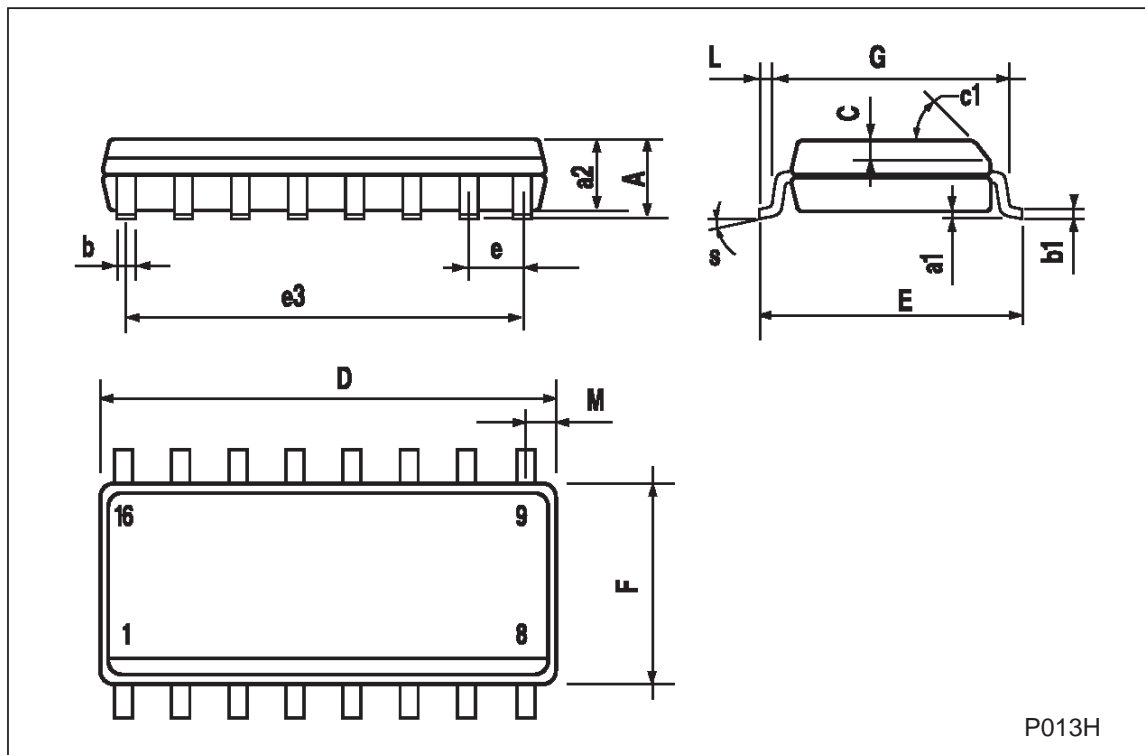
$C_L = 15/50 \text{ pF}$  or equivalent (includes jig and probe capacitance)

$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING OUTPUTS** (f=1MHz; 50% duty cycle)**WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING OUTPUTS** (f=1MHz; 50% duty cycle)

## SO-16 MECHANICAL DATA

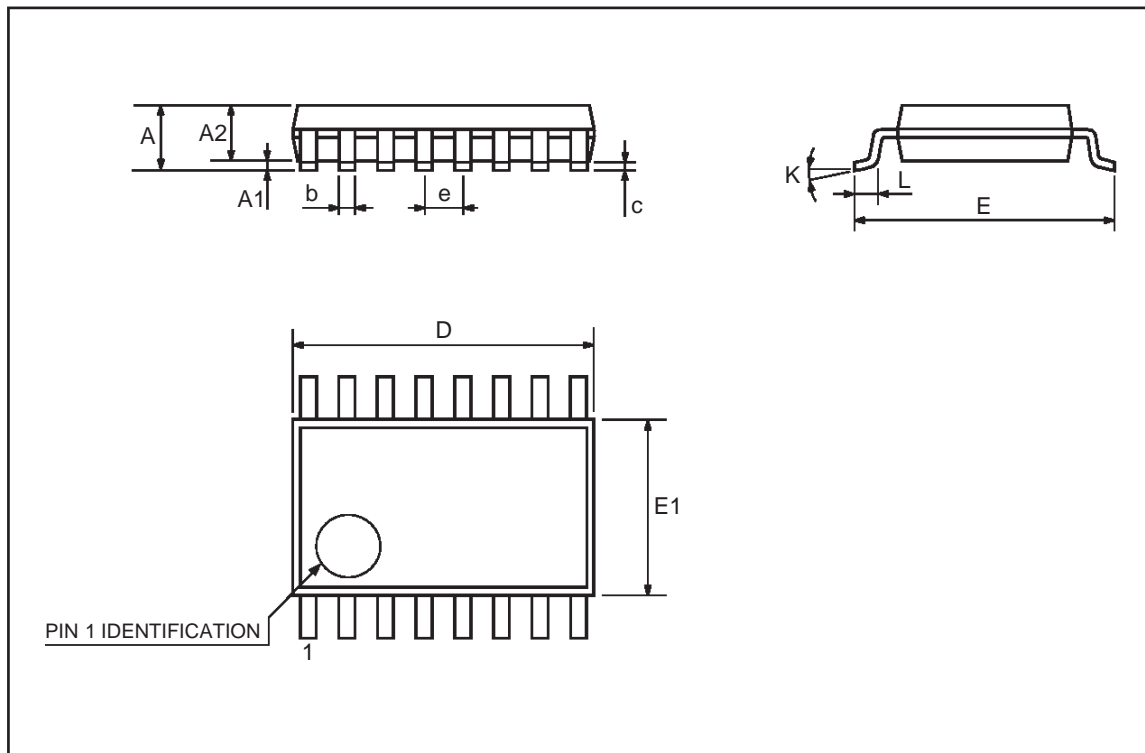
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



P013H

## TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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