DS2151Q
T1 Single-Chip Transceiver

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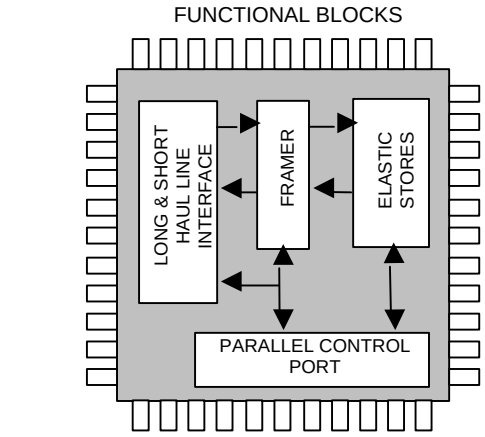
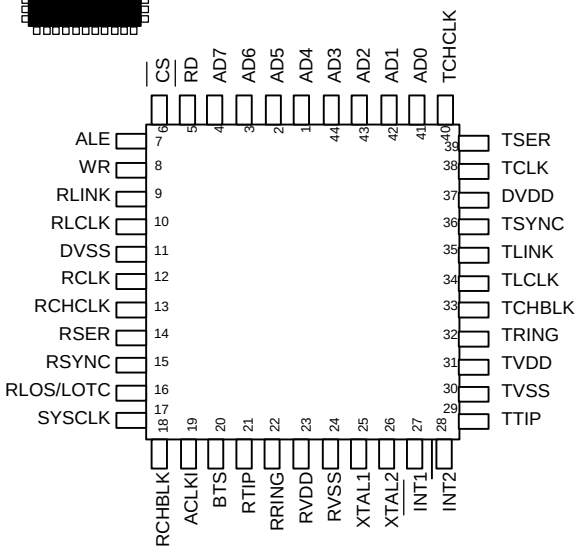
FEATURES

- Complete DS1/ISDN-PRI transceiver functionality
- Line interface can handle both long- and short-haul trunks
- 32-bit or 128-bit jitter attenuator
- Generates DSX-1 and CSU line build outs
- Frames to D4, ESF, and SLC-96^{R} formats
- Dual onboard two-frame elastic store slip buffers that connect to backplanes up to 8.192 MHz
- 8-bit parallel control port that can be used on either multiplexed or non-multiplexed buses
- Extracts and inserts Robbed-Bit signaling
- Detects and generates yellow and blue alarms
- Programmable output clocks for Fractional T1
- Fully independent transmit and receive functionality
- Onboard FDL support circuitry
- Generates and detects CSU loop codes
- Contains ANSI one's density monitor and enforcer
- Large path and line error counters including BPV, CV, CRC6, and framing bit errors
- Pin compatible with DS2153Q E1 Single-Chip Transceiver
- 5V supply; low power CMOS
- Industrial grade version (-40°C to +85°C) available (DS2151QN)

PIN ASSIGNMENT



ACTUAL SIZE OF 44-PIN PLCC



DESCRIPTION

The DS2151Q T1 Single-Chip Transceiver (SCT) contains all of the necessary functions for connection to T1 lines whether they be DS-1 long haul or DSX-1 short haul. The clock recovery circuitry automatically adjusts to T1 lines from 0 feet to over 6000 feet in length. The device can generate both DSX-1 line build outs as well as CSU build outs of -7.5 dB, -15 dB, and -22.5 dB. The onboard jitter attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting Robbed-Bit signaling data and FDL data. The device contains a set of 64 8-bit internal registers which the user can access to control the operation of the unit. Quick access via the parallel control port allows a single micro to handle many T1 lines. The device fully meets all of the latest T1 specifications including ANSI T1.403-199X, AT&T TR 62411 (12-90), and ITU G.703, G.704, G.706, G.823, and I.431.

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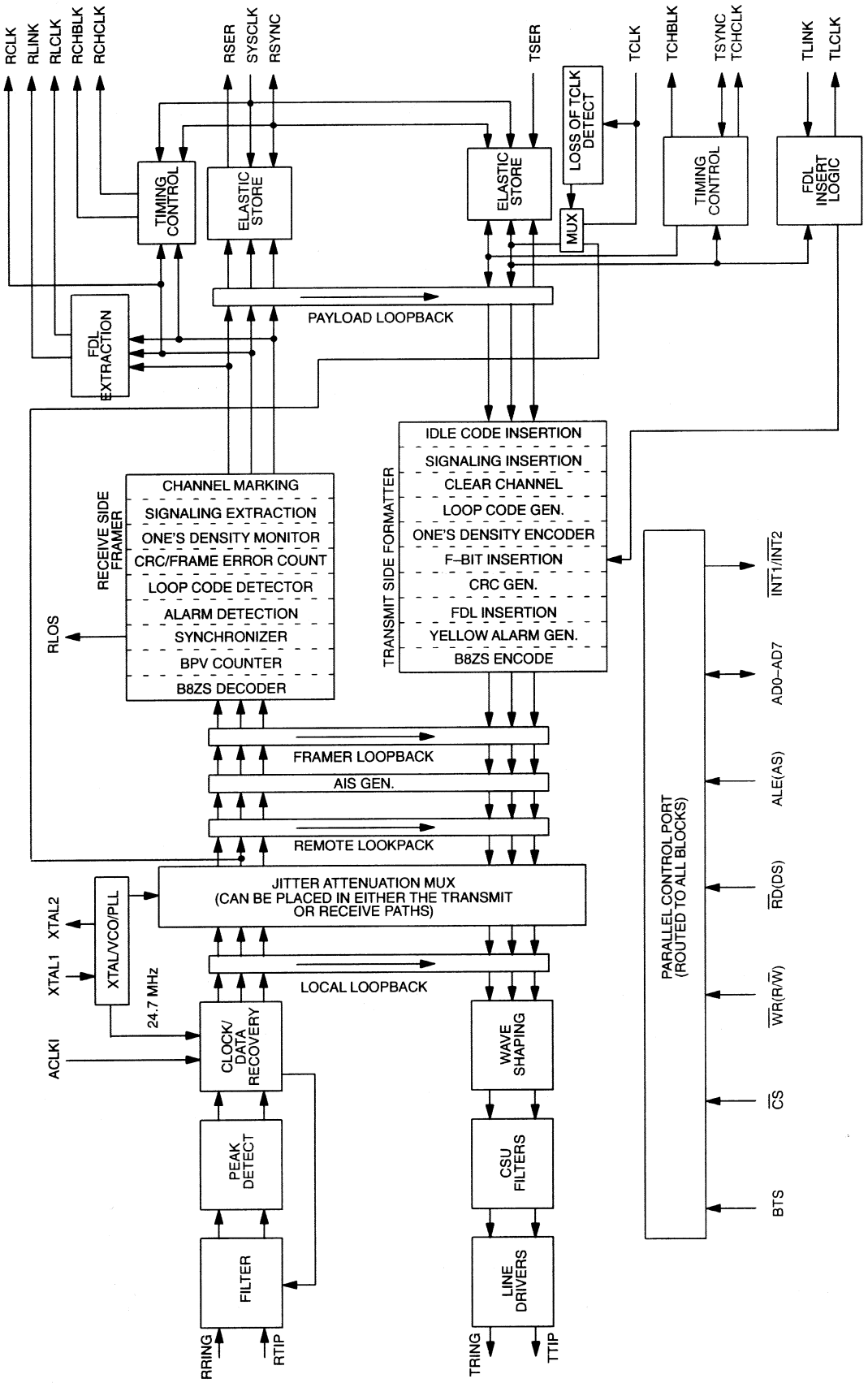
1.0 INTRODUCTION

The analog AMI waveform off of the T1 line is transformer coupled into the RRING and RTIP pins of the DS2151Q. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing pattern. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered T1 data stream and an asynchronous backplane clock which is provided at the SYSCLK input.

The transmit side of the DS2151Q is totally independent from the receive side in both the clock requirements and characteristics. Data can be either provided directly to the transmit formatter or via an elastic store. The transmit formatter will provide the necessary data overhead for T1 transmission. Once the data stream has been prepared for transmission, it is sent via the jitter attenuation mux to the waveshaping and line driver functions. The DS2151Q will drive the T1 line from the TTIP and TRING pins via a coupling transformer.

DS2151Q BLOCK DIAGRAM Figure 1-1



PIN DESCRIPTION Table 1-1

PIN	SYMBOL	TYPE	DESCRIPTION
1 2 3 4	AD4 AD5 AD6 AD7	I/O	**Address/Data Bus.** An 8-bit multiplexed address/data bus.
5	$\overline{RD}$ (DS)	I	**Read Input (Data Strobe).**
6	$\overline{CS}$	I	**Chip Select.** Must be low to read or write the port.
7	ALE(AS)	I	**Address Latch Enable (Address Strobe).** A positive going edge serves to demultiplex the bus.
8	$\overline{WR}$ (R/$\overline{W}$)	I	**Write Input (Read/Write).**
9	RLINK	O	**Receive Link Data.** Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame. See Section 13 for timing details.
10	RLCLK	O	**Receive Link Clock.** 4 kHz or 2 kHz (ZBTSI) demand clock for the RLINK output. See Section 13 for timing details.
11	DVSS	-	**Digital Signal Ground.** 0.0 volts. Should be tied to local ground plane.
12	RCLK	O	**Receive Clock**. Recovered 1.544 MHz clock.
13	RCHCLK	O	**Receive Channel Clock**. 192 kHz clock which pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data, locating Robbed-Bit signaling bits, and for blocking clocks in DDS applications. See Section 13 for timing details.
14	RSER	O	**Receive Serial Data.** Received NRZ serial data, updated on rising edges of RCLK or SYSCLK.
15	RSYNC	I/O	**Receive Sync.** An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR2.4=0) or multiframe boundaries (RCR2.4=1). If set to output frame boundaries, then via RCR2.5, RSYNC can also be set to output double-wide pulses on signaling frames. If the elastic store is enabled via the CCR1.2, then this pin can be enabled to be an input via RCR2.3 at which a frame boundary pulse is applied. See Section 13 for timing details.
16	RLOS/LOTC	O	**Receive Loss of Sync/Loss of Transmit Clock.** A dual function output. If CCR3.5=0, will toggle high when the synchronizer is searching for the T1 frame and multiframe; if CCR3.5=1, will toggle high if the TCLK pin has not toggled for 5 us.
17	SYSCLK	I	**System Clock.** 1.544 MHz or 2.048 MHz clock. Only used when the elastic store functions are enabled via either CCR1.7 or CCR1.2. Should be tied low in applications that do not use the elastic store. If tied high for more than 100 us, will force all output pins (including the parallel port) to 3-state.
18	RCHBLK	O	**Receive Channel Block.** A user programmable output that can be forced high or low during any of the 24 T1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384k bps service, 768k bps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Section 13 for timing details.

PIN	SYMBOL	TYPE	DESCRIPTION
19	ACLKI	I	**Alternate Clock Input.** Upon a receive carrier loss, the clock applied at this pin (normally 1.544 MHz) will be routed to the RCLK pin. If no clock is routed to this pin, then it should be tied to DVSS VIA A1K Ohm RESISTOR.
20	BTS	I	**Bus Type Select.** Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{RD}$ (DS), ALE(AS), and $\overline{WR}$ (R/$\overline{W}$) pins. If BTS=1, then these pins assume the function listed in parenthesis ().
21 22	RTIP RRING	-	**Receive Tip and Ring.** Analog inputs for clock recovery circuitry; connects to a 1:1 transformer (see Section 12 for details).
23	RVDD	-	**Receive Analog Positive Supply**. 5.0 volts. Should be tied to DVDD and TVDD pins.
24	RVSS	-	**Receive Signal Ground**. 0.0 volts. Should be tied to local ground plane
25 26	XTAL1 XTAL2	-	**Crystal Connections.** A pullable 6.176 MHz crystal must be applied to these pins. See Section 12 for crystal specifications.
27	$\overline{INT1}$	O	**Receive Alarm Interrupt 1.** Flags host controller during alarm conditions defined in Status Register 1. Active low, open drain output.
28	$\overline{INT2}$	O	**Receive Alarm Interrupt 2.** Flags host controller during conditions defined in Status Register 2. Active low, open drain output.
29	TTIP	-	**Transmit Tip.** Analog line driver output; connects to a step-up transformer (see Section 12 for details).
30	TVSS	-	**Transmit Signal Ground.** 0.0 volts. Should be tied to local ground plane.
31	TVDD	-	**Transmit Analog Positive Supply.** 5.0 volts. Should be tied to DVDD and RVDD pins.
32	TRING	-	**Transmit Ring**. Analog line driver outputs; connects to a step-up transformer (see Section 12 for details).
33	TCHBLK	O	**Transmit Channel Block**. A user programmable output that can be forced high or low during any of the 24 T1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384k bps service, 768k bps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Section 13 for timing details.
34	TLCLK	O	**Transmit Link Clock.** 4 kHz or 2 kHz (ZBTSI) demand clock for the TLINK input. See Section 13 for timing details.
35	TLINK	I	**Transmit Link Data.** If enabled via TCR1.2, this pin will be sampled during the F-bit time on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs bit position (D4) or the Z-bit position (ZBTSI). See Section 13 for timing details.
36	TSYNC	I/O	**Transmit Sync.** A pulse at this pin will establish either frame or multiframe boundaries for the DS2151Q. Via TCR2.2, the DS2151Q can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double-wide pulses at signaling frames. See Section 13 for timing details.
37	DVDD	-	**Digital Positive Supply.** 5.0 volts. Should be tied to RVDD and TVDD pins.

PIN	SYMBOL	TYPE	DESCRIPTION
38	TCLK	I	**Transmit Clock.** 1.544 MHz primary clock.
39	TSER	I	**Transmit Serial Data.** Transmit NRZ serial data, sampled on the falling edge of TCLK.
40	TCHCLK	O	**Transmit Channel Clock.** 192 kHz clock which pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data, locating Robbed-Bit signaling bits, and for blocking clocks in DDS applications. See Section 13 for timing details.
41 42 43 44	AD0 AD1 AD2 AD3	I/O	**Address/Data Bus.** An 8-bit multiplexed address/data bus.

DS2151Q REGISTER MAP

ADDRESS	R/W	REGISTER NAME	ADDRESS	R/W	REGISTER NAME
20	R/W	Status Register 1.	30	R/W	Common Control Register 3.
21	R/W	Status Register 2.	31	R/W	Receive Information Register 2.
22	R/W	Receive Information Register 1.	32	R/W	Transmit Channel Blocking Register 1.
23	R	Line code Violation Count Register 1.	33	R/W	Transmit Channel Blocking Register 2.
24	R	Line code Violation Count Register 2.	34	R/W	Transmit Channel Blocking Register 3.
25	R	Path Code Violation Count Register 1. (1)	35	R/W	Transmit Control Register 1.
26	R	Path Code Violation Count Register 2.	36	R/W	Transmit Control Register 2.
27	R	Multiframe Out of Sync Count Register 2.	37	R/W	Common Control Register 1.
28	R	Receive FDL Register.	38	R/W	Common Control Register 2.
29	R/W	Receive FDL Match Register 1.	39	R/W	Transmit Transparency Register 1.
2A	R/W	Receive FDL Match Register 2.	3A	R/W	Transmit Transparency Register 2.
2B	R/W	Receive Control Register 1.	3B	R/W	Transmit Transparency Register 3.
2C	R/W	Receive Control Register 2.	3C	R/W	Transmit Idle Register 1.
2D	R/W	Receive Mark Register 1.	3D	R/W	Transmit Idle Register 2.
2E	R/W	Receive Mark Register 2.	3E	R/W	Transmit Idle Register 3.
2F	R/W	Receive Mark Register 3.	3F	R/W	Transmit Idle Definition Register.
60	R	Receive Signaling Register 1.	70	R/W	Transmit Signaling Register 1.
61	R	Receive Signaling Register 2.	71	R/W	Transmit Signaling Register 2.
62	R	Receive Signaling Register 3.	72	R/W	Transmit Signaling Register 3.

DS2151Q REGISTER MAP (continued)

63	R	Receive Signaling Register 4.	73	R/W	Transmit Signaling Register 4.
64	R	Receive Signaling Register 5.	74	R/W	Transmit Signaling Register 5.
65	R	Receive Signaling Register 6.	75	R/W	Transmit Signaling Register 6.
66	R	Receive Signaling Register 7.	76	R/W	Transmit Signaling Register 7.
67	R	Receive Signaling Register 8.	77	R/W	Transmit Signaling Register 8.
68	R	Receive Signaling Register 9.	78	R/W	Transmit Signaling Register 9.
69	R	Receive Signaling Register 10.	79	R/W	Transmit Signaling Register 10.
6A	R	Receive Signaling Register 11.	7A	R/W	Transmit Signaling Register 11.
6B	R	Receive Signaling Register 12.	7B	R/W	Transmit Signaling Register 12.
6C	R/W	Receive Channel Blocking Register 1.	7C	R/W	Line Interface Control Register.
6D	R/W	Receive Channel Blocking Register 2.	7D	R/W	Test Register. (2)
6E	R/W	Receive Channel Blocking Register 3.	7E	R/W	Transmit FDL Register.
6F	R/W	Interrupt Mask Register 2.	7F	R/W	Interrupt Mask Register 1.

NOTES:

1. Address 25 also contains Multiframe Out of Sync Count Register 1.

2. The Test Register is used only by the factory; this register must be cleared (set to all 0s) on power-up initialization to insure proper operation.

2.0 PARALLEL PORT

The DS2151Q is controlled via a multiplexed bidirectional address/data bus by an external microcontroller or microprocessor. The DS2151Q can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the A.C. Electrical Characteristics for more details. The multiplexed bus on the DS2151Q saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE (AS), at which time the

DS2151Q latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS or $\overline{WR}$ pulses. In a read cycle, the DS2151Q outputs a byte of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high in Intel timing or as DS transitions low in Motorola timing. The DS2151Q can also be easily connected to non-multiplexed buses. Please see the separate Application Note for a detailed discussion of this topic.

3.0 CONTROL REGISTERS

The operation of the DS2151Q is configured via a set of eight registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2151Q has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), a Line Interface Control Register (LICR), and three Common Control Registers (CCR1, CCR2, and CCR3). Seven of the eight registers are described below. The LICR is described in Section 12.

RCR1: RECEIVE CONTROL REGISTER 1 (Address=2B Hex)

(MSB)							**(LSB)**
LCVCRF	ARC	OOF1	OOF2	SYNCC	SYNCT	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
LCVCRF	RCR1.7	**Line Code Violation Count Register Function Select.** 0=do not count excessive 0s 1=count excessive 0s
ARC	RCR1.6	**Auto Resync Criteria.** 0=Resync on OOF or RCL event 1=Resync on OOF only
OOF1	RCR1.5	**Out Of Frame Select 1.** 0=2/4 frame bits in error 1=2/5 frame bits in error
OOF2	RCR1.4	**Out Of Frame Select 2.** 0=follow RCR1.5 1=2/6 frame bits in error
SYNCC	RCR1.3	**Sync Criteria.** In D4 Framing Mode 0=search for Ft pattern, then search for Fs pattern 1=cross couple Ft and Fs pattern In ESF Framing Mode 0=search for FPS pattern only 1=search for FPS and verify with CRC6
SYNCT	RCR1.2	**Sync Time**. 0=qualify 10 bits 1=qualify 24 bits

SYNCE	RCR1.1	**Sync Enable**. 0=auto resync enabled 1=auto resync disabled
RESYNC	RCR1.0	**Resync**. When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync.

RCR2: RECEIVE CONTROL REGISTER 2 (Address=2C Hex)

(MSB)							(LSB)
RCS	RZBTSI	RSDW	RSM	RSIO	RD4YM	FSBE	MOSCRF

SYMBOL	POSITION	NAME AND DESCRIPTION
RCS	RCR2.7	**Receive Code Select.** 0=idle code (7F Hex) 1=digital milliwatt code (1E/0B/0B/1E/9E/8B/8B/9E Hex)
RZBTSI	RCR2.6	**Receive Side ZBTSI Enable.** 0=ZBTSI disabled 1=ZBTSI enabled
RSDW	RCR2.5	**RSYNC Double-Wide.** 0=do not pulse double-wide in signaling frames 1=do pulse double-wide in signaling frames (note: this bit must be set to 0 when RCR2.4=1 or when RCR2.3=1)
RSM	RCR2.4	**RSYNC Mode Select.** 0=frame mode (see the timing in Section 13) 1=multiframe mode (see the timing in Section 13)
RSIO	RCR2.3	**RSYNC I/O Select.** 0=RSYNC is an output 1=RSYNC is an input (only valid if elastic store enabled) (note: this bit must be set to 0 when CCR1.2=0)
RD4YM	RCR2.2	**Receive Side D4 Yellow Alarm Select.** 0=0s in bit 2 of all channels 1=a 1 in the S-bit position of frame 12
FSBE	RCR2.1	**PCVCR Fs Bit Error Report Enable.** 0=do not report bit errors in Fs bit position; only Ft bit position 1=report bit errors in Fs bit position as well as Ft bit position
MOSCRF	RCR2.0	**Multiframe Out of Sync Count Register Function Select**. 0=count errors in the framing bit position 1=count the number of multiframes out of sync

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=35 Hex)

(MSB)							(LSB)
LOTCMC	TFPT	TCPT	RBSE	GB7S	TLINK	TBL	TYEL

SYMBOL	POSITION	NAME AND DESCRIPTION

LOTCMC	TCR1.7	**Loss Of Transmit Clock Mux Control**. Determines whether the transmit side formatter should switch to the ever present RCLK if the TCLK input should fail to transition (see Figure 1-1 for more details). 0=do not switch to RCLK if TCLK stops 1=switch to RCLK if TCLK stops
TFPT	TCR1.6	**Transmit Framing Pass Through**. (see note below) 0=Ft or FPS bits sourced internally 1=Ft or FPS bits sampled at TSER during F-bit time
TCPT	TCR1.5	**Transmit CRC Pass Through**. (see note below) 0=source CRC6 bits internally 1=CRC6 bits sampled at TSER during F-bit time
RBSE	TCR1.4	**Robbed-Bit Signaling Enable**. (see note below) 0=no signaling is inserted in any channel 1=signaling is inserted in all channels (the TTR registers can be used to block insertion on a channel by channel basis)
GB7S	TCR1.3	**Global Bit 7 Stuffing**. (see note below) 0=allow the TTR registers to determine which channels containing all 0s are to be Bit 7 stuffed 1=force Bit 7 stuffing in all 0 byte channels regardless of how the TTR registers are programmed
TLINK	TCR1.2	**TLINK Select**. (see note below) 0=source FDL or Fs bits from TFDL register 1=source FDL or Fs bits from the TLINK pin
TBL	TCR1.1	**Transmit Blue Alarm**. (see note below) 0=transmit data normally 1=transmit an unframed all 1s code at TPOS and TNEG
TYEL	TCR1.0	**Transmit Yellow Alarm**. (see note below) 0=do not transmit yellow alarm 1=transmit yellow alarm

Note: for a detailed description of how the bits in TCR1 affect the transmit side formatter of the DS2151Q, please see Figure 13-9.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=36 Hex)

(MSB)							(LSB)
TEST1	TEST0	TZBTSI	TSDW	TSM	TSIO	TD4YM	B7ZS

SYMBOL	POSITION	NAME AND DESCRIPTION
TEST1	TCR2.7	**Test Mode Bit 1 for Output Pins.** See Table 3-1.
TEST0	TCR2.6	**Test Mode Bit 0 for Output Pins.** See Table 3-1.
TZBTSI	TCR2.5	**Transmit Side ZBTSI Enable.** 0=ZBTSI disabled 1=ZBTSI enabled
TSDW	TCR2.4	**TSYNC Double-Wide.** (note: this bit must be set to 0 when TCR2.3=1 or when TCR2.2=0) 0=do not pulse double-wide in signaling frames 1=do pulse double-wide in signaling frames
TSM	TCR2.3	**TSYNC Mode Select.** 0=frame mode (see the timing in Section 13) 1=multiframe mode (see the timing in Section 13)
TSIO	TCR2.2	**TSYNC I/O Select.** 0=TSYNC is an input 1=TSYNC is an output
TD4YM	TCR2.1	**Transmit Side D4 Yellow Alarm Select.** 0=0s in bit 2 of all channels 1=a 1 in the S-bit position of frame 12
B7ZS	XTCR2.0	**Bit 7 0 Suppression Enable.** 0=no stuffing occurs 1=Bit 7 force to a 1 in channels with all 0s

OUTPUT PIN TEST MODES Table 3-1

TEST1	TEST0	EFFECT ON OUTPUT PINS
0	0	operate normally
0	1	force all output pins 3-state (including all I/O pins and parallel port pins)
1	0	force all output pins low (including all I/O pins except parallel port pins)
1	1	force all output pins high (including all I/O pins except parallel port pins)

CCR1: COMMON CONTROL REGISTER 1 (Address=37 Hex)

(MSB)							(LSB)
TESE	LLB	RSAO	RLB	SCLKM	RESE	PLB	FLB

SYMBOL	POSITION	NAME AND DESCRIPTION
TESE	CCR1.7	**Transmit Elastic Store Enable.** 0=elastic store is bypassed 1=elastic store is enabled
LLB	CCR1.6	**Local Loopback.** 0=loopback disabled 1=loopback enabled
RSAO	CCR1.5	**Receive Signaling All 1s.** 0=allow robbed signaling bits to appear at RSER 1=force all robbed signaling bits at RSER to 1
RLB	CCR1.4	**Remote Loopback.** 0=loopback disabled 1=loopback enabled
SCLKM	CCR1.3	**SYSCLK Mode Select.** 0=if SYSCLK is 1.544 MHz 1=if SYSCLK is 2.048 MHz
RESE	CCR1.2	**Receive Elastic Store Enable.** 0=elastic store is bypassed 1=elastic store is enabled
PLB	CCR1.1	**Payload Loopback.** 0=loopback disabled 1=loopback enabled
FLB	CCR1.0	**Framer Loopback.** 0=loopback disabled 1=loopback enabled

LOCAL LOOPBACK

When CCR1.6 is set to a 1, the DS2151Q will be forced into Local LoopBack (LLB). In this loopback, data will continue to be transmitted as normal through the transmit side of the SCT. Data being received at RTIP and RRING will be replaced with the data being transmitted. Data in this loopback will pass through the jitter attenuator and the jitter attenuator should be programmed to be in the transmit path. LLB is primarily used in debug and test applications. Please see the DS2151Q Block Diagram in Section 1 for more details.

REMOTE LOOPBACK

When CCR1.4 is set to a 1, the DS2151Q will be forced into Remote LoopBack (RLB). In this loopback, data recovered off the T1 line from the RTIP and RRING pins will be transmitted back onto the T1 line

(with any BPVs that might have occurred intact) via the TTIP and TRING pins. Data will continue to pass through the receive side of the DS2151Q as it would normally and the data at the TSER input will be ignored. Data in this loopback will pass through the jitter attenuator. RLB is used to place the DS2151Q into "line" loopback which is a requirement of both ANSI T1.403 and AT&T TR62411. Please see the DS2151Q Block Diagram in Section 1 for more details.

PAYLOAD LOOPBACK

When CCR1.1 is set to a 1, the DS2151Q will be forced into Payload LoopBack (PLB). Normally, this loopback is only enabled when ESF framing is being performed. In a PLB situation, the DS2151Q will loop the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, they are reinserted by the DS2151Q. When PLB is enabled, the following will occur:

1. Data will be transmitted from the TTIP and TRING pins synchronous with RCLK instead of TCLK.

2. All of the receive side signals will continue to operate normally.

3. The TCHCLK and TCHBLK signals are forced low.

4. Data at the TSER pin is ignored.

5. The TLCLK signal will become synchronous with RCLK instead of TCLK.

FRAMER LOOPBACK

When CCR1.0 is set to a 1, the DS2151Q will enter a Framer LoopBack (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS2151Q will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. Unless the RLB is active, an unframed all 1s code will be transmitted at TTIP and TRING.

2. Data off the T1 line at RTIP and RRING will be ignored.

3. The RCLK output will be replaced with the TCLK input.

CCR2: COMMON CONTROL REGISTER 2 (Address=38 Hex)

(MSB)							(LSB)
TFM	TB8ZS	TSLC96	TFDL	RFM	RB8ZS	RSLC96	RFDL

SYMBOL	POSITION	NAME AND DESCRIPTION
TFM	CCR2.7	**Transmit Frame Mode Select.** 0=D4 framing mode 1=ESF framing mode
TB8ZS	CCR2.6	**Transmit B8ZS Enable.** 0=B8ZS disabled 1=B8ZS enabled
TSLC96	CCR2.5	**Transmit SLC-96/Fs Bit Loading Enable.** 0=SLC-96/Fs bit Loading disabled 1=SLC-96/Fs bit Loading enabled
TFDL	CCR2.4	**Transmit FDL 0 Stuffer Enable.** 0=0 stuffer disabled 1=0 stuffer enabled
RFM	CCR2.3	**Receive Frame Mode Select.** 0=D4 framing mode 1=ESF framing mode
RB8ZS	CCR2.2	**Receive B8ZS Enable.** 0=B8ZS disabled 1=B8ZS enabled
RSLC96	CCR2.1	**Receive SLC-96 Enable.** 0=SLC-96 disabled 1=SLC-96 enabled
RFDL	CCR2.0	**Receive FDL 0 Destuffer Enable.** 0=0 destuffer disabled 1=0 destuffer enabled

CCR3: COMMON CONTROL REGISTER 3 (Address=30 Hex)

(MSB)							(LSB)
ESMDM	ESR	P16F	RSMS	PDE	TLD	TLU	LIRST

SYMBOL	POSITION	NAME AND DESCRIPTION
ESMDM	CCR3.7	**Elastic Store Minimum Delay Mode.** See Section 10.3 for details. 0=elastic stores operate at full two-frame depth 1=elastic stores operate at 32-bit depth
ESR	CCR3.6	**Elastic Store Reset.** Setting this bit from a 0 to a 1 will force the elastic stores to a known depth. Should be toggled after SYSCLK has been applied and is stable. Must be cleared and set again for a subsequent reset.
P16F	CCR3.5	**Function of Pin 16.** 0=Receive Loss of Sync (RLOS). 1=Loss of Transmit Clock (LOTC).
RSMS	CCR3.4	**RSYNC Multiframe Skip Control.** Useful in framing format conversions from D4 to ESF. 0=RSYNC will output a pulse at every multiframe 1=RSYNC will output a pulse at every other multiframe note: for this bit to have any affect, the RSYNC must be set to output multiframe pulses (RCR2.4=1 and RCR2.3=0) and the receive elastic store must be bypassed. (CCR1.2 = 0).
PDE	CCR3.3	**Pulse Density Enforcer Enable.** 0=disable transmit pulse density enforcer 1=enable transmit pulse density enforcer
TLD	CCR3.2	**Transmit Loop Down Code (001).** 0=transmit data normally 1=replace normal transmitted data with Loop Down code
TLU	CCR3.1	**Transmit Loop Up Code (00001).** 0=transmit data normally 1=replace normal transmitted data with Loop Up code
LIRST	CCR3.0	**Line Interface Reset.** Setting this bit from a 0 to a one will initiate an internal reset that affects the slicer, AGC, clock recovery state machine and jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.

LOOP CODE GENERATION

When either the CCR3.1 or CCR3.2 bits are set to 1, the DS2151Q will replace the normal transmitted payload with either the Loop Up or Loop Down code respectively. The DS2151Q will overwrite the repeating loop code pattern with the framing bits. The SCT will continue to transmit the loop codes as long as either bit is set. It is an illegal state to have both CCR3.1 and CCR3.2 set to 1 at the same time.

PULSE DENSITY ENFORCER

The SCT always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403-199X:

- no more than 15 consecutive 0s
- at least N 1s in each and every time window of 8 x (N +1) bits where N=1 through 23

Violations for the transmit and receive data streams are reported in the RIR2.0 and RIR2.1 bits respectively.

When the CCR3.3 is set to 1, the DS2151Q will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, the CCR3.3 bit should be set to 0, since B8ZS encoded data streams cannot violate the pulse density requirements.

POWER-UP SEQUENCE

On power-up, after the supplies are stable, the DS2151Q should be configured for operation by writing to all of the internal registers (this includes setting the Test Register to 00Hex) since the contents of the internal registers cannot be predicted on power-up. Next, the LIRST bit should be toggled from 0 to 1 to reset the line interface (it will take the DS2151Q about 40 ms to recover from the LIRST being toggled). Finally, after the SYSCLK input is stable, the ESR bit should be toggled from a 0 to a 1 (this step can be skipped if the elastic stores are disabled).

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS2151Q: Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register 1 (RIR1), and Receive Information Register 2 (RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a 1. All of the bits in these registers operate in a latched fashion. This means that if an event occurs and a bit is set to a 1 in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm(s) is still present.

The user will always precede a read of these registers with a write. The byte written to the register will inform the DS2151Q which bits the user wishes to read and have cleared. The user will write a byte to one of these four registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register will be updated with current value and the previous value will be cleared. When a 0 is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that the bit does indeed clear. This second write is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. The write-read-write scheme is unique to the four status registers and it allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2151Q with higher-order software languages.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ pins respectively. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked

from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively.

RIR1: RECEIVE INFORMATION REGISTER 1 (Address=22 Hex)

(MSB)							(LSB)
COFA	8ZD	16ZD	RESF	RESE	SEFE	B8ZS	FBE

SYMBOL	POSITION	NAME AND DESCRIPTION
COFA	RIR1.7	**Change of Frame Alignment.** Set when the last resync resulted in a change of frame or multiframe alignment.
8ZD	RIR1.6	**Eight 0 Detect.** Set when a string of eight consecutive 0s have been received at RPOS and RNEG.
16ZD	RIR1.5	**Sixteen 0 Detect.** Set when a string of 16 consecutive 0s have been received at RPOS and RNEG.
RESF	RIR1.4	**Receive Elastic Store Full.** Set when the receive elastic store buffer fills and a frame is deleted.
RESE	RIR1.3	**Receive Elastic Store Empty.** Set when the receive elastic store buffer empties and a frame is repeated.
SEFE	RIR1.2	**Severely Errored Framing Event.** Set when 2 out of 6 framing bits (Ft or FPS) are received in error.
B8ZS	RIR1.1	**B8ZS Code Word Detect.** Set when a B8ZS code word is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not via CCR2.6.
FBE	RIR1.0	**Frame Bit Error.** Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

RIR2: RECEIVE INFORMATION REGISTER 2 (Address=31 Hex)

(MSB)							(LSB)
RL1	RL0	TESF	TESE	TSLIP	JALT	RPDV	TPDV

SYMBOL	POSITION	NAME AND DESCRIPTION
RL1	RIR2.7	**Receive Level Bit 1.** See Table 4-1.
RL0	RIR2.6	**Receive Level Bit 0.** See Table 4-1.
TESF	RIR2.5	**Transmit Elastic Store Full.** Set when the transmit elastic store buffer fills and a frame is deleted.
TESE	RIR2.4	**Transmit Elastic Store Empty.** Set when the transmit elastic store buffer empties and a frame is repeated.
TSLIP	RIR2.3	**Transmit Elastic Store Slip Occurrence.** Set when the transmit elastic store has either repeated or deleted a frame.
JALT	RIR2.2	**Jitter Attenuator Limit Trip.** Set when the jitter attenuator FIFO reaches to within 4 bits of its limit; useful for debugging jitter attenuation operation.
RPDV	RIR2.1	**Receive Pulse Density Violation.** Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.
TPDV	RIR2.0	**Transmit Pulse Density Violation.** Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.

DS2151Q RECEIVE T1 LEVEL INDICATION Table 4-1

RL1	RL0	TYPICAL LEVEL RECEIVED
0	0	+2 dB to -7.5 dB
0	1	-7.5 dB to -15 dB
1	0	-15 dB to -22.5 dB
1	1	less than -22.5 Db

SR1: STATUS REGISTER 1 (Address=20 Hex)

(MSB)							(LSB)
LUP	LDN	LOTC	RSLIP	RBL	RYEL	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	SR1.7	**Loop Up Code Detected**. Set when the repeating ...00001... loop up code is being received.
LDN	SR1.6	**Loop Down Code Detected**. Set when the repeating ...001... loop down code is being received.
LOTC	SR1.5	**Loss of Transmit Clock**. Set when the TCLK pin has not transitioned for one channel time (or 5.2 us). Will force pin 16 high if enabled via CCR1.6. Based on RCLK.
RSLIP	SR1.4	**Receive Elastic Store Slip Occurrence**. Set when the receive elastic store has either repeated or deleted a frame.
RBL	SR1.3	**Receive Blue Alarm**. Set when a blue alarm is received at RTIP and RRING. See note below.
RYEL	SR1.2	**Receive Yellow Alarm**. Set when a yellow alarm is received at RTIP and RRING.
RCL	SR1.1	**Receive Carrier Loss**. Set when 192 consecutive 0s have been detected at RTIP and RRING.
RLOS	SR1.0	**Receive Loss of Sync**. Set when the device is not synchronized to the receive T1 stream.

DS2151Q ALARM SET AND CLEAR CRITERIA Table 4-2

ALARM	SET CRITERIA	CLEAR CRITERIA
Blue Alarm (AIS) (see note 1 below)	when over a 3 ms window, five or less 0s are received	when over a 3 ms window, six or more 0s are received
Yellow Alarm 1. D4 bit 2 mode (RCR2.2=0)	when bit 2 of 256 consecutive channels is set to 0 for at least 254 occurrences	when bit 2 of 256 consecutive channels is set to 0 for less than 254 occurrences
2. D4 12th F-bit mode (RCR2.2=1; this mode is also referred to as the "Japanese Yellow Alarm")	when the 12th framing bit is set to 1 for two consecutive occurrences	when the 12th framing bit is set to 0 for two consecutive occurrences
3. ESF Mode	when 16 consecutive patterns of 00FF hex appear in the FDL	when 14 or less patterns of 00FF hex out of 16 possible appear in the FDL
Red Alarm (RCL) (this alarm is also referred to as Loss of Signal)	when 192 consecutive 0s are received	when 14 or more 1s out of 112 possible bit positions are received starting with the first 1 received

NOTE:

1. The definition of Blue Alarm (or Alarm Indication Signal) is an unframed all 1s signal. Blue alarm detectors should be able to operate properly in the presence of a 10-3 error rate and they should not falsely trigger on a framed all 1s signal. The blue alarm criteria in the DS2151Q has been set to achieve this performance. It is recommended that the RBL bit be qualified with the RLOS status bit in detecting a blue alarm.

LOOP UP/DOWN CODE DETECTION

Bits SR1.7 and SR1.6 will indicate when either the standard Loop Up or Loop Down codes are being received by the DS2151Q. When a Loop Up code has been received for 5 seconds, the CPE is expected to loop the recovered data (without correcting BPVs) back to the source. The Loop Down code indicates that the loopback should be discontinued. See the AT&T publication TR 62411 for more details. The DS2151Q will detect the Loop Up/Down codes in both framed and unframed circumstances with bit error rates as high as 10**-2. The loop code detector has a nominal integration period of 48 ms. Hence, after about 48 ms of receiving either code, the proper status bit will be set to a 1. After this initial indication, it is recommended that the software poll the DS2151Q every 100 ms to 500 ms until 5 seconds have elapsed to insure that the code is continuously present. Once 5 seconds have passed, the DS2151Q should be taken into or out of loopback via the Remote Loopback (RLB) bit in CCR1.

SR2: STATUS REGISTER 2 (Address=21 Hex)

(MSB)							(LSB)
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	-

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	**Receive Multiframe**. Set on receive multiframe boundaries.
TMF	SR2.6	**Transmit Multiframe**. Set on transmit multiframe boundaries.
SEC	SR2.5	**One Second Timer**. Set on increments of 1 second based on RCLK; will be set in increments of 999 ms, 999 ms, and 1002 ms every 3 seconds.
RFDL	SR2.4	**Receive FDL Buffer Full**. Set when the receive FDL buffer (RFDL) fills to capacity (8 bits).
TFDL	SR2.3	**Transmit FDL Buffer Empty**. Set when the transmit FDL buffer (TFDL) empties.
RMTCH	SR2.2	**Receive FDL Match Occurrence**. Set when the RFDL matches either RFDLM1 or RFDLM2.
RAF	SR2.1	**Receive FDL Abort**. Set when eight consecutive 1s are received in the FDL.
-	SR2.0	**Not Assigned**. Should be set to 0 when written.

IMR1: INTERRUPT MASK REGISTER 1 (Address=7F Hex)

(MSB)							(LSB)
LUP	LDN	LOTC	SLIP	RBL	RYEL	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	IMR1.7	**Loop Up Code Detected.** 0=interrupt masked 1=interrupt enabled
LDN	IMR1.6	**Loop Down Code Detected.** 0=interrupt masked 1=interrupt enabled
LOTC	IMR1.5	**Loss of Transmit Clock.** 0=interrupt masked 1=interrupt enabled
SLIP	IMR1.4	**Elastic Store Slip Occurrence.** 0=interrupt masked 1=interrupt enabled
RBL	IMR1.3	**Receive Blue Alarm.** 0=interrupt masked 1=interrupt enabled
RYEL	IMR1.2	**Receive Yellow Alarm.** 0=interrupt masked 1=interrupt enabled
RCL	IMR1.1	**Receive Carrier Loss.** 0=interrupt masked 1=interrupt enabled
RLOS	IMR1.0	**Receive Loss of Sync.** 0=interrupt masked 1=interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address=6F Hex)

(MSB)							(LSB)
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	-

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	**Receive Multiframe.** 0=interrupt masked 1=interrupt enabled
TMF	IMR2.6	**Transmit Multiframe.** 0=interrupt masked 1=interrupt enabled
SEC	IMR2.5	**One-Second Timer.** 0=interrupt masked 1=interrupt enabled
RFDL	IMR2.4	**Receive FDL Buffer Full.** 0=interrupt masked 1=interrupt enabled
TFDL	IMR2.3	**Transmit FDL Buffer Empty.** 0=interrupt masked 1=interrupt enabled
RMTCH	IMR2.2	**Receive FDL Match Occurrence.** 0=interrupt masked 1=interrupt enabled
RAF	IMR2.1	**Receive FDL Abort.** 0=interrupt masked 1=interrupt enabled
-	IMR2.0	**Not Assigned.** Should be set to 0 when written to.

5.0 ERROR COUNT REGISTERS

There are a set of three counters in the DS2151Q that record bipolar violations, excessive 0s, errors in the CRC6 code words, framing bit errors, and number of multiframes that the device is out of receive synchronization. Each of these three counters are automatically updated on one second boundaries as determined by the one second timer in Status Register 2 (SR2.5). Hence, these registers contain performance data from the previous second. The user can use the interrupt from the 1-second timer to determine when to read these registers. The user has a full second to read the counters before the data is lost. All three counters will saturate at their respective maximum counts and they will not rollover (note: only the Line Code Violation Count Register has the potential to overflow).

5.1 Line Code Violation Count Register (LCVCR)

Line Code Violation Count Register 1 (LCVCR1) is the most significant word and LCVCR2 is the least significant word of a 16-bit counter that records code violations (CVs). CVs are defined as Bipolar Violations (BPVs) or excessive 0s. See Table 5-1 for details of exactly what the LCVCRs count. If the

B8ZS mode is set for the receive side via CCR2.2, then B8ZS code words are not counted. This counter is always enabled; it is not disabled during receive loss of synchronization (RLOS=1) conditions.

LCVCR1: LINE CODE VIOLATION COUNT REGISTER 1 (Address=23 Hex)
LCVCR2: LINE CODE VIOLATION COUNT REGISTER 2 (Address=24 Hex)

(MSB)							(LSB)	
LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8	LCVCR1
LCV7	LCV6	LCV5	LCV4	LCV3	LCV2	LCV1	LCV0	LCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
LCV15	LCVCR1.7	MSB of the 16-bit code violation count
LCV0	LCVCR2.0	LSB of the 16-bit code violation count

LINE CODE VIOLATION COUNTING ARRANGEMENTS Table 5-1

COUNT EXCESSIVE 0S? (RCR1.7)	B8ZS ENABLED? (CCR2.2)	WHAT IS COUNTED IN THE LCVCRs
no	no	BPVs
yes	no	BPVs + 16 consecutive 0s
no	yes	BPVs (B8ZS code words not counted)
yes	yes	BPVs + 8 consecutive 0s

5.2 Path Code Violation Count Register (PCVCR)

When the receive side of the DS2151Q is set to operate in the ESF framing mode (CCR2.3=1), PCVCR will automatically be set as a 12-bit counter that will record errors in the CRC6 code words. When set to operate in the D4 framing mode (CCR2.3=0), PCVCR will automatically count errors in the Ft framing bit position. Via the RCR2.1 bit, the DS2151Q can be programmed to also report errors in the Fs framing bit position. The PCVCR will be disabled during receive loss of synchronization (RLOS=1) conditions. See Table 5-2 for a detailed description of exactly what errors the PCVCR counts.

PCVCR1: PATH VIOLATION COUNT REGISTER 1 (Address=25 Hex)
PCVCR2: PATH VIOLATION COUNT REGISTER 2 (Address=26 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	CRC/FB11	CRC/FB10	CRC/FB9	CRC/FB8	PCVCR1
CRC/FB7	CRC/FB6	CRC/FB5	CRC/FB4	CRC/FB3	CRC/FB2	CRC/FB1	CRC/FB0	PCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC/FB11	PCVCR1.3	MSB of the 12-Bit CRC6 Error or Frame Bit Error Count (note 2)
CRC/FB0	PCVCR2.0	LSB of the 12-Bit CRC6 Error or Frame Bit Error Count (note 2)

NOTES:

1. The upper nibble of the counter at address 25 is used by the Multiframes Out of Sync Count Register.

2. PCVCR counts either errors in CRC code words (in the ESF framing mode; CCR2.3=1) or errors in the framing bit position (in the D4 framing mode; CCR2.3=0).

PATH CODE VIOLATION COUNTING ARRANGEMENTS Table 5-2

FRAMING MODE (CCR2.3)	COUNT FS ERRORS? (RCR2.1)	WHAT IS COUNTED IN THE PCVCRs
D4	no	errors in the Ft pattern
D4	yes	errors in both the Ft and Fs patterns
ESF	don't care	errors in the CRC6 code words

5.3 Multiframes Out of Sync Count Register (MOSCR)

Normally the MOSCR is used to count the number of multiframes that the receive synchronizer is out of sync (RCR2.0=1). This number is useful in ESF applications needing to measure the parameters Loss Of Frame Count (LOFC) and ESF Error Events as described in AT&T publication TR54016. When the MOSCR is operated in this mode, it is not disabled during receive loss of synchronization (RLOS=1) conditions. The MOSCR has alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the MOSCR is operated in this mode, it is disabled during receive loss of synchronization (RLOS=1) conditions. See Table 5-3 for a detailed description of what the MOSCR is capable of counting.

MOSCR1: MULTIFRAMES OUT OF SYNC COUNT REGISTER 1 (Address=25 Hex)

MOSCR2: MULTIFRAMES OUT OF SYNC COUNT REGISTER 2 (Address=27 Hex)

(MSB)							(LSB)	
MOS/FB11	MOS/FB10	MOS/FB9	MOS/FB8	(note 1)	(note 1)	(note 1)	(note 1)	MOSCR1
MOS/FB7	MOS/FB6	MOS/FB5	MOS/FB4	MOS/FB3	MOS/FB2	MOS/FB1	MOS/FB0	MOSCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
MOS/FB11	MOSCR1.7	MSB of the 12-Bit Multiframes Out of Sync or F-Bit Error Count (note 2)
MOS/FB0	MOSCR2.0	LSB of the 12-Bit Multiframes Out of Sync or F-Bit Error Count (note 2)

NOTES:

1. The lower nibble of the counter at address 25 is used by the Path Code Violation Count Register.

2. MOSCR counts either errors in framing bit position (RCR2.0=0) or the number of multiframes out of sync (RCR2.0=1).

MULTIFRAMES OUT OF SYNC COUNTING ARRANGEMENTS Table 5-3

FRAMING MODE (CCR2.3)	COUNT MOS OR F-BIT ERRORS? (RCR2.0)	WHAT IS COUNTED IN THE MOSCRs
D4	MOS	number of multiframes out of sync
D4	F-Bit	errors in the Ft pattern
ESF	MOS	number of multiframes out of sync
ESF	F-Bit	errors in the FPS pattern

6.0 FDL/FS EXTRACTION AND INSERTION

The DS2151Q has the ability to extract/insert data from/into the Facility Data Link (FDL) in the ESF framing mode and from/into Fs bit position in the D4 framing mode. Since SLC-96 utilizes the Fs bit position, this capability can also be used in SLC-96 applications. The operation of the receive and transmit sections will be discussed separately.

6.1 Receive Section

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the Receive FDL register (RFDL). Since the RFDL is 8 bits in length, it will fill up every 2 ms (8 times 250 us). The DS2151Q will signal an external microcontroller that the buffer has filled via the SR2.4 bit. If enabled via IMR2.4, the $\overline{INT2}$ pin will toggle low indicating that the buffer has filled and needs to be read. The user has 2 ms to read this data before it is lost. If the byte in the RFDL matches either of the bytes programmed into the RFDLM1 or RFDLM2 registers, then the SR2.2 bit will be set to a 1 and the $\overline{INT2}$ pin will be toggled low if enabled via IMR2.2. This feature allows an external microcontroller to ignore the FDL or Fs pattern until an important event occurs.

The DS2151Q also contains a 0 destuffer which is controlled via the CCR2.0 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.0, the DS2151Q will automatically look for five 1s in a row, followed by a 0. If it finds such a pattern, it will automatically remove the 0. If the 0 destuffer sees six or more 1s in a row followed by a 0, the 0 is not removed. The CCR2.0 bit should always be set to a 1 when the DS2151Q is extracting the FDL. More on how to use the DS2151Q in FDL and SLC-96 applications is covered in a separate Application Note. **Also, contact the factory for C code software that implements both ANSI T1.403 and AT&T TR54016.**

RFDL: RECEIVE FDL REGISTER (Address=28 Hex)

(MSB)							**(LSB)**
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RFDL7	RFDL.7	MSB of the Received FDL Code
RFDL0	RFDL.0	LSB of the Received FDL Code

The Receive FDL Register (RFDL) reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first.

RFDLM1: RECEIVE FDL MATCH REGISTER 1 (Address=29 Hex)
RFDLM2: RECEIVE FDL MATCH REGISTER 2 (Address=2A Hex)

(MSB)							**(LSB)**
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RFDL7	RFDL.7	MSB of the FDL Match Code
RFDL0	RFDL.0	LSB of the FDL Match Code

When the byte in the Receive FDL Register matches either of the two Receive FDL Match Registers (RFDLM1/RFDLM2), SR2.2 will be set to a 1 and the $\overline{INT2}$ will go active if enabled via IMR2.2.

6.2 Transmit Section

The transmit section will shift out into the T1 data stream, either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL register (TFDL). When a new value is written to the TFDL, it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full 8 bits have been shifted out, the DS2151Q will signal the host microcontroller that the buffer is empty and that more data is needed by setting the SR2.3 bit to a 1. The $\overline{INT2}$ will also toggle low if enabled via IMR2.3. The user has 2 ms to update the TFDL with a new value. If the TFDL is not updated, the old value in the TFDL will be transmitted once again.

The DS2151Q also contains a 0 stuffer which is controlled via the CCR2.4 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.4, the DS2151Q will automatically look for five 1s in a row. If it finds such a pattern, it will automatically insert a 0 after the five 1s. The CCR2.4 bit should always be set to a 1 when the DS2151Q is inserting the FDL. More on how to use the DS2151Q in FDL and SLC-96 applications is covered in a separate Application Note.

TFDL: TRANSMIT FDL REGISTER (Address=7E Hex)

(MSB)							(LSB)
TFDL7	TFDL6	TFDL5	TFDL4	TFDL3	TFDL2	TFDL1	TFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
TFDL7	TFDL.7	MSB of the FDL code to be transmitted
TFDL0	TFDL.0	LSB of the FDL code to be transmitted

The Transmit FDL Register (TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream in ESF mode. The LSB is transmitted first. In D4 operation the TFDL can be the source of the Fs pattern. In this case a 1ch is written to the TFDL register.

7.0 SIGNALING OPERATION

The Robbed-Bit signaling bits embedded in the T1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS2151Q. There is a set of 12 registers for the receive side (RS1 to RS12) and 12 registers on the transmit side (TS1 to TS12). The signaling registers are detailed below. The CCR1.5 bit is used to control the robbed signaling bits as they appear at RSER. If CCR1.5 is set to 0, then the robbed signaling bits will appear at RSER in their proper position as they are received. If CCR1.5 is set to a 1, then the robbed signaling bit positions will be forced to a 1 at RSER.

RS1 TO RS12: RECEIVE SIGNALING REGISTERS (Address=60 to 6B Hex)

(MSB)							**(LSB)**	
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	RS1 (60)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	RS2 (61)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	RS3 (62)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	RS4 (63)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	RS5 (64)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	RS6 (65)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	RS7 (66)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	RS8 (67)
A/C(24)	A/C(23)	A/C(22)	A/C(1)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	RS9 (68)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	RS10 (69)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	RS11 (6A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	RS12 (6B)

SYMBOL	**POSITION**	**NAME AND DESCRIPTION**
D(24)	RS12.7	Signaling Bit D in Channel 24
A(1)	RS1.0	Signaling Bit A in Channel 1

Each Receive Signaling Register (RS1 to RS12) reports the incoming Robbed-Bit signaling from eight DS0 channels. In the ESF framing mode, there can be up to 4 signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only 2 framing bits per channel (A and B). In the D4 framing mode, the DS2151Q will replace the C and D signaling bit positions with the A and B signaling bits from the previous multiframe. Hence, whether the DS2151Q is operated in either framing mode, the user needs only to retrieve the signaling bits every 3 ms. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The Receive Signaling Registers are frozen and not updated during a loss of sync condition (SR1.0=1). They will contain the most recent signaling information before the “OOF” occurred.

TS1 TO TS12: TRANSMIT SIGNALING REGISTERS (Address=70 to 7B Hex)

(MSB)							(LSB)	
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	TS1 (70)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	TS2 (71)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	TS3 (72)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	TS4 (73)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	TS5 (74)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	TS6 (75)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	TS7 (76)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	TS8 (77)
A/C(24)	A/C(23)	A/C(22)	A/C(1)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	TS9 (78)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	TS10 (79)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	TS11 (7A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	TS12 (7B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	TS12.7	Signaling Bit D in Channel 24
A(1)	TS1.0	Signaling Bit A in Channel 1

Each Transmit Signaling Register (TS1 to TS12) contains the Robbed-Bit signaling for eight DS0 channels that will be inserted into the outgoing stream if enabled to do so via TCR1.4. In the ESF framing mode, there can be up to 4 signaling bits per channel (A, B, C, and D). On multiframe boundaries, the DS2151Q will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe Interrupt in Status Register 2 (SR2.6) to know when to update the signaling bits. In the ESF framing mode, the interrupt will come every 3 ms and the user has a full 3 ms to update the TSRs. In the D4 framing mode, there are only 2 framing bits per channel (A and B). However in the D4 framing mode, the DS2151Q uses the C and D bit positions as the A and B bit positions for the next multiframe. The DS2151Q will load the values in the TSRs into the outgoing shift register every other D4 multiframe.

8.0 SPECIAL TRANSMIT SIDE REGISTERS

There is a set of seven registers in the DS2151Q that can be used to custom tailor the data that is to be transmitted onto the T1 line, on a channel by channel basis. Each of the 24 T1 channels can be either forced to be transparent or to have a user defined idle code inserted into them. Each of these special registers is defined below.

TTR1/TTR2/TTR3: TRANSMIT TRANSPARENCY REGISTERS (Address=39 to 3B Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1 (39)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2 (3A)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3 (3B)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TTR3.7	**Transmit Transparency Registers**. 0=this DS0 channel is not transparent
CH1	TTR1.0	1=this DS0 channel is transparent

Each of the bit positions in the Transmit Transparency Registers (TTR1/TTR2/TTR3) represents a DS0 channel in the outgoing frame. When these bits are set to a 1, the corresponding channel is transparent (or clear). If a DS0 is programmed to be clear, no Robbed-Bit signaling will be inserted nor will the channel have Bit 7 stuffing performed. However, in the D4 framing mode, Bit 2 will be overwritten by a 0 when a Yellow Alarm is transmitted. Also the user has the option to prevent the TTR registers from determining which channels are to have Bit 7 stuffing performed. If the TCR2.0 and TCR1.3 bits are set to 1, then all 24 T1 channels will have Bit 7 stuffing performed on them regardless of how the TTR registers are programmed. In this manner, the TTR registers are only affecting which channels are to have Robbed-Bit signaling inserted into them. Please see Figure 13-9 for more details.

TIR1/TIR2/TIR3: TRANSMIT IDLE REGISTERS (Address=3C to 3E Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (3C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (3D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (3E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TIR3.7	**Transmit Idle Registers.** 0=do not insert the Idle Code into this DS0 channel
CH1	TIR1.0	1=insert the Idle Code into this channel

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=3F Hex)

(MSB)							(LSB)
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code
TIDR0	TIDR.0	LSB of the Idle Code

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3) represents a DS0 channel in the outgoing frame. When these bits are set to a 1, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). Robbed-Bit signaling and Bit 7 stuffing will occur over the programmed Idle Code unless the DS0 channel is made transparent by the Transmit Transparency Registers.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3) control the RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHCLK pins are user-programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a UART or LAPD controller in Fractional T1 or ISDN-PRI applications. When the appropriate bits are set to a 1, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing in Section 13 for an example.

RCBR1/RCBR2/RCBR3: RECEIVE CHANNEL BLOCKING REGISTERS

(Address=6C to 6E Hex)

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (6C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (6D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (6E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RCBR3.7	**Receive Channel Blocking Registers** 0=force the RCHBLK pin to remain low during this channel time
CH1	RCBR1.0	1=force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3: TRANSMIT CHANNEL BLOCKING REGISTERS

(Address=32 to 34 Hex)

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (32)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (33)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (34)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TCBR3.7	**Transmit Channel Blocking Registers**. 0=force the TCHBLK pin to remain low during this channel time
CH1	TCBR1.0	1=force the TCHBLK pin high during this channel time

10.0 ELASTIC STORES OPERATION

The DS2151Q has two onboard two-frame (386 bits) elastic stores. These elastic stores have two main purposes. First, they can be used to rate-convert the T1 data stream to 2.048 Mbps (or a multiple of 2.048 Mbps), which is the E1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the T1 data stream and an asynchronous (i.e., not frequency locked) backplane clock. Both elastic stores contain full controlled slip capability which is necessary for this second purpose. The receive side elastic store can be enabled via CCR1.2 and the transmit side elastic store is enabled via CCR1.7. The elastic stores can be forced to a known depth via the Elastic Store Reset bit (CCR3.6).

10.1 Receive Side

If the receive side elastic store is enabled (CCR1.2=1), then the user must provide either a 1.544 MHz (CCR1.3=0) or 2.048 MHz (CCR1.3=1) clock at the SYSCLK pin. The user has the option of either providing a frame sync at the RSYNC pin (RCR2.3=1) or having the RSYNC pin provide a pulse on frame boundaries (RCR2.3=0). If the user wishes to obtain pulses at the frame boundary, then RCR2.4 must be set to 0 and if the user wishes to have pulses occur at the multiframe boundary, then RCR2.4 must be set to 1. If the user selects to apply a 2.048 MHz clock to the SYSCLK pin, then the data output at RSER will be forced to all 1s every fourth channel and the F-bit will be deleted. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be forced to a 1.

Also, in 2.048 MHz applications, the RCHBLK output will be forced high during the same channels as the RSER pin. See Section 13 for more details. This is useful in T1 to CEPT (E1) conversion applications. If the 386-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (193 bits) will be repeated at RSER and the SR1.4 and RIR1.3 bits will be set to a 1. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR1.4 bits will be set to a 1.

10.2 Transmit Side

The transmit side elastic store can only be used if the receive side elastic store is enabled. The operation of the transmit elastic store is very similar to the receive side; both have controlled slip operation and both can operate with either a 1.544 MHz or a 2.048 MHz SYSCLK. When the transmit elastic store is enabled, both the SYSCLK and RSYNC signals are shared by both the elastic stores. Hence, they will have the same backplane PCM frame and data structure. Controlled slips in the transmit elastic store are reported in the RIR2.5 bit and the direction of the slip is reported in the RIR2.3 and RIR2.4 bits.

10.3 Minimum Delay Synchronous SYSCLKMode

In applications where the DS2151Q is connected to backplanes that are frequency-locked to the recovered T1 clock (i.e., the RCLK output), the full two-frame depth of the onboard elastic stores is really not needed. In fact, in some delay-sensitive applications the normal two-frame depth may be excessive. If the CCR3.7 bit is set to 1, then the receive elastic store (and also the transmit elastic store if it is enabled) will be forced to a maximum depth of 32 bits instead of the normal 386 bits. In this mode, the SYSCLK must be frequency-locked to RCLK and all of the slip contention logic in the DS2151Q is disabled (since slips cannot occur). Also, since the buffer depth is no longer two frames deep, the DS2151Q must be set up to source either a frame or multiframe pulse at the RSYNC pin. On power-up after the SYSCLK has locked to the RCLK signal, the Elastic Store Reset bit (CCR3.6) should be toggled from a 0 to a 1 to insure proper operation.

11.0 RECEIVE MARK REGISTERS

The DS2151Q has the ability to replace the incoming data on a channel-by-channel basis with either an idle code (7F Hex) or the digital milliwatt code, which is an 8-byte repeating pattern that represents a 1 kHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). The RCR2.7 bit will determine which code is used. Each bit in the RMRs, represents a particular channel. If a bit is set to a 1, then the receive data in that channel will be replaced with one of the two codes. If a bit is set to 0, no replacement occurs.

RMR1/RMR2/RMR3: RECEIVE MARK REGISTERS (Address=2D to 2F Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1 (2D)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2 (2E)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3 (2F)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RMR3.7	**Receive Channel Blocking Registers**. 0=do not affect the receive data associated with this channel
CH1	RMR1.0	1=replace the receive data associated with this channel with either the idle code or the digital milliwatt code (depends on the RCR2.7 bit)

12.0 LINE INTERFACE FUNCTIONS

The line interface function in the DS2151Q contains three sections; (1) the receiver which handles clock and data recovery, (2) the transmitter which waveshapes and drives the T1 line, and (3) the jitter attenuator. Each of these three sections is controlled by the Line Interface Control Register (LICR), which is described below.

LICR: LINE INTERFACE CONTROL REGISTER (Address=7C Hex)

(MSB)							(LSB)	
L2	L1	L0	EGL	JAS	JABDS	DJA	TPD	LICR

SYMBOL	POSITION	NAME AND DESCRIPTION
L2	LICR.7	**Line Build Out Select Bit 2.** Sets the transmitter build out; see the Table 12-2
L1	LICR.6	**Line Build Out Select Bit 1**. Sets the transmitter build out; see the Table 12-2
L0	LICR.5	**Line Build Out Select Bit 0**. Sets the transmitter build out; see the Table 12-2
EGL	LICR.4	**Receive Equalizer Gain Limit**. 0= -36 dB 1= -30 dB
JAS	LICR.3	**Jitter Attenuator Select**. 0=place the jitter attenuator on the receive side 1=place the jitter attenuator on the transmit side
JABDS	LICR.2	**Jitter Attenuator Buffer Depth Select.** 0=128 bits 1=32 bits (use for delay sensitive applications)
DJA	LICR.1	**Disable Jitter Attenuator**. 0=jitter attenuator enabled

1=jitter attenuator disabled

TPD LICR.0 **Transmit Power Down**.
0=normal transmitter operation
1=powers down the transmitter and 3-states the TTIP and TRING pins

12.1 Receive Clock and Data Recovery

The DS2151Q contains a digital clock recovery system. See the DS2151Q Block Diagram in Section 1 and Figure 12-1 for more details. The DS2151Q couples to the receive T1 twisted pair via a 1:1 transformer. See Table 12-3 for transformer details. The DS2151Q automatically adjusts to the T1 signal being received at the RTIP and RRING pins and can handle T1 lines from 0 feet to over 6000 feet in length. The crystal attached at the XTAL1 and XTAL2 pins is multiplied by 4 via an internal PLL and fed to the clock recovery system. The clock recovery system uses both edges of the clock from the PLL circuit to form a 32 times oversampler which is used to recover the clock and data. This oversampling technique offers outstanding jitter tolerance (see Figure 12-2). The EGL bit in the Line Interface Control Register is used to limit the sensitivity of the receiver in the DS2151Q. For most CPE applications, a receiver sensitivity of -30 dB is wholly sufficient and hence the EGL bit should be set to 1. In some applications, more sensitivity than -30 dB may be required and the DS2151Q will allow the receiver to go as low as -36 dB if the EGL bit is set to 0. However, when the EGL bit is set to 0, the DS2151Q will be more susceptible to crosstalk and its jitter tolerance will suffer.

Normally, the clock that is output at the RCLK pin is the recovered clock from the T1 AMI waveform presented at the RTIP and RRING inputs. When no AMI signal is present at RTIP and RRING, a Receive Carrier Loss (RCL) condition will occur and the RCLK can be sourced from either the ACLKI pin or from the crystal attached to the XTAL1 and XTAL2 pins. The DS2151Q will sense the ACLKI pin to determine if a clock is present. If no clock is applied to the ACLKI pin, then it should be tied to RVSS to prevent the device from falsely sensing a clock. See Table 12-1. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit short high cycles of the clock. This is due to the highly oversampled digital clock recovery circuitry. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to being close to 50% duty cycle. Please see the Receive AC Timing Characteristics in Section 14 for more details.

SOURCE OF RCLK UPON RCL Table 12-1

ACLKI PRESENT?	RECEIVE SIDE JITTER ATTENUATOR	TRANSMIT SIDE JITTER ATTENUATOR
Yes	ACLKI via the jitter attenuator	ACLKI
No	centered crystal	TCLK via the jitter attenuator

12.2 Transmit Waveshaping and Line Driving

The DS2151Q uses a set of laser-trimmed delay lines along with a precision Digital-to-Analog Converter (DAC) to create the waveforms that are transmitted onto the T1 line. The waveforms created by the DS2151Q meet the latest ANSI, AT&T, and CCITT specifications. See Figure 12-3. The user will select which waveform is to be generated by properly programming the L0 to L2 bits in the Line Interface Control Register (LICR).

LBO SELECT IN LICR Table 12-2

L2	L1	L0	LINE BUILD OUT	APPLICATION
0	0	0	0 to 133 feet/0 dB	DSX-1/CSU
0	0	1	133 to 266 feet	DSX-1
0	1	0	266 to 399 feet	DSX-1
0	1	1	399 to 533 feet	DSX-1
1	0	0	533 to 655 feet	DSX-1
1	0	1	-7.5 dB	CSU
1	1	0	-15 dB	CSU
1	1	1	-22.5 dB	CSU

Due to the nature of the design of the transmitter in the DS2151Q, very little jitter (less then 0.005 UIpp broad-band from 10 Hz to 100 kHz) is added to the jitter present on TCLK. Also, the waveforms that they create are independent of the duty cycle of TCLK. The transmitter in the DS2151Q couples to the T1 transmit twisted pair via a 1:1.15 or 1:1.36 step up transformer as shown in Figure 12-1. In order for the devices to create the proper waveforms, the transformer used must meet the specifications listed in Table 12-3.

TRANSFORMER SPECIFICATIONS Table 12-3

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio	1:1 (receive) and 1:1.15 or 1:1.36 (transmit) ±5%
Primary Inductance	600 µH minimum
Leakage Inductance	1.0 µH maximum
Intertwining Capacitance	40 pF maximum
DC Resistance	1.2 ohms maximum

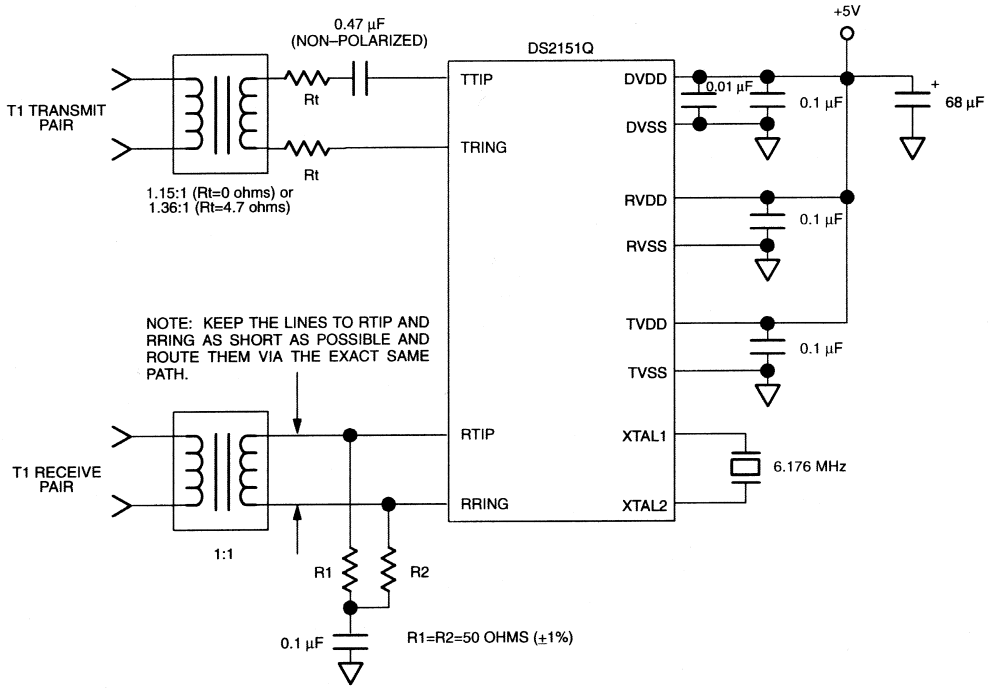
12.3 JITTER ATTENUATOR

The DS2151Q contains an onboard jitter attenuator that can be set to a depth of either 32 or 128 bits via the JABDS bit in the Line Interface Control Register (LICR). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in Figure 12-4. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit in the LICR. Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA-bit in the LICR. In order for the jitter attenuator to operate properly, a crystal with the specifications listed in Table 12-4 below must be connected to the XTAL1 and XTAL2 pins. The jitter attenuator divides the clock provided by the 6.176 MHz crystal at the XTAL1 and XTAL2 pins to create an output clock that contains very little jitter. Onboard circuitry will pull the crystal (by switching in or out load capacitance) to keep it long-term averaged to the same frequency as the incoming T1 signal. If the incoming jitter exceeds either 120UIpp (buffer depth is 128 bits) or 28 UIpp (buffer depth is 32 bits), then the DS2151Q will divide the attached crystal by either 3.5 or 4.5 instead of the normal 4 to keep the buffer from overflowing. When the device divides by either 3.5 or 4.5, it also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register 2 (RIR2.2).

CRYSTAL SELECTION GUIDELINES Table 12-4

PARAMETER	SPECIFICATION
Parallel Resonant Frequency	6.176 MHz
Mode	Fundamental
Load Capacitance	18 pF to 20 pF (18.5 pF nominal)
Tolerance	±50 ppm
Pullability	CL=10 pF, delta frequency=+175 to +250 ppm CL=45 pF, delta frequency=-175 to -250 ppm
Effective Series Resistance	40 ohms maximum
Crystal Cut	AT

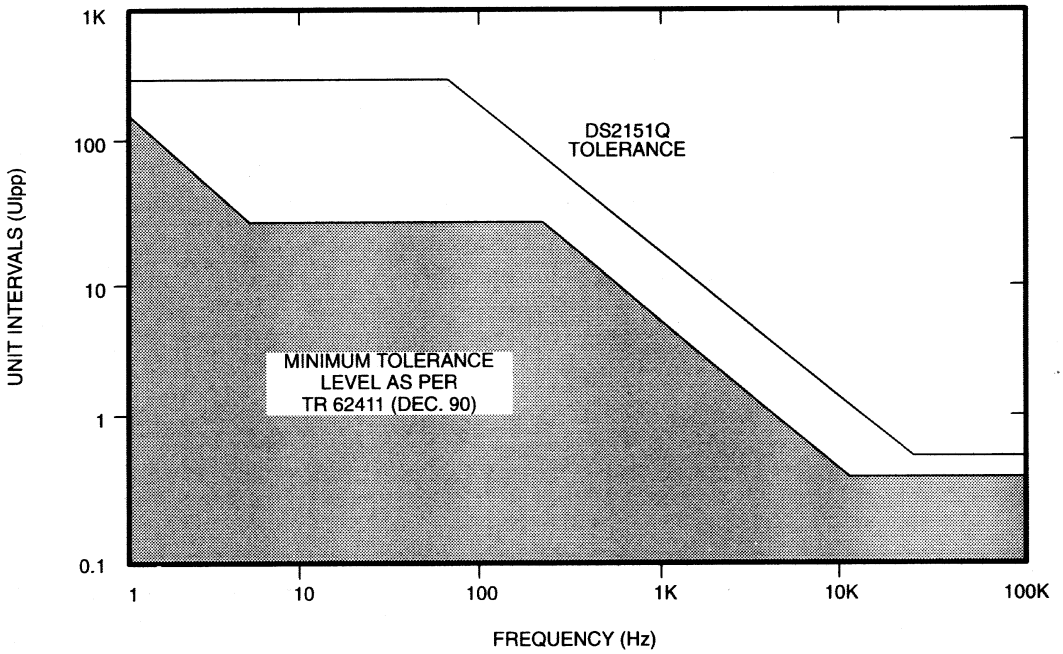
DS2151Q EXTERNAL ANALOG CONNECTIONS Figure 12-1



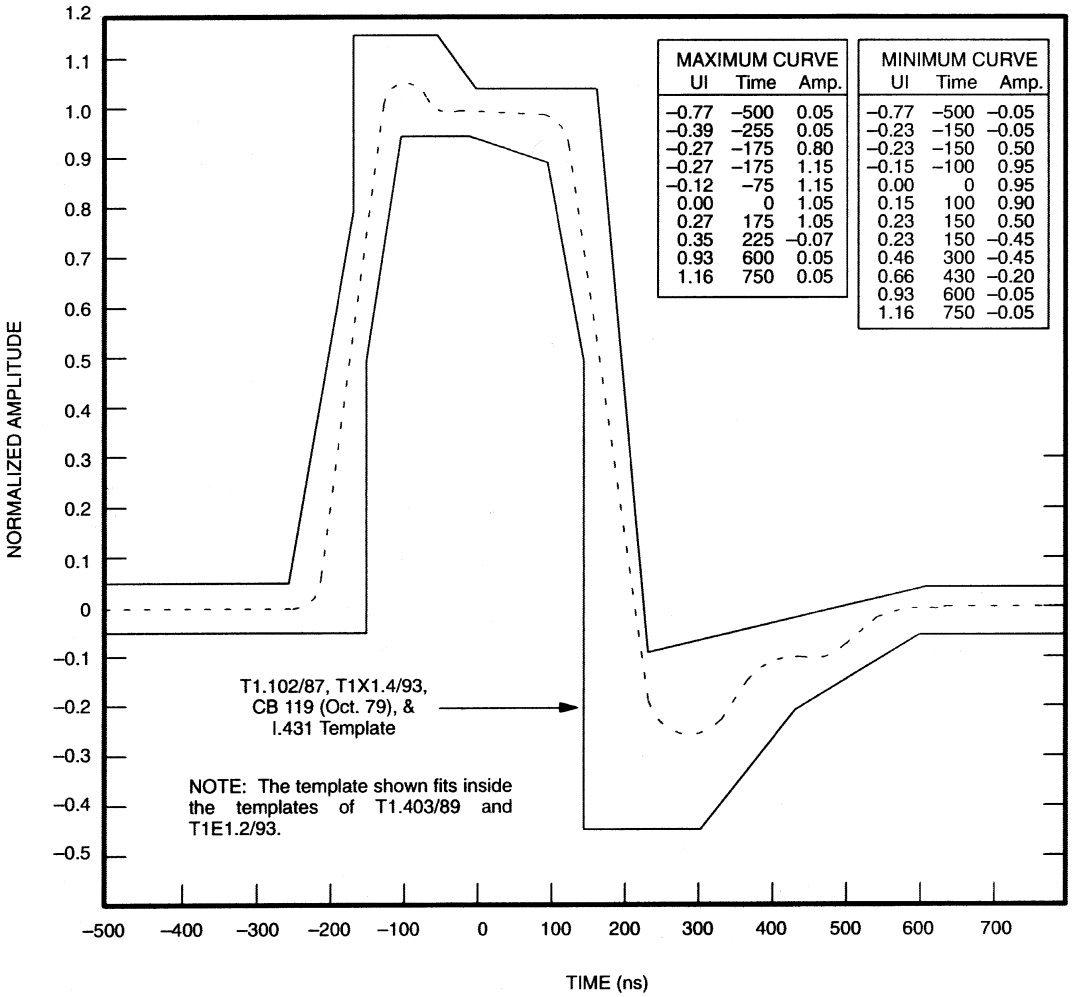
NOTE:

See the separate Application Note for details on how to construct a protected interface.

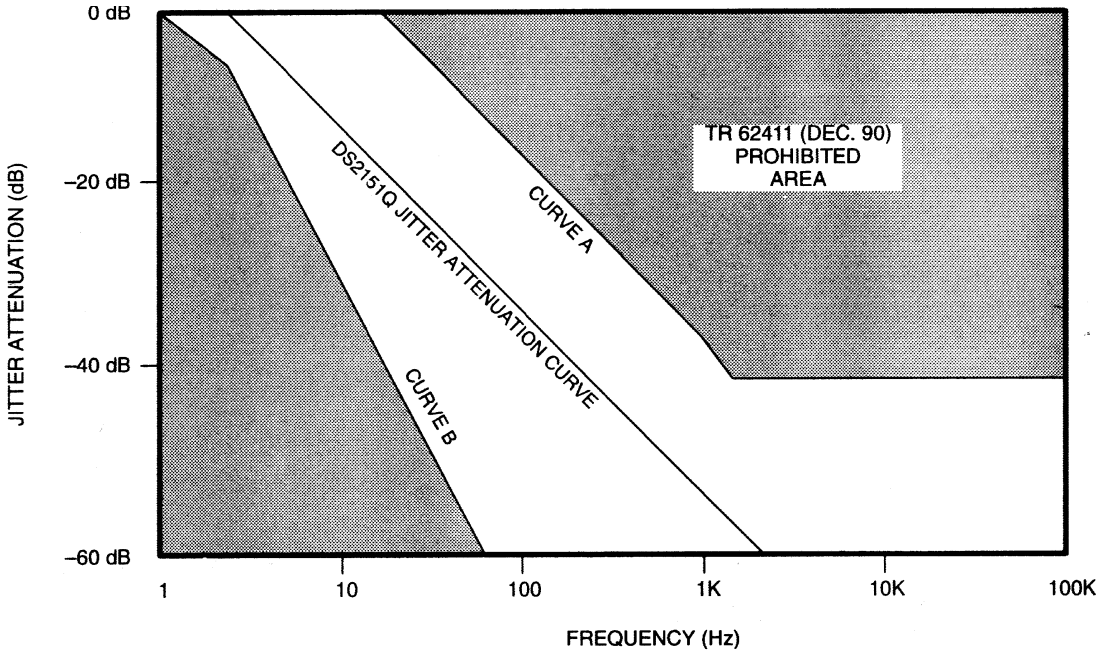
DS2151Q JITTER TOLERANCE Figure 12-2



DS2151Q TRANSMIT WAVEFORM TEMPLATE Figure 12-3

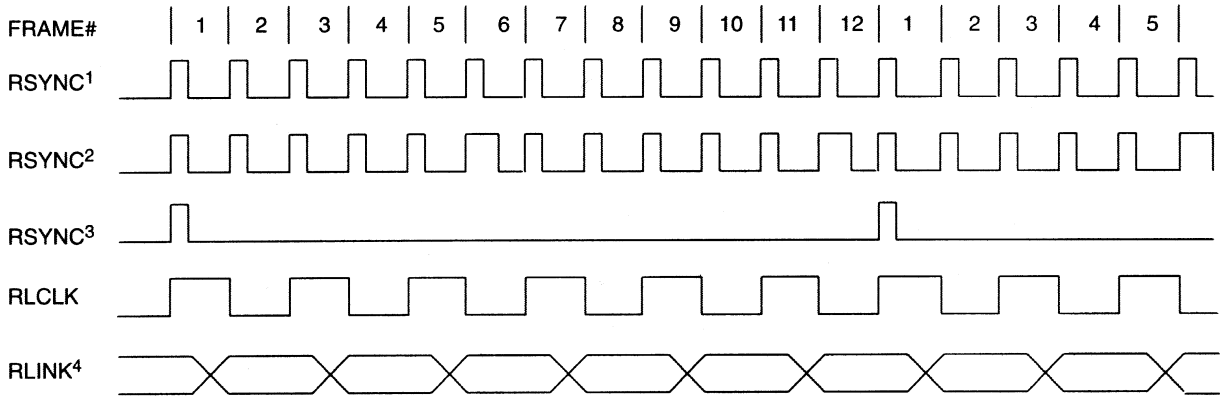


DS2151Q JITTER ATTENUATION Figure 12-4



13.0 TIMING DIAGRAMS

RECEIVE SIDE D4 TIMING Figure 13-1



NOTES:

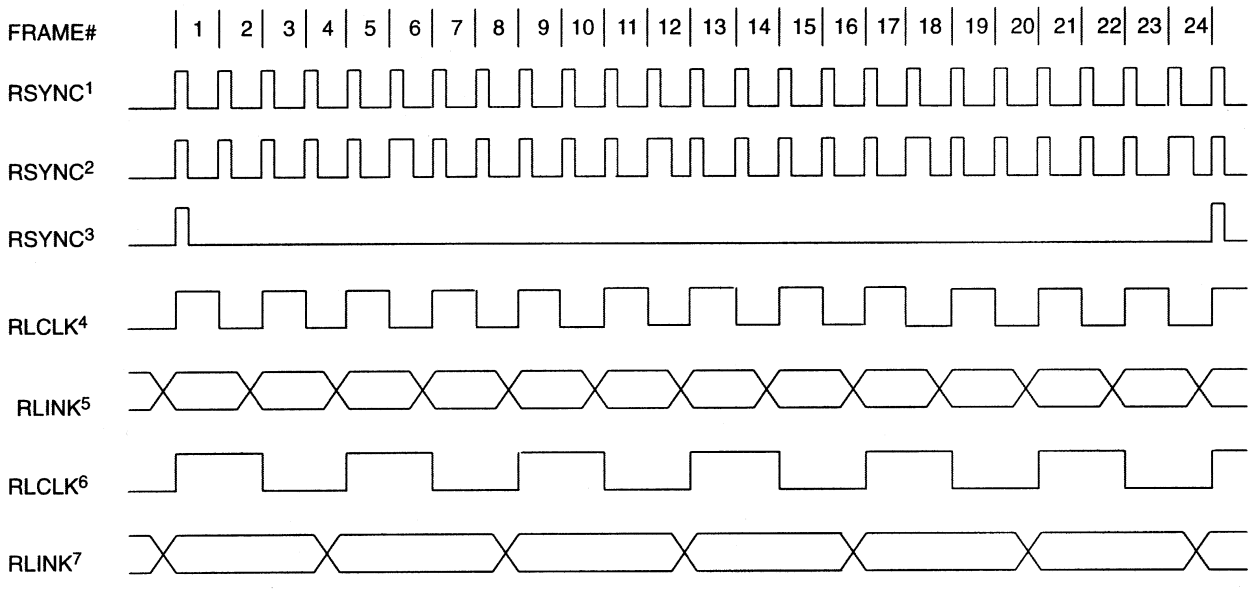
1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).

2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).

3. RSYNC in the multiframe mode (RCR2.4=1).

4. RLINK data (S-bit) is updated 1 bit prior to even frames and held for two frames.

RECEIVE SIDE ESF TIMING Figure 13-2

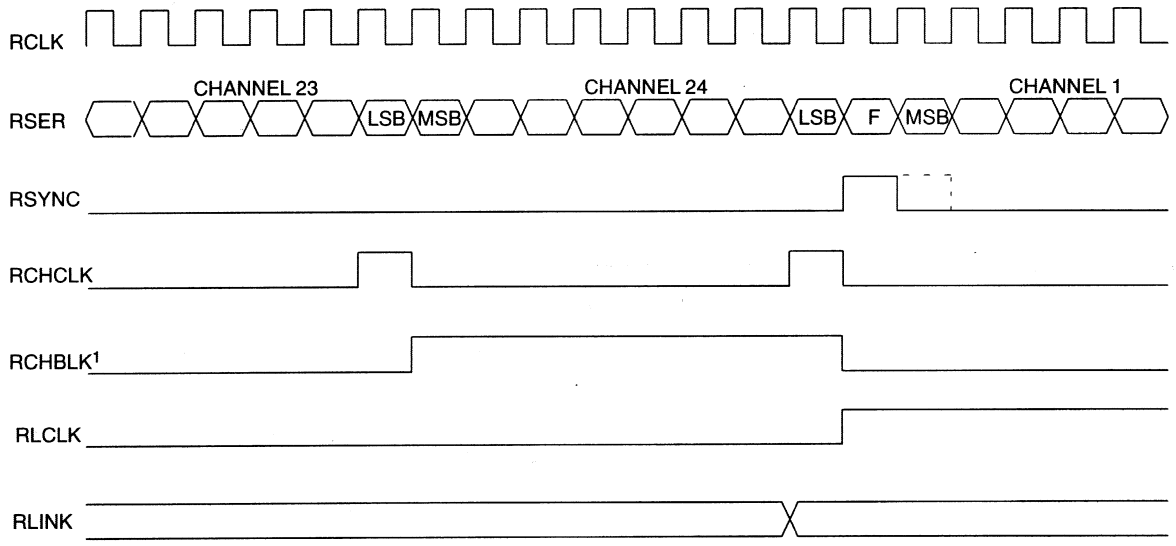


NOTES:

1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).
2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).
3. RSYNC in the multiframe mode (RCR2.4=1).
4. ZBTSI mode disabled (RCR2.6=0).
5. RLINK data (FDL bits) is updated 1 bit-time before odd frames and held for two frames.
6. ZBTSI mode is enabled (RCR2.6=1).
7. RLINK data (Z bits) is updated 1 bit-time before odd frame and held for four frames.

RECEIVE SIDE BOUNDARY TIMING WITH ELASTIC STORE(S) DISABLED

Figure 13-3



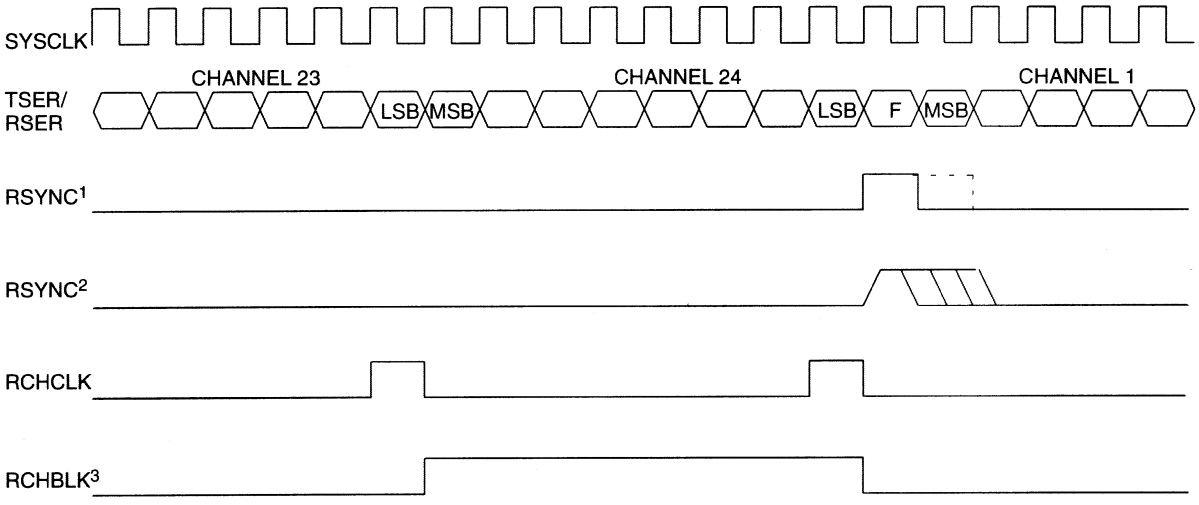
NOTES:

1. RCHBLK is programmed to block channel 24.

2. An ESF boundary is shown.

1.544 MHz BOUNDARY TIMING WITH ELASTIC STORE(S) ENABLED

Figure 13-4



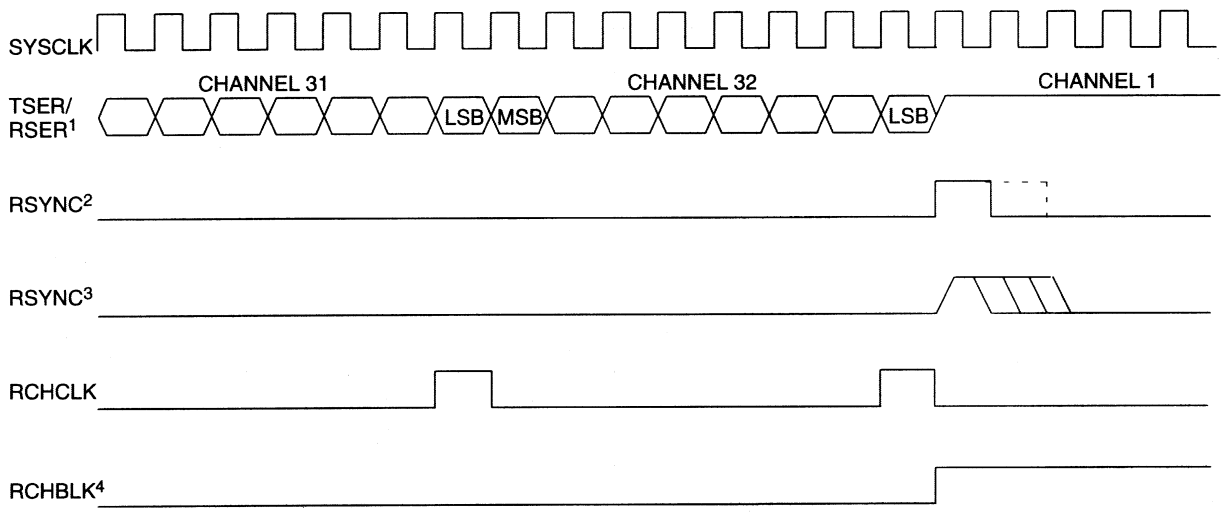
NOTES:

1. RSYNC is in the output mode (RCR2.3=0).

2. RSYNC is in the input mode (RCR2.3=1).

3. RCHBLK is programmed to block channel 24.

2.048 MHz BOUNDARY TIMING WITH ELASTIC STORE(S) ENABLED Figure 13-5



NOTES:

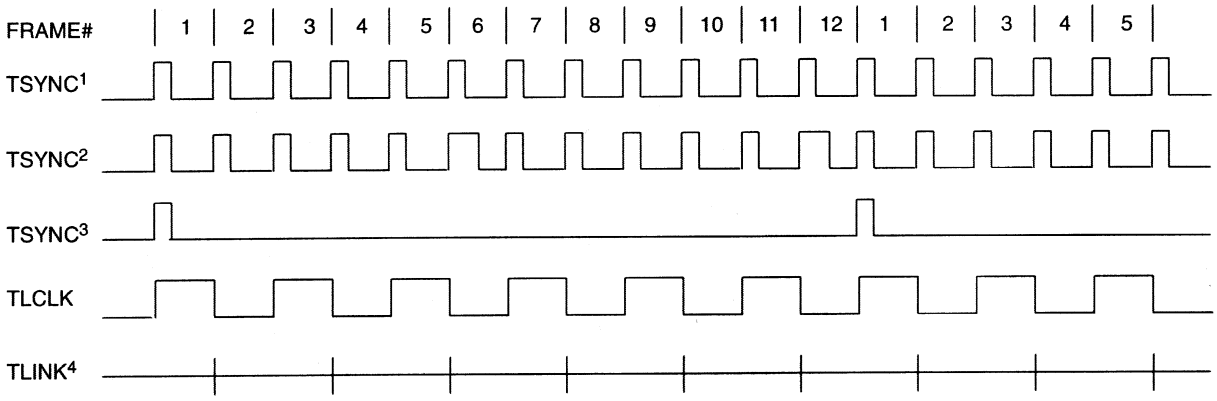
1. RSER data in channels 1, 5, 9, 13, 17, 21, 25, and 29 are forced to 1; TSER ignored during these channels.

2. RSYNC is in the output mode (RCR2.3=0).

3. RSYNC is in the input mode (RCR2.3=1).

4. RCHBLK is forced to 1 in the same channels as RSER (see Note 1).

TRANSMIT SIDE D4 TIMING Figure 13-6



NOTES:

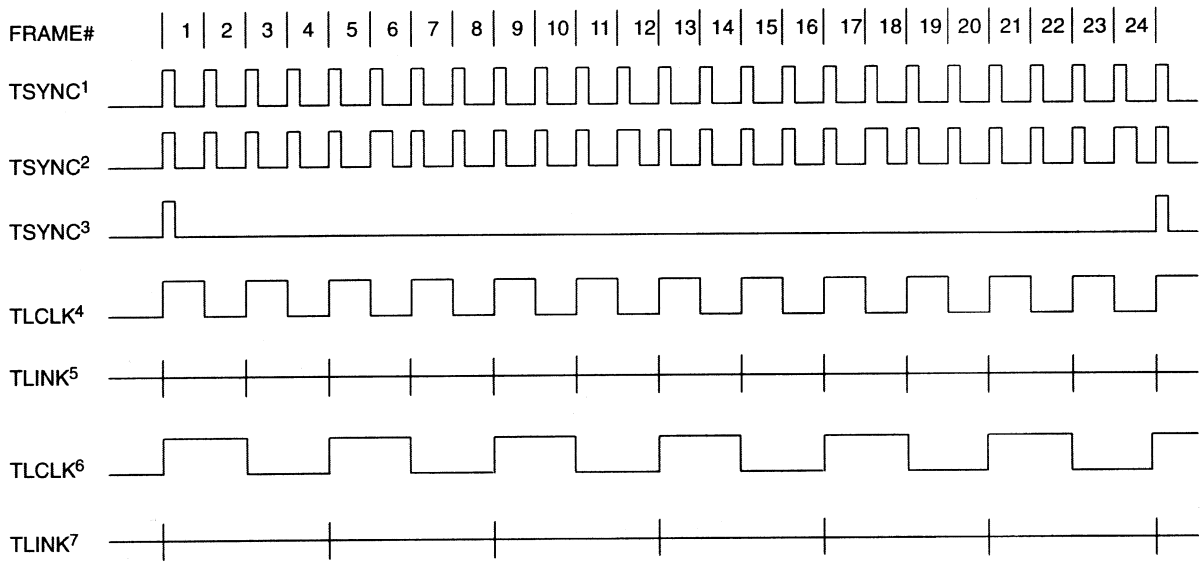
1. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is not enabled (TCR2.4=0).

2. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is enabled (TCR2.4=1).

3. TSYNC in the multiframe mode (TCR2.3=1).

4. TLINK data (S-bit) is sampled during the F-bit position of even frames for insertion into the outgoing T1 stream when enabled via TCR1.2.

TRANSMIT SIDE ESF TIMING Figure 13-7

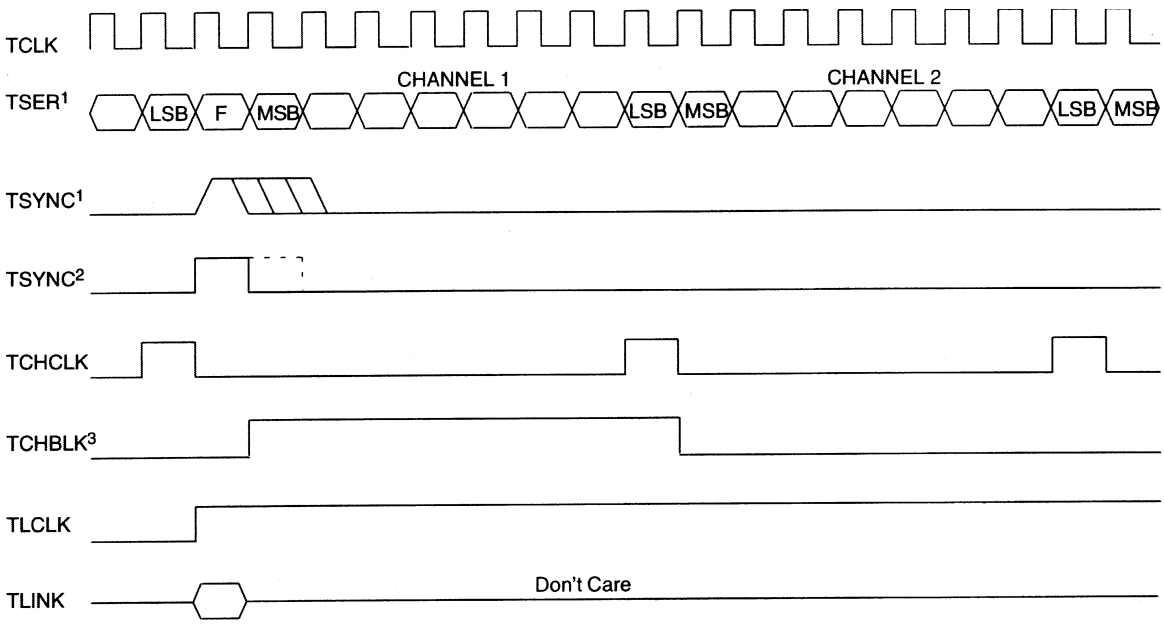


NOTES:

1. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is not enabled (TCR2.4=0).
2. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is enabled (TCR2.4=1).
3. TSYNC in the multiframe mode (TCR2.4=1).
4. ZBTSI mode disabled (TCR2.5=0).
5. TLINK data (FDL bits) is sampled during the F-bit time of odd frame and inserted into the outgoing T1 stream if enabled via TCR1.2.
6. ZBTSI mode is enabled (TCR2.5=1).
7. TLINK data (Z bits) is sampled during the F-bit time of frame 1, 5, 9, 13, 17, and 21 and inserted into the outgoing stream if enabled via TCR1.2.

TRANSMIT SIDE BOUNDARY TIMING (WITH ELASTIC STORE(S) DISABLED)

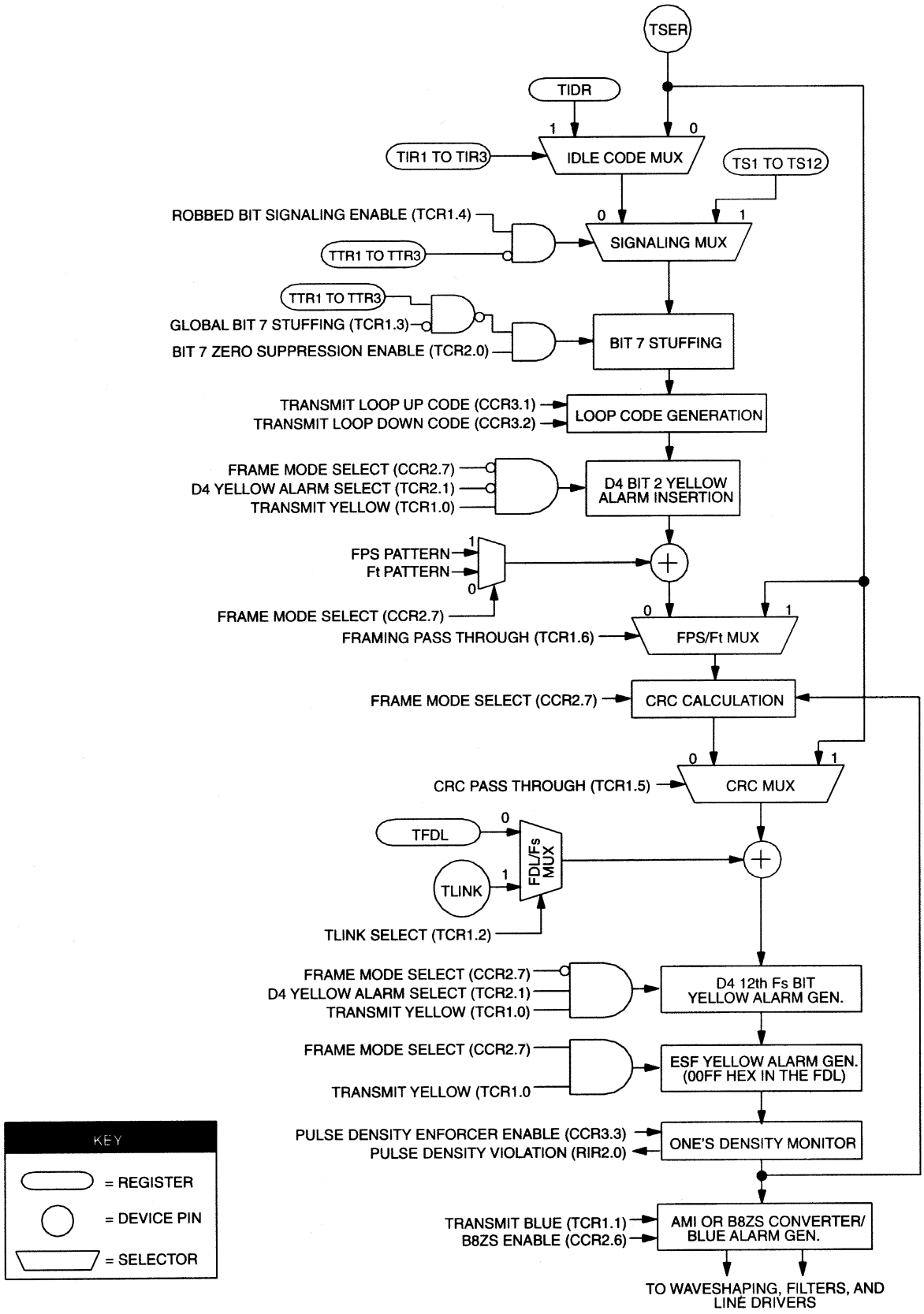
Figure 13-8



NOTES:

1. TSYNC is in the input mode (TCR2.2=0).
2. TSYNC is in the output mode (TCR2.2=1).
3. TCHBLK is programmed to block channel 1.
4. See Figures 13-4 and 13-5 for details on timing with the transmit side elastic store enabled.

DS2151Q TRANSMIT DATA FLOW Figure 13-9



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C (-40°C to +85°C for DS2151QN)
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)
(-40°C to +85°C for DS2151QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD} +0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.75		5.25	V	1

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

(0°C to 70°C; V_{DD} =5V ± 5%)
(-40°C to +85°C for DS2151QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}		65		mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Leakage	I_{LO}			1.0	µA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. Applies to RVDD, TVDD, and DVDD.

2. TCLK=1.544 MHz.

3. $0.0V < V_{IN} < V_{DD}$.

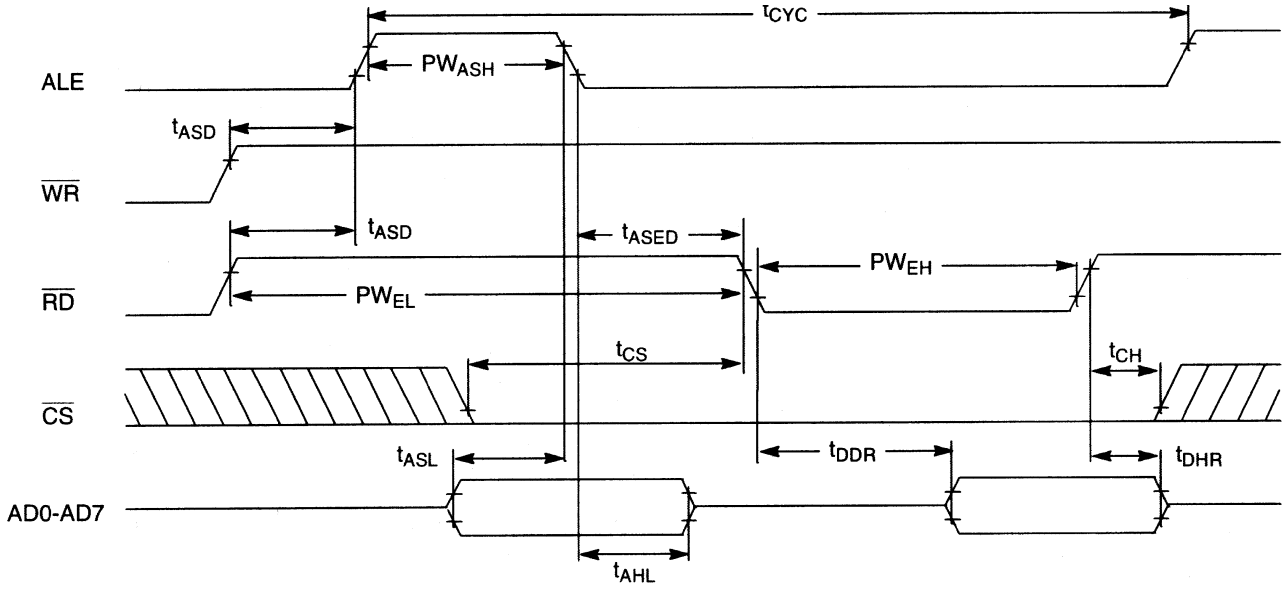
4. Applies to $\overline{INT1}$ and $\overline{INT1}$ when 3-stated.

AC CHARACTERISTICS PARALLEL PORT

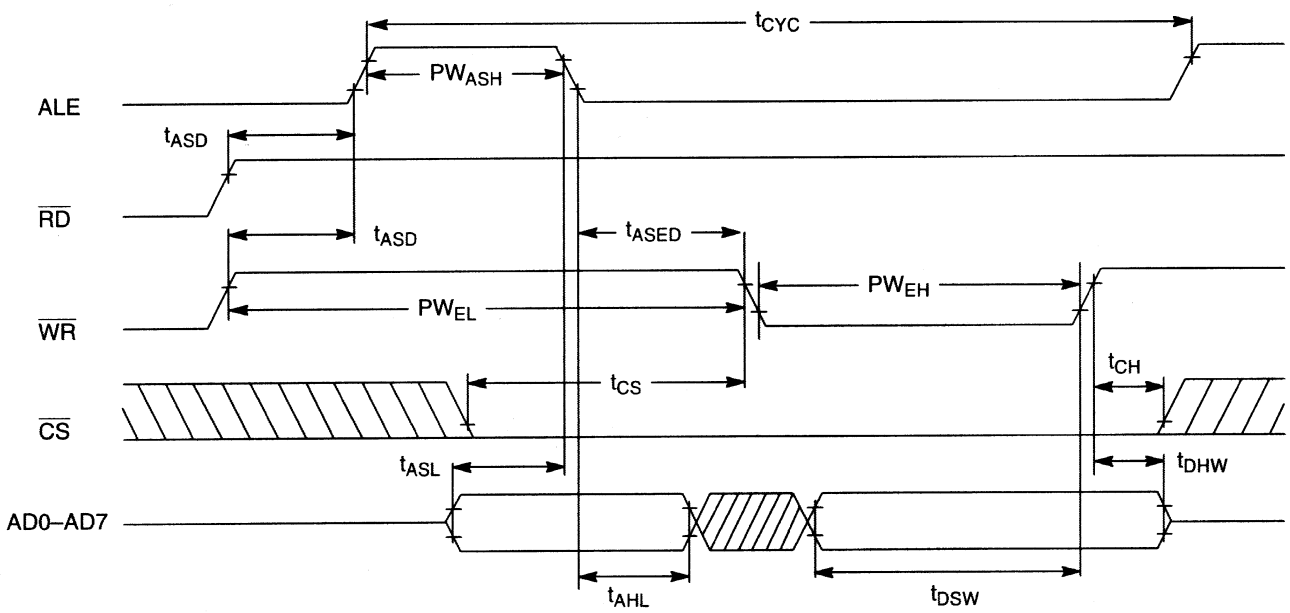
(0°C to 70°C; V_{DD} = 5V ± 5%)
(-40°C to +85°C for DS2151QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	250			ns	
Pulse Width, DS Low or $\overline{RD}$ High	PW_{EL}	150			ns	
Pulse Width, DS High or $\overline{RD}$ Low	PW_{EH}	100			ns	
Input Rise/Fall Times	t_R , t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time before DS High	t_{RWS}	50			ns	
$\overline{CS}$ Setup Time before DS, $\overline{WR}$ or $\overline{RD}$ active	t_{CS}	20			ns	
$\overline{CS}$ Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid to AS or ALE fall	t_{ASL}	20			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS, $\overline{WR}$ or $\overline{RD}$ to AS or ALE Rise	t_{ASD}	25			ns	
Pulse Width AS or ALE High	PW_{ASH}	40			ns	
Delay Time, AS or ALE to DS, $\overline{WR}$ or $\overline{RD}$	t_{ASED}	20			ns	
Output Data Delay Time from DS or $\overline{RD}$	t_{DDR}	20		100	ns	
Data Setup Time	t_{DSW}	80			ns	

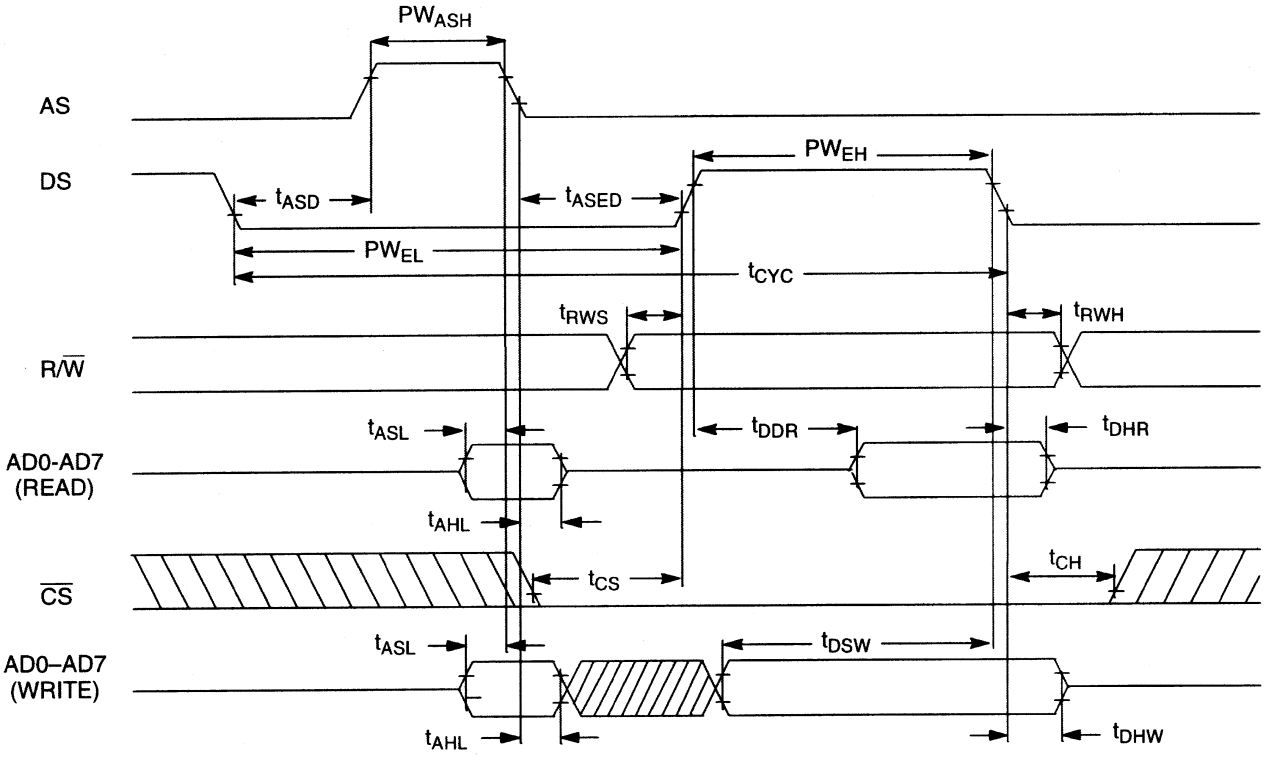
INTEL BUS READ AC TIMING



INTEL BUS WRITE AC TIMING



MOTOROLA BUS AC TIMING



AC CHARACTERISTICS PARALLEL PORT

(0°C to 70°C; V_{DD} = 5V ± 5%)
(-40°C to +85°C for DS2151QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
ACLKI/RCLK Period	t_{CP}		648		ns	
RCLK Pulse Width	t_{CH} t_{CL}	230 230	324 324		ns ns	1
RCLK Pulse Width	t_{CH} t_{CL}	115 115			ns ns	2
SYSCLK Period	t_{SP} t_{SP}		648 488		ns ns	3 4
SYSCLK Pulse Width	t_{SH} t_{SL}	75 75			ns	
RSYNC Set Up to SYSCLK Falling	t_{SU}	25		t_{SH} -5	ns	
RSYNC Pulse Width	t_{PW}	50			ns	
SYSCLK Rise/Fall Times	t_R t_F			25	ns	
Delay RCLK or SYSCLK to RSER Valid	t_{DD}	10		80	ns	
Delay RCLK or SYSCLK to RCHCLK	t_{D1}	10		90	ns	
Delay RCLK or SYSCLK to RCHBLK	t_{D2}	10		90	ns	
Delay RCLK or SYSCLK to RSYNC	t_{D3}	10		80	ns	
Delay RCLK to RLCLK	t_{D4}	10		80	ns	
Delay RCLK to RLINK Valid	t_{D5}	10		110	ns	

NOTES:

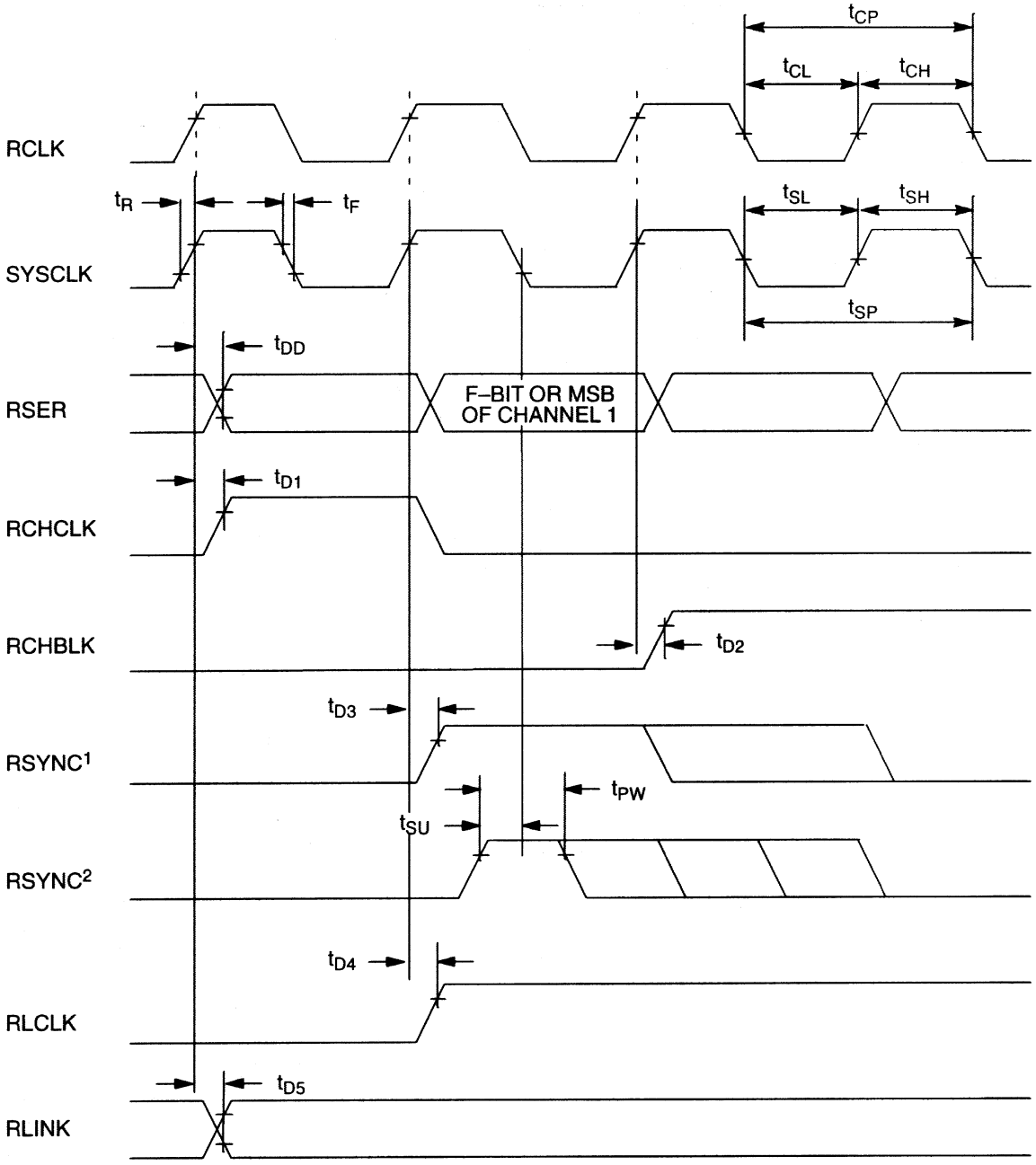
1. Jitter attenuator enabled in the receive side path.

2. Jitter attenuator disabled or enabled in the transmit path.

3. SYSCLK=1.544 MHz

4. SYSCLK=2.048 MHz

RECEIVE SIDE AC TIMING



NOTES:

1. RSYNC is in the output mode (RCR2.3=0).
2. RSYNC is in the input mode (RCR2.3=1).
3. RLCLK and RLINK only have a timing relationship to RCLK.
4. RCLK can exhibit a short high time if the jitter attenuator is either disabled or in the transmit path.

AC CHARACTERISTICS - TRANSMIT SIDE

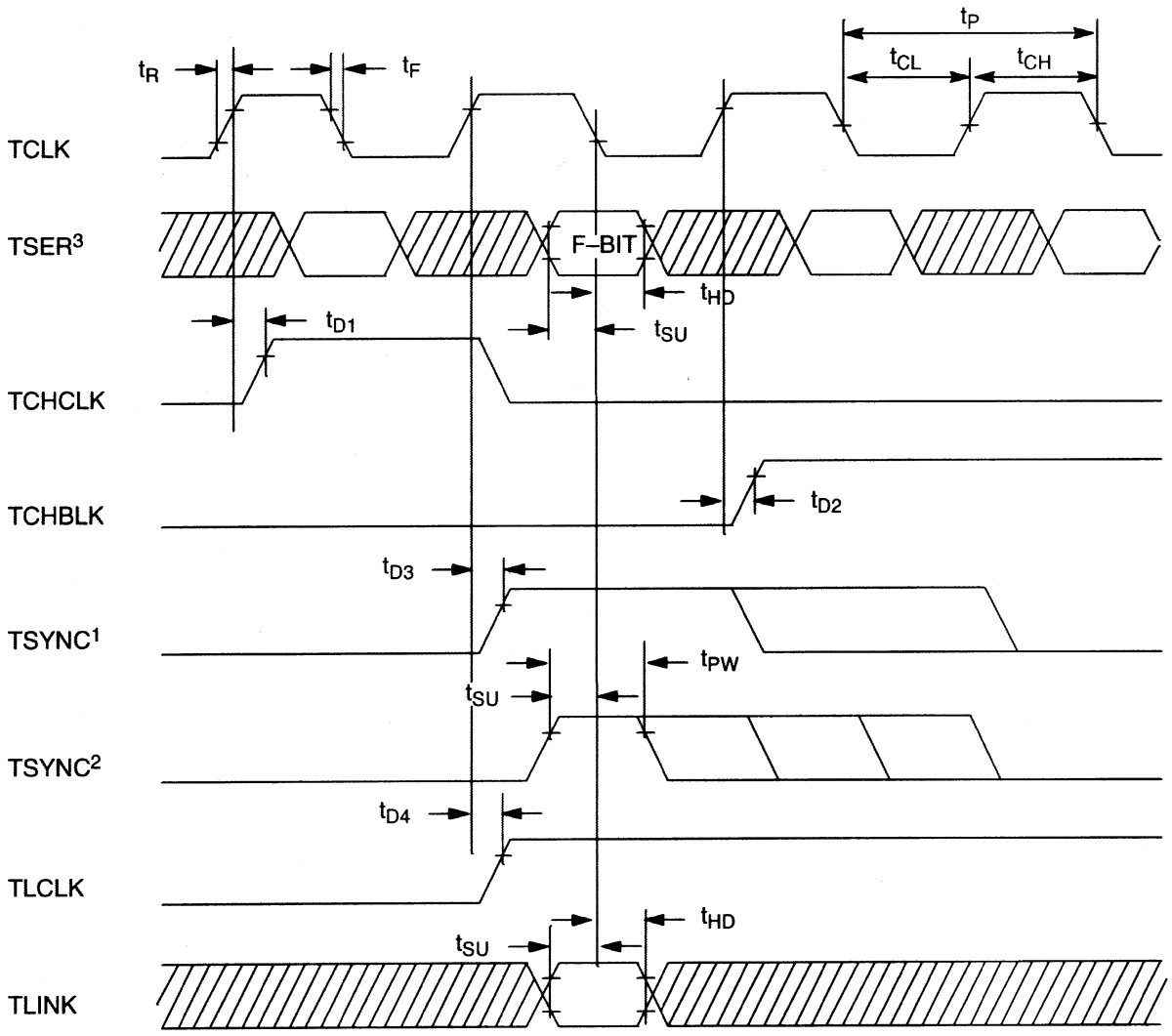
(0°C to 70°C; V_{DD} = 5V ± 5%)
(-40°C to +85°C for DS2151QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_P		648		ns	
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
TSER and TLINK Set up to TCLK Falling	t_{SU}	25			ns	1
TSER and TLINK Hold from TCLK Falling	t_{HD}	25			ns	1
TSYNC Set up to TCLK Falling	t_{SU}	25		t_{CH} -5		
TSYNC Pulse Width	t_{PW}	50				
TCLK Rise/Fall Times	t_R t_F			25	ns	
Delay TCLK to TCHCLK	t_{D1}	10		60	ns	
Delay TCLK to TCHBLK	t_{D2}	10		70	ns	
Delay TCLK to TSYNC	t_{D3}	10		60	ns	
Delay TCLK to TLCLK	t_{D4}	10		60	ns	

NOTE:

If the transmit side elastic store is enabled, then TSER is sampled on the falling edge of SYSCLK and the parameters t_{SU} and t_{HD} still apply.

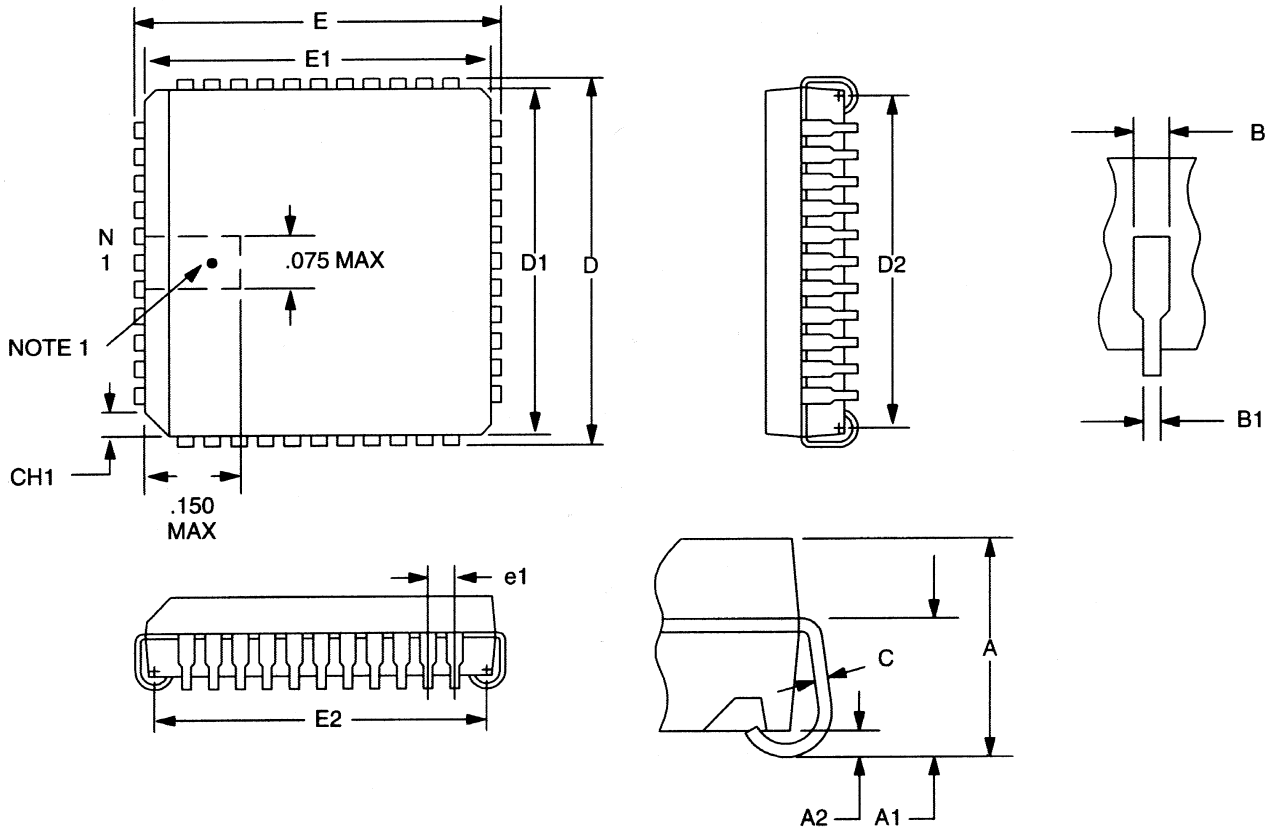
TRANSMIT SIDE AC TIMING



NOTES:

1. TSYNC is in the output mode (TCR2.2=1).
2. TSYNC is in the input mode (TCR2.2=0).
3. TSER is sampled on the falling edge of SYSCLK if the transmit side elastic store is enabled.

DS2151Q T1 CONTROLLER 44-PIN PLCC



NOTE1: PIN 1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.

DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	–
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	–