DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT40102
8-bit synchronous BCD down counter

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

8-bit synchronous BCD down counter 74HC/HCT40102

FEATURES

- Cascadable
- Synchronous or asynchronous preset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40102 are high-speed Si-gate CMOS devices and are pin compatible with the “40102” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40102 consist each of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The “40102” is configured as two cascaded 4-bit BCD counters and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output ($\overline{TC}$) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ($\overline{TE}$) is HIGH. The terminal count output ($\overline{TC}$) goes LOW when the count reaches zero if $\overline{TE}$ is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ($\overline{PE}$) is LOW, data at the jam input (P_0 to P_7) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{TE}$. When the asynchronous preset enable input ($\overline{PL}$) is LOW, data at the jam input (P_0 to P_7) is asynchronously forced into the counter regardless of the state of $\overline{PE}$, $\overline{TE}$, or CP. The jam inputs (P_0 to P_7) represent two 4-bit BCD words.

When the master reset input ($\overline{MR}$) is LOW, the counter is asynchronously cleared to its maximum count (decimal 99) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except $\overline{TE}$ are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 clock pulses long.
The “40102” may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

APPLICATIONS

- Divide-by-n counters
- Programmable timers
- Interrupt timers
- Cycle/program counters

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay CP to $\overline{TC}$	C_L = 15 pF; V_{CC} = 5 V	30	31	ns
f_{max}	maximum clock frequency		30	30	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	20	25	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	$\overline{MR}$	asynchronous master reset input (active LOW)
3	$\overline{TE}$	terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	P_0 to P_7	jam inputs
8	GND	ground (0 V)
9	$\overline{PL}$	asynchronous preset enable input (active LOW)
14	$\overline{TC}$	terminal count output (active LOW)
15	$\overline{PE}$	synchronous preset enable input (active LOW)
16	V_{CC}	positive supply voltage

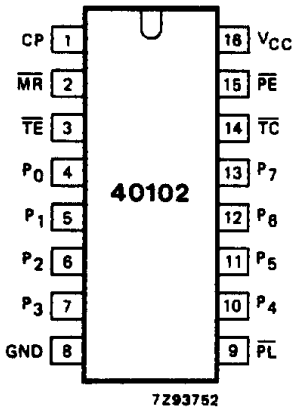


Fig.1 Pin configuration.

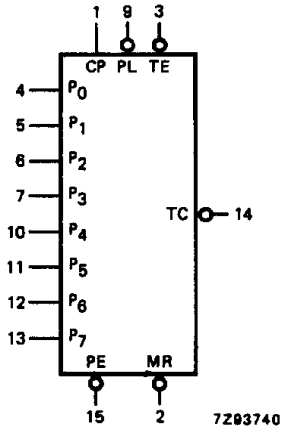


Fig.2 Logic symbol.

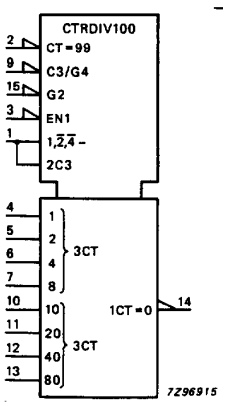


Fig.3 IEC logic symbol.

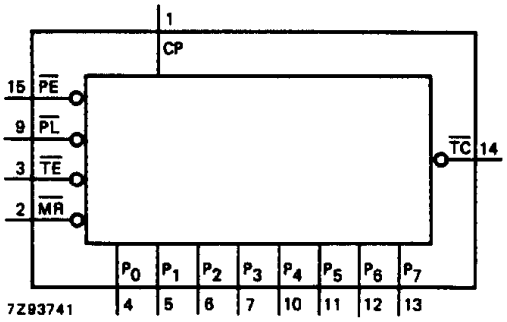


Fig.4 Functional diagram.

FUNCTION TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	synchronous	inhibit counter
H	H	H	L		count down
H	H	L	X		preset on next LOW-to HIGH clock transition
H	L	X	X	asynchronous	preset asynchronously
L	X	X	X		clear to maximum count

Notes

1. Clock connected to CP.
2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
3. Jam inputs: MSD = P_7, LSD = P_0.

H = HIGH voltage level
L = LOW voltage level
X = don't care

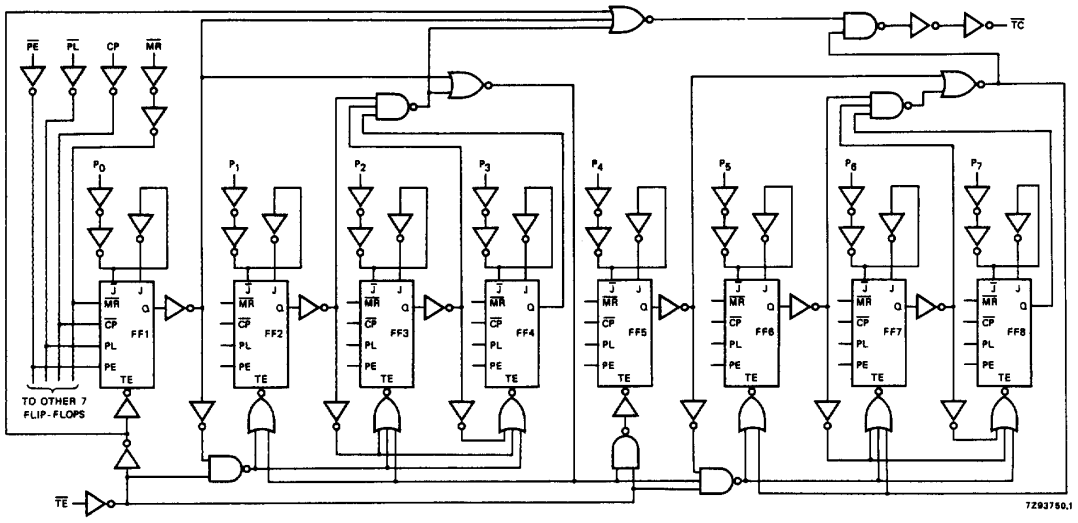


Fig.5 Logic diagram.

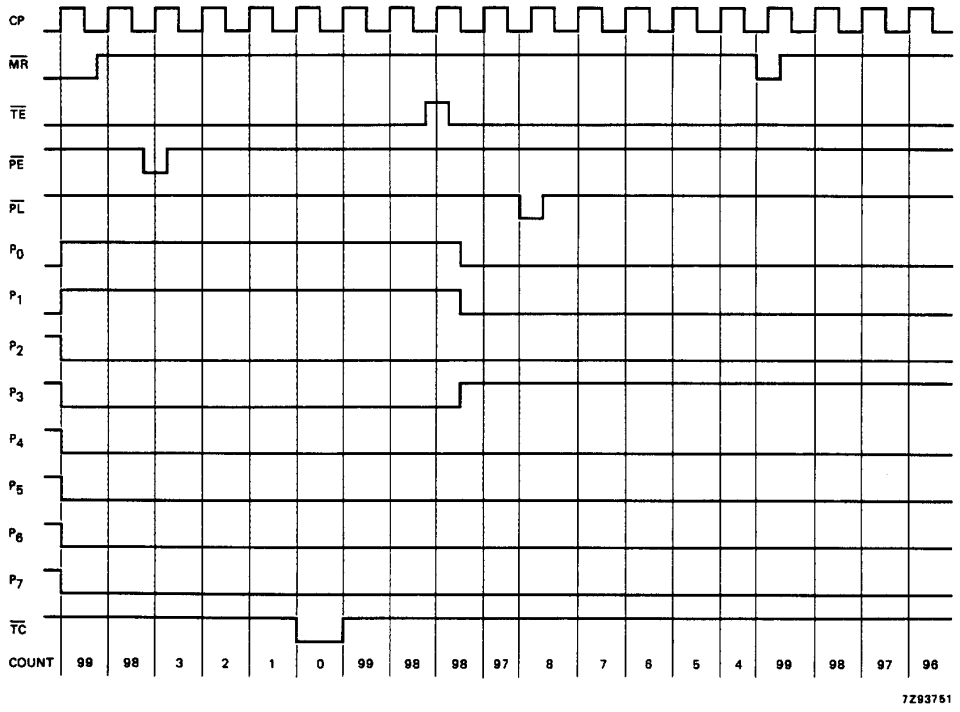


Fig.6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to $\overline{TC}$		96 35 28	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay $\overline{TE}$ to $\overline{TC}$		50 18 14	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay P_n, $\overline{PL}$ to $\overline{TC}$		110 40 32	240 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig.8
t_{PLH}	propagation delay $\overline{MR}$ to $\overline{TC}$		83 30 24	275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig.8
t_{THL}/ t_{TLH}	output transition time		9 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 8
t_W	clock pulse width HIGH or LOW	165 33 28	22 8 6		205 41 35		250 50 43		ns	2.0 4.5 6.0	Fig.8
t_W	master reset pulse width LOW	150 30 26	30 11 9		190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig.8
t_W	preset enable pulse width $\overline{PL}$; LOW	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig.8
t_{rem}	removal time $\overline{PL}$; $\overline{MR}$ to CP	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.8
t_{su}	set-up time $\overline{PE}$ to CP	100 20 17	36 13 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.8
t_{su}	set-up time $\overline{TE}$ to CP	175 35 30	50 18 14		220 44 37		265 53 45		ns	2.0 4.5 6.0	Fig.8

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{su}	set-up time P_n to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.8
t_h	hold time $\overline{PE}$ to CP	2 2 2	−8 −3 −2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.8
t_h	hold time $\overline{TE}$ to CP	0 0 0	−41 −15 −12		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.8
t_h	hold time P_n to CP	2 2 2	−5 −5 −5		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.8
f_{max}	maximum clock pulse frequency	3 15 18	8.9 27 32		2 12 14		2 10 12		MHz	2.0 4.5 6.0	Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

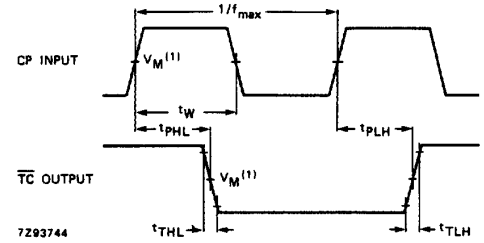
INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$, $\overline{PE}$	1.50
$\overline{MR}$	1.00
$\overline{TE}$	0.80
P_n	0.25
$\overline{PL}$	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

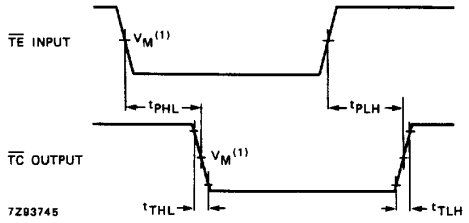
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay P_n; CP to $\overline{TC}$		38	63		79		95	ns	4.5	Figs 8 and 8
t_{PHL}/ t_{PLH}	propagation delay $\overline{TE}$ to $\overline{TC}$		25	50		63		75	ns	4.5	Fig.8
t_{PHL}/ t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}$		49	83		104		125	ns	4.5	Fig.8
t_{PLH}	propagation delay $\overline{MR}$ to $\overline{TC}$		31	55		69		83	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8 and 8
t_W	clock pulse width HIGH or LOW	33	11		41		50		ns	4.5	Fig.8
t_W	master reset pulse width LOW	30	16		38		45		ns	4.5	Fig.8
t_W	preset enable pulse width $\overline{PL}$; LOW	43	25		54		65		ns	4.5	Fig.8
t_{rem}	removal time $\overline{PL}$; $\overline{MR}$ to CP	10	1		13		15		ns	4.5	Fig.8
t_{su}	set-up time $\overline{PE}$ to CP	20	10		25		30		ns	4.5	Fig.8
t_{su}	set-up time $\overline{TE}$ to CP	40	20		50		60		ns	4.5	Fig.8
t_{su}	set-up time P_n to CP	20	12		25		30		ns	4.5	Fig.8
t_h	hold time $\overline{PE}$ to CP	0	−4		0		0		ns	4.5	Fig.8
t_h	hold time $\overline{TE}$ to CP	0	−15		0		0		ns	4.5	Fig.8
t_h	hold time P_n to CP	0	−6		0		0		ns	4.5	Fig.8
f_{max}	maximum clock pulse frequency	15	27		12		10		MHz	4.5	Fig.8

AC WAVEFORMS



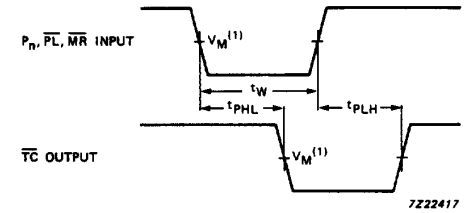
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the clock input (CP) to $\overline{TC}$ propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.



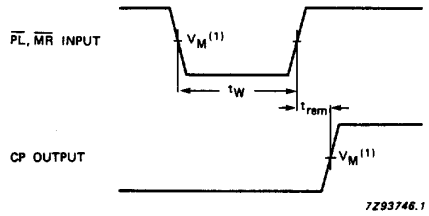
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the $\overline{TE}$ to $\overline{TC}$ propagation delays.



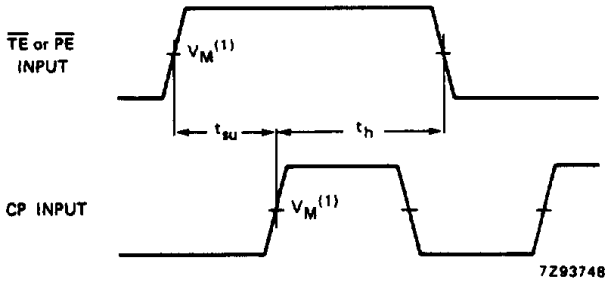
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing $\overline{PL}$, $\overline{MR}$, P_n to $\overline{TC}$ propagation delays.



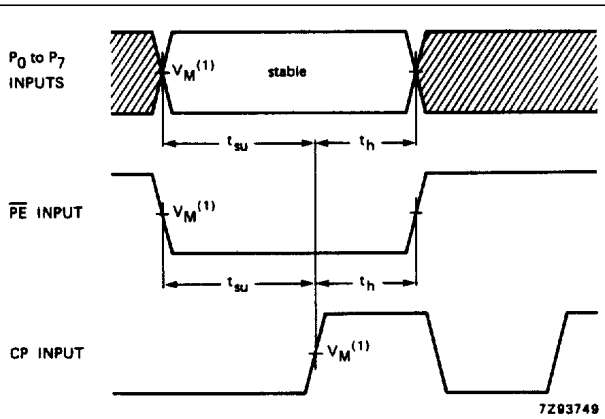
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.10 Waveforms showing removal time for $\overline{MR}$ and $\overline{PL}$.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.11 Waveforms showing hold and set-up times for $\overline{MR}$ or $\overline{PE}$ to CP.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.12 Waveforms showing hold and set-up times for P_n, $\overline{PE}$ to CP.

APPLICATION INFORMATION

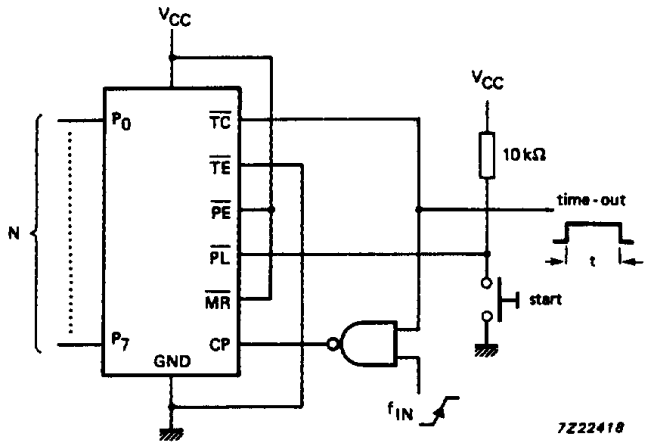


Fig.13 Programmable timer.

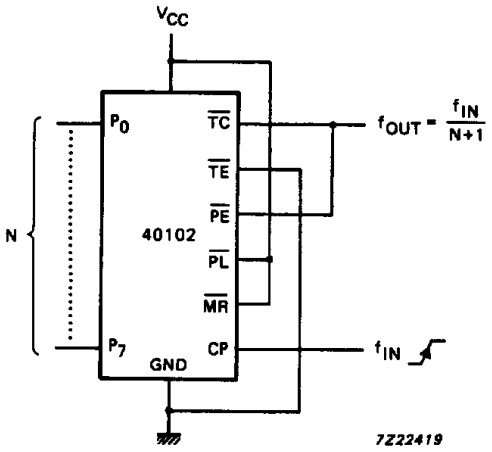


Fig.14 Divide-by-N counter.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.